TEXAS INSTRUMENTS

Unitrode Products from Texas Instruments

Interface Products (IF)

Data Book

2000

Analog and Mixed-Signal

On October 15, 1999, Texas Instruments strengthened its ability to provide you with truly premier Power Management solutions. We are proud to announce the acquisition of Power Management expert Unitrode and Battery Management expert Benchmarq.

As you may know, Unitrode has a 40-year history of designing and supplying Power Management components and subsystems. Benchmarq, based in Dallas and acquired by Unitrode last year, has won multiple awards for its industry-leading Battery Management solutions.

TI's commitment to the Power Management marketplace is already evident in its growing portfolio of industry-leading low dropout regulators, supply voltage supervisors, low-power DC-DC converters, power distribution switches and processor power products. Now, with the combination of TI's and Unitrode's high-performance products and TI's leading-edge process technologies and packaging expertise, we are positioned to provide you with easy-to-use, high-performance Power Management solutions.

Unitrode brings a family of products that complements TI's existing portfolio. TI's worldwide network of service and support increases access to and support for the Unitrode and Benchmarq portfolios. Most important, Unitrode brings to this union hundreds of experienced employees dedicated to the Power Management market.

What's in this for you? TI and Unitrode designers are working together right now to develop next-generation Power and Battery Management solutions. Maybe you're looking for easy-to-design-in, turn-key solutions. Or perhaps you need high-performance products, and complete systems and applications knowledge so you can put a power system together yourself. Either way, TI is dedicated to satisfying all of your Power Management needs today and in the future.

The combined TI and Unitrode Power Management offering comprises a rich portfolio that we intend to build upon together. To find out more, including ordering samples, you can visit our website at **www.ti.com/sc/powerleader**, complete the enclosed reply card, or call us for more information, using the TI contact information found on the back cover of this book.

Using Unitrode Data Books

Data sheets and other information about Unitrode's products are organized, by business line, into four volumes: Interface (IF), Portable Power (PP), Power Supply Control (PP), and Nonvolatile SRAMs and Real-Time Clocks (NV).

Each book contains general information as well as sections devoted to the specific business line. Information in these books is referenced in several ways.

Information Source	Volume/ Page Location			
	IF	NV	PP	PS
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Master Application Note Index by Publication Number	1-24	1-24	1-24	1-25
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Reading the Indices

The master indices, contained in all four data books, list the location of all data sheets. Each entry is preceded by one of the following 2-letter abbreviations:

- **IF** Interface
- **NV** Nonvolatile SRAMs and Real-Time Clocks
- **PP** Portable Power
- **PS** Power Supply Control

Unitrode's Products

Unitrode Corporation is a world leader in the design and manufacture of innovative, high-performance linear and mixed-signal ICs and modules. This data book introduces the Company's products designed for commercial, industrial, consumer, and military/aerospace applications.

Focused on power management, battery management, and high-speed data communications, products include:

- Off-line power management
- DC/DC power management
- Protection/supervisory circuits
- Portable power management
- Motion/motor controls
- High-speed interface
- Nonvolatile controllers and NVSRAMs
- Real-time clocks

Unitrode also offers an assortment of special function ICs, including fiber-to-curb ringers, CAN transceivers, IrDA transceivers, cellular power-management products and pager/PDA power controllers.

All Unitrode products are backed by design and applications teams that understand the interaction between the Company's products and rest of the power system/subsystem. Unitrode designs technically advanced products in response to customer needs and in anticipation of market trends.

Whatever the application—Power Management, Battery Management, or Ultrafast Data Communications—Unitrode is an innovative, dependable and customer-driven source for catalog, semi-custom, and custom linear/mixed-signal ICs and modules.

Worldwide Service

Unitrode serves its customers around the world from many locations:

- Design centers in New Hampshire, Texas, California, and North Carolina
- A facility in Dallas for assembly and manufacturing
- A facility in Singapore for testing, assembly subcontractor coordination, and customer service
- A worldwide network of manufacturers' representatives and distributors

Process Capabilities

Unitrode's bipolar process, optimized for both precision-analog and power functions, is constantly updated with the latest process options, such as:

- Operating-voltage ranges from 4–65V
- Schottky and integrated injection logic
- Ion implant
- Thin-film resistors for high accuracy
- Double-level metallization for high-density, high-current layouts and buried zener reference

The Company's BiCMOS process is ideal for high-density linear and mixed-mode designs, especially where speed and low power-consumption are of primary importance.

Options include:

- 3-, 2.5-, and 1-micron processes
- Up to 15V operation
- High-current, double-level metallization
- 125 fully isolated, vertical NPN transistors
- Thin-film resistors

This year, a new BCDMOS process offers all the options available with BiCMOS, as well as a lateral DMOS device with up to 35V operation for added power-handling capability.

An ISO9001 and 9002 Firm

Unitrode was one of the first U.S. linear/analog manufacturers to achieve IS/ISO 9001/EN29001 registration, and in 1998, the registrars completed recertification of the Merrimack and Singapore facilities and renewed the Company's registration to ISO 9001/9002-1994, respectively.

To be registered, the Company passed a rigorous examination of its quality systems—from product design through shipment. These registrations thus assure customers all over the world that Unitrode is adhering to very high, precisely defined standards.

Listening To Customers

To develop custom and semi-custom parts, Unitrode design engineers work very closely with customers, so all requirements are accurately understood, all possibilities are fully explored, and all products meet or exceed specified needs.

Unitrode also pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that satisfy them.

Important Notice

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

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Product Production Status

The table below defines three types of data sheets issued at various stages of product development. Unitrode reserves the right to change products without notice to improve design performance, reliability, or manufacturability.

CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheets	First Production	Supplementary data may be published at a later date. Unitrode reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product is in full production.


UNITRODE

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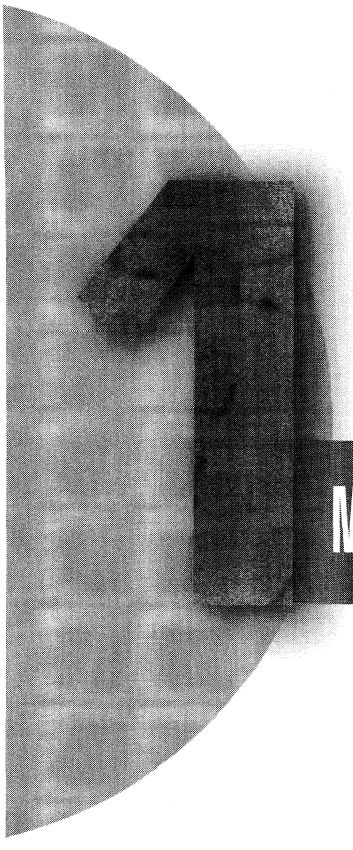

Master Part Number and Application Indices

Numeric Master Part Index

Part numbers are listed numerically, not by prefix (bq, DV, EV, UC, UCC).
Products included in this book are listed in ***bold****.*

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Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-64	Inductorless Bias Supply for Synchronous Rectification and High Side Drive Applications	UCC3583	PS/3-502
DN-65	Considerations in Powering BiCMOS ICs	UCC3809-1,-2	PS/3-505
DN-66	Unitrode - UC3854A/B and UC3855A/B Provide Power Limiting with Sinusoidal Input Current for PFC Front Ends	UC3854A/B	PS/4-86
DN-67	UCC3913 Electronic Circuit Breaker for Negative Voltage Applications Evaluation Kit List of Materials for a -48V/1A Test Circuit	UCC3913	IF/5-105
DN-68	Parelling UCC3912 Electronic Circuit Breaker ICs	UCC3912	IF/5-106
DN-70	UC3573 Buck Regulator PWM Control IC	UC3573	PS/3-508
DN-72	Lamp Ignitor Circuit	UCC3305	PS/9-52
DN-73	UCC3941 One Volt Boost Converter Demonstration Kit - Schematic and List of Materials	UCC3941-3/5/ADJ	PP/7-101
DN-75	Using the UC3871 and UC3872 Resonant Fluorescent Lamp Drivers in Floating Lamp Applications	UC3872	PP/8-50
DN-76	Closed Loop Temperature Regulation Using the UC3638 H-Bridge Motor Controller and a Thermoelectric Cooler	UC3638	PS/8-118
DN-77	Overcurrent Shutdown with the UC3853	UC3853	PS/4-91
DN-78	High Power Factor Preregulator IC, Evaluation Board, Schematic and List of Materials	UC3853	PS/4-92
DN-79	UCC3750 Demonstration Board Operating Guidelines	UCC3750	PS/9-55
DN-81	UCC3911 Demo Board Information	UCC3911	PP/6-51
DN-82	UCC3958 Demonstration Board Schematic and Bill of Materials	UCC3958	PP/6-55
DN-83	UC3584 DW Secondary Side Post Regulator, Evaluation Board, Schematic, and List of Materials	UC3584	PS/3-511
DN-84	UCC3956 Switch Mode Lithium-Ion Battery Charger Controller Evaluation Board, Schematic and List of Materials	UCC3956	PP/3-413
DN-85	UCC3831 USB Power Controller IC, Evaluation Board – Schematic and List of Materials	UCC3831	IF/5-106
DN-86	UCC3954 Single Cell Lithium-Ion to +3.3V Converter Performance Evaluation Kit – Schematic and List of Materials	UCC3954	PP/7-103
DN-87	UCC3918 Low On-Resistance Hot Swap Power Manager Performance Evaluation Kit , Schematic and List of Materials	UCC3918	IF/5-113
DN-88	UCC5342 IrDA 115.2kbps Tranceiver Performance Evaluation Board – Schematic and List of Materials	UCC5342	PP/9-15
DN-89	Comparing the UC3842, UCC3802, and UCC3809 Primary-Side PWM Controllers	UC3842/3/4/5	PS/3-514
DN-90	UCC3858 "Energy Star" PFC Evaluation Board, Schematic and List of Materials	UCC3858	PS/4-94
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DN-92	UCC5630 SCSI Multimode (LVD/SE) Evaluation Board and List of Materials	UCC5630	IF/3-122
DN-93	UCC3957, Three - Four Cell Lithium-Ion Protector Circuit, Evaluation Board and List of Materials	UCC3957	PP/6-57
DN-94	UCC5343, IrDA Transceiver with Encoder/Decoder, Evaluation Board and List of Materials	UCC5343	PP/9-19
DN-95	UCC3919 Hot Swap Power Manager Evaluation Circuit Board and Bill of Materials	UCC3919	IF/5-116
DN-96	UCC3952 Evaluation Board and List of Materials	UCC3952	PP/6-61

*Publications included in this book are listed in **bold**.*

Application/Design Notes by Publication Number

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DN-97	UCC39411 Low Power Synchronous Boost Converter Evaluation Kit, Schematic and Bill of Materials	UCC39411/2/3	PP/7-106
DN-98	UCC3917 Positive Floating Hot Swap Power Manager Evaluation Kit, Schematic and Bill of Materials	UCC3917	IF/5-120
DN-99	Pulse Edge Transmission (PET) circuit	UCC3961	PS/8-102
DN-501	Using RAM Clear Function with bq3285/bq3287A RTCs	bq3285/bq3287	NV/4-321
DN-502	High-Side Current Sensing with Benchmarq Portable Power Fast-Charge Control IC		PP/3-307
U-100A	UC3842/3/4/5 Provides Low-Cost Current-Mode Control	UC3842/3/4/5	PS/3-532
U-102	UC1637/2637/3637 Switched Mode Controller for DC Motor Drive	UC3637	PS/8-126
U-104	Improved Charging Methods for Lead-Acid Batteries using the UC3906	UC3906	PP/3-388
U-110	1.5MHz Current Mode IC Controlled 50W Power Supply	UC3825	PS/3-546
U-111	Practical Considerations in Current Mode Power Supplies	UC3709	PS/3-558
U-112	A High Precision PWM Transconductance Amplifier for Microstepping using Unitrode's UC3637	UC3637	PS/8-137
U-113	Design Notes on Precision Phase Locked Speed Control for DC Motors	UC3634	PS/8-145
U-115	New Integrated Circuit Produces Robust, Noise Immune System for Brushless DC Motors	UC3625	PS/8-155
U-118	New Driver ICs Optimize High Speed Power MOSFET Switching Characterisitics	UC3709	PS/6-92
U-120	A Simplified Approach to DC Motor Modeling for Dynamic Stability Analysis	UC3638	PS/8-162
U-122	A New Family of Integrated Circuits Controls Resonant Mode Power Converters	UC3861-8	PS/3-576
U-127	Unique Chip Pair Simplifies High Side Switch Drive	UC3725	PS/6-107
U-128	The UC3823A,B & UC3825A,B Enhanced Generation of PWM Controllers	UC3823/5A/B/3	PS/3-585
U-129	UC3907 Load Share IC Simplifies Parallels Power Supply Design	UC3907	PS/7-84
U-130	Dedicated ICs Simplify Brushless DC Servo Amplifier Design	UC3625	PS/8-166
U-131	Simple Switchmode Lead-Acid Battery Charger	UC3906	PP/3-417
U-132	Power Factor Correction Using the UC3852 Controlled ON-Time Zero Current Switching Technique	UC3852	PS/4-98
U-133A	UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs	UCC3800/1/2/3/4/5	PS/3-594
U-134	UC3854 Controlled Power Factor Correction Circuit Design	UC3854	PS/4-114
U-135	The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters	UC3848	PS/3-612
U-136A	Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller	UC3875/6/7/8	PS/3-623
U-137	Practical Considerations in High Performance MOSFET, IGBT & MCT Gate Drive Circuits	UC3709	PS/6-122
U-138	Zero Voltage Switching Resonant Power Conversion	UC3861-8	PS/3-637
U-140	Average Current Mode Control of Switching Power Supplies	UC3849	PS/3-664
U-141	Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution	UC3871	PP/8-27
U-143C	New Chip Pair Provides Isolated Drive for High Voltage IGBTs	UC3727	PS/6-137
U-144	UCC3806 BiCMOS Current Mode Control IC	UCC3806	PS/3-678
U-148	Dimmable Cold-Cathode Fluorescent Lamp Ballast Design Using the UC3871	UC3871	PP/8-35
U-149A	Simple Off-Line Bias Supply for Very Low Power Applications	UCC3888	PS/3-685

*Publications included in this book are listed in **bold**.*

Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
U-150	Applying the UCC3570 Voltage-Mode PWM Controller to Both Off-Line and DC/DC Converter Designs	UCC3570	PS/3-696
U-151	UCC3912 Integrated Hot Swap Power Manager™ IC for Hot-Swap and Power Management Applications	UCC3912	IF/5-124
U-152	A High Performance Linear Regulator for Low Dropout Applications	UC3832/3	PS/5-71
U-153	UC3855A/B High Performance Power Factor Preregulator	UC3855A/B	PS/4-134
U-154	The New UC3879 Phase Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters	UC3879	PS/3-709
U-155	Implementing Multi-State Charge Algorithm with the UC3909 Switchmode Lead-Acid Battery Charger Controller	UC3909	PP/3-426
U-156	The UC3886 PWM Controller Uses Average Current Mode Control to Meet the Transient Regulation Performance of High End Processors	UC3886	PS/3-717
U-157	Fueling the Megaprocessor - A DC/DC Converter Design Review Featuring the UC3886 and UC3910	UC3886	PS/3-741
U-158	The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies	UC3910	PS/3-771
U-159	Boost Power Factor Corrector Design with the UC3853	UC3853	PS/4-154
U-161	Powering a 35W DC Metal Halide High Intensity Discharge (HID) Lamp using the UCC3305 HID Lamp Controller	UCC3305	PS/9-61
U-163	The UC3902 Load Share Controller and Its Performance in Distributed Power Systems	UC3902	PS/7-100
U-164	The UCC3884 Frequency Foldback Pulse Width Modulator	UCC3884	PS/3-783
U-165	Design Review: Isolated 50W Flyback with the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier	UC3965	PS/3-800
U-166	An Off-Line Lead-Acid Charger Based on the UC3909	UC3909	PP/3-399
U-167	UC3578 Telecom Buck Converter Evaluation Board	UC3578	PS/3-818
U-168	Implementing an Off-Line Lithium-Ion Charger Using the UCC3809 Primary Side Controller and the UCC3956 Battery Charger Controller	UCC3809-1,-2	PS/3-455
U-169	The New UCC3750 Source Ringer Controller Provides A Complete Control Solution for a Four-Quadrant Fluback Converter	UCC3750	PS/9-76
U-500	Using the bq4845 for a Low-Cost RTC/NVSRAM Subsystem	bq4845	NV/4-310
U-502	Time-Base Oscillator for RTC ICs		NV/4-322
U-503	Using the bq3285/7E in a Green or Portable Environment	bq3285/7E	NV/4-331
U-504	Using the bq2000/T to Control Fast Charge	bq2000/T	PP/3-262
U-505	Using the bq2003 to Control Fast Charge	bq2003	PP/3-273
U-506	Step-Down Switching Current Regulation Using the bq2003 Fast-Charge IC	bq2003	PP/3-291
U-507	Using the bq2005 to Control Fast Charge	bq2005	PP/3-309
U-508	Using the bq2007 Display Mode Options	bq2007	PP/3-327
U-509	Using the bq2007 Enhanced Features for Fast Charge	bq2007	PP/3-332
U-510	Using the bq2031 to Charge Lead-Acid Batteries	bq2031	PP/3-346
U-511	Switch-Mode Power Conversion Using the bq2031	bq2031	PP/3-360
U-512	Using the bq2902/3 Rechargeable Alkaline ICs	bq2902/3	PP/3-376
U-513	Using the bq2040: Smart Battery System Gas Gauge IC	bq2040	PP/4-372
U-514	Using the bq2010: A Tutorial for Gas Gauging	bq2010	PP/4-390
U-93	A New Integrated Circuit for Current Mode Control	UC3846/7	PS/3-518
U-94	The UC1901 Simplifies the Problem of Isolated Feedback in Switching Regulators	UC3901	PS/7-72
U-95	Versatile UC1834 Optimizes Linear Regulator Efficiency	UC3834	PS/5-49
U-97	Modeling, Analysis and Compensation of the Current Mode Converter	UCC3813	PS/3-526
U-99	UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor	UC3717	PS/8-118

*Publications included in this book are listed in **bold**.*

INTERFACE (IF)

Hot Swap Power Managers

SCSI

NONVOLATILE SRAMs AND REAL-TIME CLOCKS (NV)

Real-Time Clocks

PORTABLE POWER (PP)

Battery Charging

*Publications included in this book are listed in **bold**.*

Battery Capacity Monitoring

Cold Cathode Fluorescent Lamp Driver (CCFL)

Lighting Circuits

Reference Designs

CCFL Drives

Battery Protection

Battery Charging

POWER SUPPLY CONTROL (PS)

Bias Supplies

Bootstrap Circuits

Publications included in this book are listed in ***bold****.*

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Frequency Foldback

Gate Drives

Isolation Amplifier

Leading Edge Blanking

Lighting Circuits

Linear Voltage Regulators

Load Sharing

Magnetics Design

*Publications included in this book are listed in **bold**.*

Microprocessor Voltage Regulators

Linear Regulators

Switching Regulators

Motor Control

Brush DC Motors

Brushless DC Motors

Phase Locked Loops

Power H-Bridge Design

Small Signal Modeling

Stepper Motors

Optocoupler Isolation

Post Regulation

Power Device Drivers

Publications included in this book are listed in ***bold****.*

Power Factor Correction

PWM Oscillators

Rectification

Resonant Converters

Ring Generator Controllers

*Publications included in this book are listed in **bold**.*

Secondary Side Regulation

Small Signal Analysis

Subharmonic Oscillation

Supervisory Functions

Switching Regulators - Reference Designs

Flyback Converters

Forward Converters

Non-Isolated Buck, Boost, Flyback and SEPIC Converters

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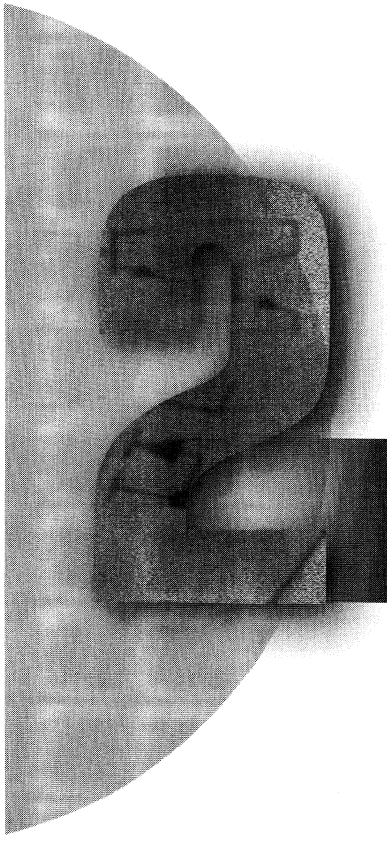


General Information

Ordering Information

(see Benchmarq ordering information page for "bq" prefix products)

UC	XXXXX	XX	XX	XXXX	general syntax
UC	17131 27131 37131	A	J	883B	example

PREFIX
"UC" ~ Linear Integrated Circuits
"UCC" ~ BiCMOS

PART NUMBER
First digit "1" ~ Military Temperature Range*
First digit "2" ~ Industrial Temperature Range*
First digit "3" ~ Commercial Temperature Range*
(*consult individual data sheets for specific temperature ranges on each part)

SCREEN/PROCESSING OPTIONS
"883" ~ MIL-STD-883
Class Q of MIL-PRF-38535

PACKAGE OPTIONS

OPTIONAL GRADES
A or B ~ Improved Version

Letter Designator	Package Type
D	Plastic Narrow Body (150 mil) SOIC
DW	Plastic Wide Body (300 mil) SOIC
DP	Plastic Narrow Body Power SOIC
DS	Plastic Narrow Body (150 mil) SOIC with Shunt Current Sense
DWP	Plastic Wide Body Power SOIC
FP	Power Plastic Metric Quad Flatpack (MQFP)
FQ	Power Low Profile Quad Flatpack (LQFP)
FQP	Power Plastic Low Profile Quad Flatpack (LQFP)
J	Ceramic Dual-in-Line (300 mil and 600 mil)
L	Ceramic Leadless Chip Carrier
LP	Power LCC
M	Quasi Shrink Small Outline (150 mil body, 0.635mm pitch)
MWP	Power Quasi Shrink Small Outline (300 mil body, 0.88mm pitch)
N	Plastic Dual-in-Line (300mil and 600 mil)
P	Mini SOIC
PW	Thin Shrink Small Outline (TSSOP)
PWP	Power TSSOP
Q	Plastic Leadless Chip Carrier (PLCC)
QP	Power (PLCC)
SP	Power Ceramic Dual-in-Line
T	Plastic TO-220
TD	Plastic TO-263 Power Surface Mount
Z	Zig-Zag In-Line Power Package

Quality and innovation characterize our products!

Our commitment begins with our Quality Assurance System. In October 1992, Unitrode Corporation became one of the first in our industry to achieve IS/ISO 9001/EN 29001 Registration. Currently, Unitrode's quality-assurance system exceeds the rigorous requirements of ISO 9001-1994 and MIL-PRF-38535. Quality Management Institute (QMI) has awarded Unitrode a Certificate of Registration (Number 003889) indicating compliance with ISO 9001, for the design and manufacture of analog integrated circuits. For its Singapore branch, Unitrode also holds an ISO 9002 Certificate of Registration (Number 93-2-0148) from the Singapore Productivity and Standards Board, for semiconductor IC manufacturing, factory inspection and testing, and wafer-probe testing.

In August 1996, the Defense Supply Center-Columbus (DSCC) granted Unitrode full Q-Level certification to MIL-PRF-38535 for listing on the Qualified Manufacturers List (QML). In addition, DSCC continued Unitrode's laboratory suitability by certifying that our test methods accord with MIL-STD-883.

All Unitrode products and manufacturing processes meet extensive qualification requirements. Qualification ensures that

- Customer and/or design requirements are translated efficiently into manufacturing requirements
- All groups are integrated, coordinated, and capable
- Our processes are manufacturable
- Our products meet or exceed the reliability requirements of our customers

Process Qualification

When a process qualification is required, Quality Assurance organizes a cross-functional team that prepares and completes a formal qualification plan according to QP 2515. Key requirements for major processes include

- Documented design rules and process specifications; process and device simulation with full SPICE models
- Completed process control plan with identified critical, significant, and non-critical characteristics
- Implemented process-control charts
- Demonstrated Cp, and Cpk for significant and critical characteristics
- Documented out-of-control action plans (OCAPs)
- Completed quality audit
- Process-acceptance criteria
- Gage R&R studies
- Construction analyses

Reliability Testing

Our extensive reliability requirements ensure that our new processes demonstrate, for commercial products under typical use conditions, a 200 FIT rate or better (failures in time calculated at 70°C, 0.7eV activation energy, 60% confidence) at the time of qualification, using a minimum of three wafer lots. Figure 1, on page 2-6, lists typical reliability tests performed for new major processes.

Package Qualification

Whenever a new package is introduced, in addition to qualifying the manufacturing process using requirements appropriate to assembly processing, Unitrode performs a complete battery of reliability tests.

Figure 2, on page 2-7, depicts typical requirements for plastic packages. Figure 3, on page 2-8, presents the requirements for hermetic packages.

Product Qualification

New products must be manufactured using qualified processes and packages. Unitrode's new product qualification consists of 2 major milestones: Release For Introduction (RFI) and Release to Production (RTP).

RFI is the term Unitrode uses to describe devices that

- Are built on a qualified process
- Meet the preliminary data sheet over the specified temperature range
- Demonstrate no infant mortality
- Have been verified in the appropriate application
- Have had ESD measured and classified
- Have a released preliminary test program

Devices that achieve RTP meet all the RFI requirements (plus additional requirements) and complete Unitrode's product qualification. Typical RTP requirements include

- Bench and temperature characterization
- Demonstrated compliance to all data-sheet parameters
- Cp, Cpk targets met for all untrimmed parameters in data sheet
- Test program complete and released to production
- Machine capability less than 5% of the device specification range
- Test schematic(s), test program(s), bonding diagram(s), and burn-in diagrams approved and released
- ESD measured and classified (human body model)
- Passed latch-up and HTOL test to 1000 hours
- Final data sheet approved and released.

Results

As a result of our comprehensive qualification procedures, we are able to report long-term device reliability of 4.0 FIT or lower for combined functional families. This figure is estimated from millions of hours of life-testing at accelerated temperatures.

Failure Analysis

If we do experience a failure during pre-production qualification, we have an extensive failure-analysis lab to determine and fix the root cause before the products reach our customers. We begin by verifying the failure to published specifications. We provide written failure-verification to our customers within 72 hours.

This notification is followed by failure-mode identification through laboratory analyses such as electrical measurements, optical and electron microscopy, radiography, device deprocessing, microsectioning, spectrometry, and cholesteric liquid-crystal analysis. Unitrode maintains a ten-day cycle to identify moderately complex failures from receipt of failed units.

If needed, closed-loop corrective action is managed through our Corrective Action Continuous Improvement Team using the 8D approach.

Customer Notification

Our continuous improvement requires an occasional product or process change. Unitrode notifies the customer (a 90-day notification whenever possible) when

- A waiver to a customer's or Unitrode's specification is required before shipment of material deemed suitable by Unitrode or our customer
- Any product, process or mask change requires a change to Unitrode's data sheet, SCD, purchase order, or customer specification
- Any product, process or mask change reduces ESD rating
- A change occurs in manufacturing location, including wafer fabrication, assembly, and test
- There is a change in wafer starting material, dieletric, passivation or metalization materials and certain assembly materials
- A major change occurs in manufacturing process on a critical or significant characteristic, according to our process control plan(s)
- A manufacturing process changes a characteristic that is a reliability concern
- Unitrode's operating procedures or quality systems change significantly

Total Business Excellence

Unitrode's policy of Total Business Excellence (TBE) goes well beyond the scope of Quality Assurance. A company demonstrating Total Business Excellence must have more rigorous business practices than industry standards and a supporting culture to enable and improve these practices.

TBE requires continuous improvement. It is a never-ending search for ways to improve everything we do, and a pledge to ultimately translate improvements into better products and services for our customers.

Our goals include improved designs that meet the broadest spectrum of application needs, improved translation of customer requirements into actual product performance characteristics, improved understanding of process capabilities to improve the product introduction process, higher productivity, less scrap and rework, and lower production costs.

For example, Unitrode internal qualification procedures now include rigorous qualification of our suppliers, subcontractors, and the wafer fabrication (both major new processes and unit processes). Each qualification is managed by a cross-functional quality team. Qualification requirements include detailed and advanced process control plans, out-of-control action plans (OCAPs), demonstrated process-capability, advanced statistical process-control techniques, and Gage R&R studies.

We've improved many of our internal practices: for example, shop floor control, document management, customer notification, and corrective action. We've replaced our old hardcopy system with electronically based systems using the best software systems and relational databases.

Total Business Excellence affects every department, activity, and product, from initial concept to end-user installation and operation.

For all of these reasons we deliver high-quality, reliable products. Our continuing quest to improve everything we do yields better and more reliable products and services for our customers. That is what earns customer loyalty!

Figure 1. Typical Reliability Tests for New Processes

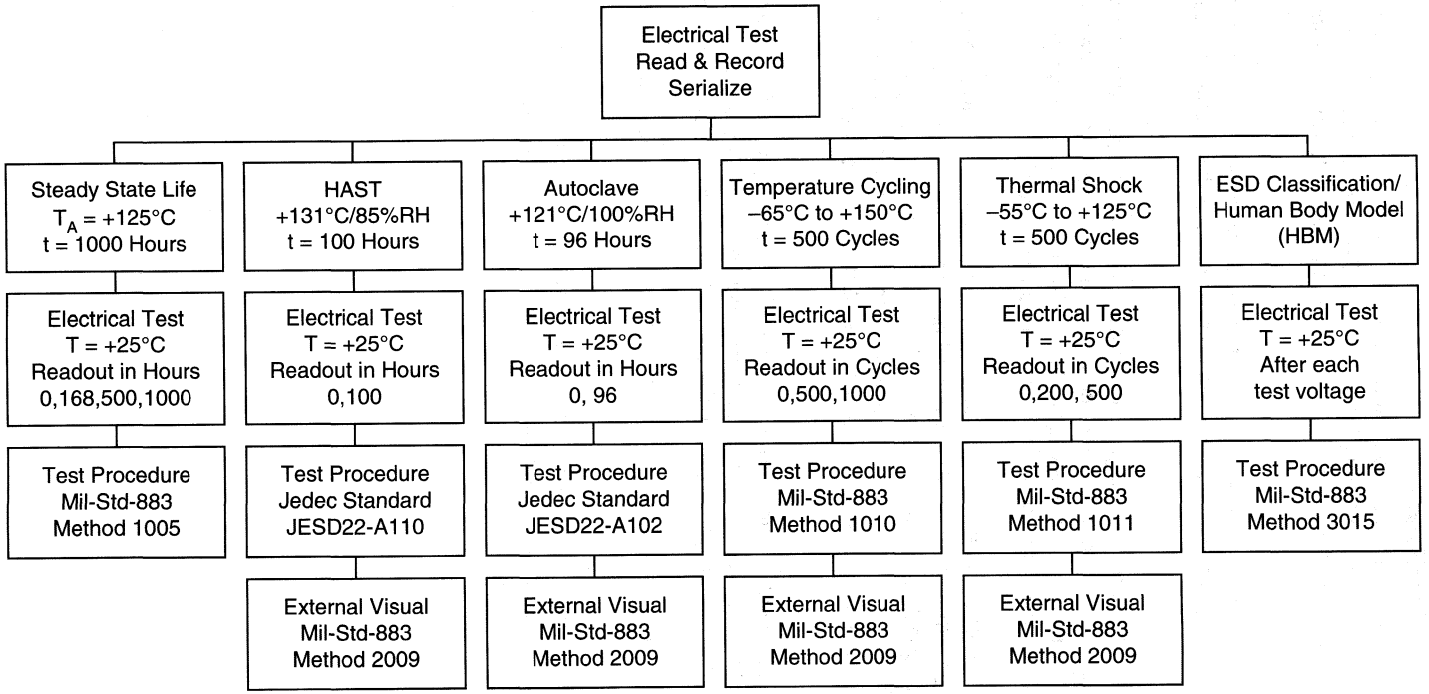
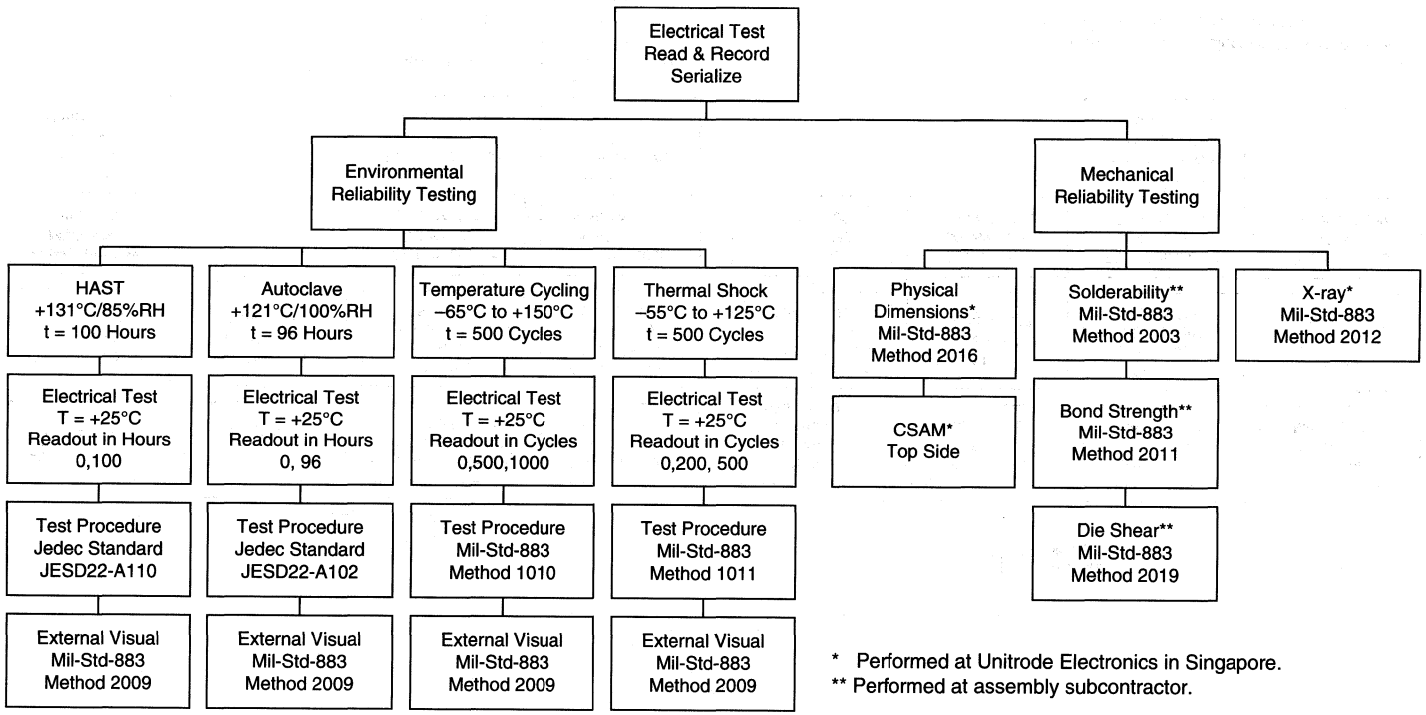
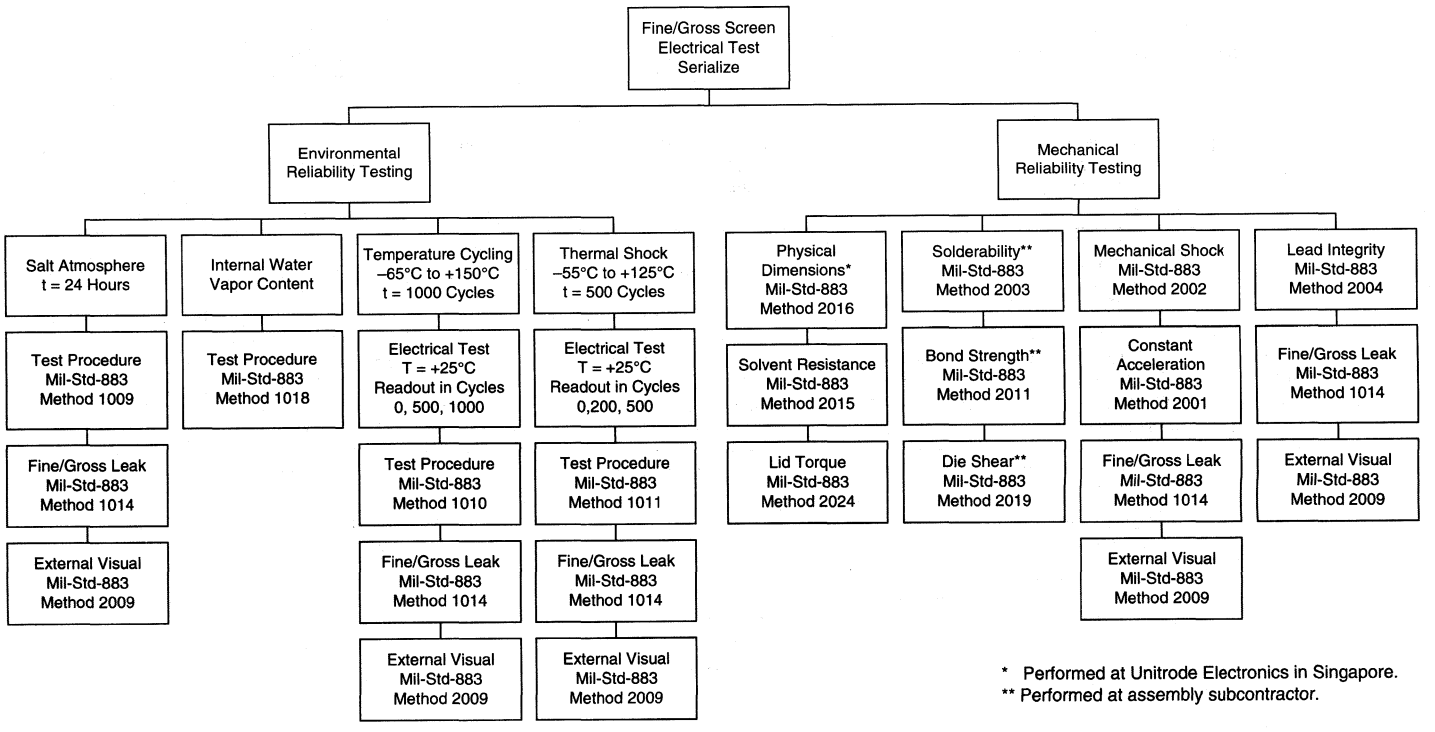


Figure 2. Typical Reliability Requirements for Plastic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Figure 3. Typical Reliability Requirements for Hermetic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Description

Unitrode offers most of our products in die and/or wafer form through our die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques.Die thickness is either 12 mils or 15 mils, +/- 1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing

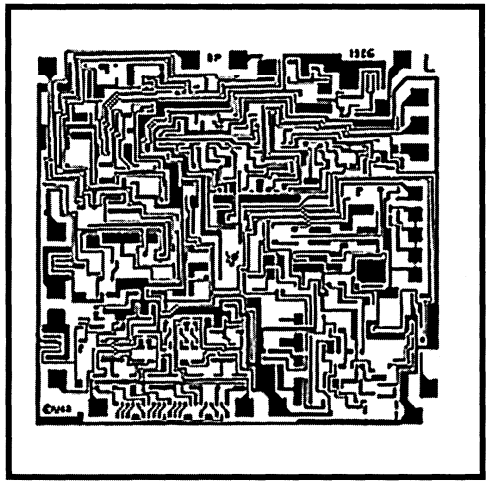
All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications, with the exception of some high power or high speed devices where production probe equipment limit the test environment.

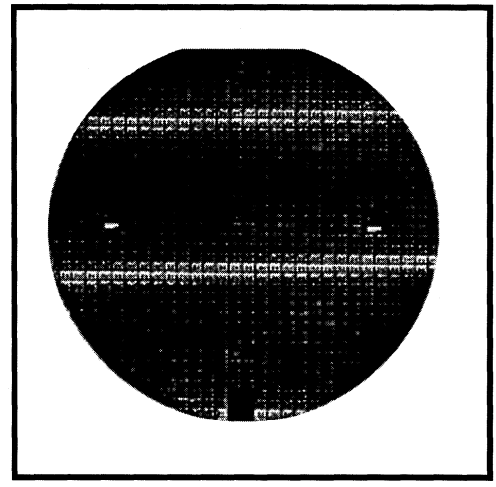
Inspection

Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering

Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.



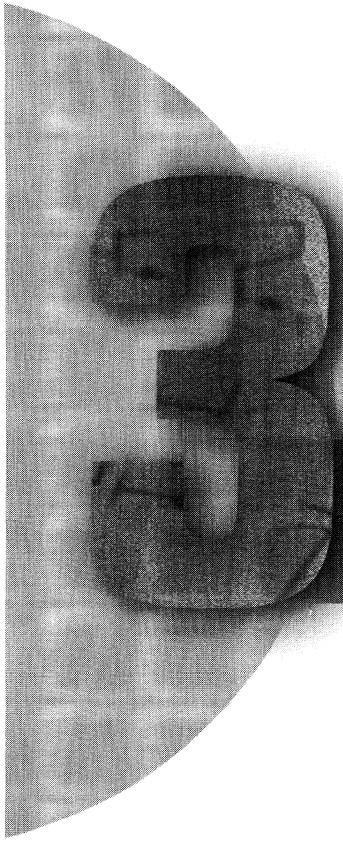


Small Computer Systems Interface (SCSI)

Bus Bias Generators

Hot Swap Power Manager™ ICs

Drivers/Receiver Transceivers



SCSI

SCSI

Multimode/ LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5628+	UCC5630	UCC5632	UCC5638+	UCC5639+
Channels	14	9	9	15	15
Channel Capacitance	4	4	4	4	4
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150
Disconnect High or Low	H	H	H	H	L
TermpwrVoltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD / SE	LVD / SE
Page Number	IF/3-78	IF/3-83	IF/3-93	IF/3-94	IF/3-99

Multimode/ LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5640+	UCC5641+	UCC5646		
Channels	9	9	27		
Channel Capacitance	3	3	3		
Termination Impedance	Differential 105, Common Mode 150	Differential 105, Common Mode 150	Differential 105, Common Mode 150		
Disconnect High or Low	H	L	H		
TermpwrVoltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type LVD or SE / LVD	LVD	LVD	LVD		
Page Number	IF/3-104	IF/3-108	IF/3-112		

+ New Product

SCSI (cont.)

Multimode LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5510+	UCC5630A	UCC5672+	UCC5680	
Channels	9	9	9	9	
Channel Capacitance	4	4	4	4	
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	
Diff B input filter	N	N	Y	Y	
Disconnect High or Low	N/A	H	H	H	
TermpwrVoltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	
Supports Active Negation	Y	Y	Y	Y	
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD	
Page Number	IF/3-5	IF/3-87	IF/3-120	IF/3-121	

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5601	UC5602	UC5603	UC5604	UC5605
Channels	18	18	9	9	9
Channel Capacitance	10	11	6	9	4
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	H	H	H	L
TermpwrVoltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	N	N	Y	N	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-9	IF/3-13	IF/3-18	IF/3-22	IF/3-26

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5606	UC5607	UC5608	UC5609	UC5612
Channels	9	18	18	18	9
Channel Capacitance	1.8	8	6	6	4
Termination Impedance	110 & 2500	110	110	110	110
Disconnect High or Low	L	2L	H	L	H
TermpwrVoltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-30	IF/3-34	IF/3-37	IF/3-40	IF/3-43

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5613	UCC5614	UCC5617	UCC5618	UCC5619
Channels	9	9	18	18	27
Channel Capacitance	3	1.8	2.5	2.5	3
Termination Impedance	110	110 & 2500	110	110	110
Disconnect High or Low	H	H	L	H	L
TermpwrVoltage Range	4 - 5.25	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-47	IF/3-51	IF/3-55	IF/3-59	IF/3-63

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5620	UCC5621	UCC5622		
Channels	27	27	27		
Channel Capacitance	3	3	3		
Termination Impedance	110	110	110		
Disconnect High or Low	H	Split Low	Split High		
TermpwrVoltage Range	4 - 5.25	4 - 5.25	4 - 5.25		
Supports Active Negation	Y	Y	Y		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type SE, LVD or SE / LVD	SE	SE	SE		
Page Number	IF/3-66	IF/3-70	IF/3-74		

Special Functions Circuit	UNITRODE PART NUMBER		
	UCC5661		
Part Name	Ethernet Coaxial Impedance Monitor		
Description	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT		
Page Number	IF/3-112		

+ New Product

Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator

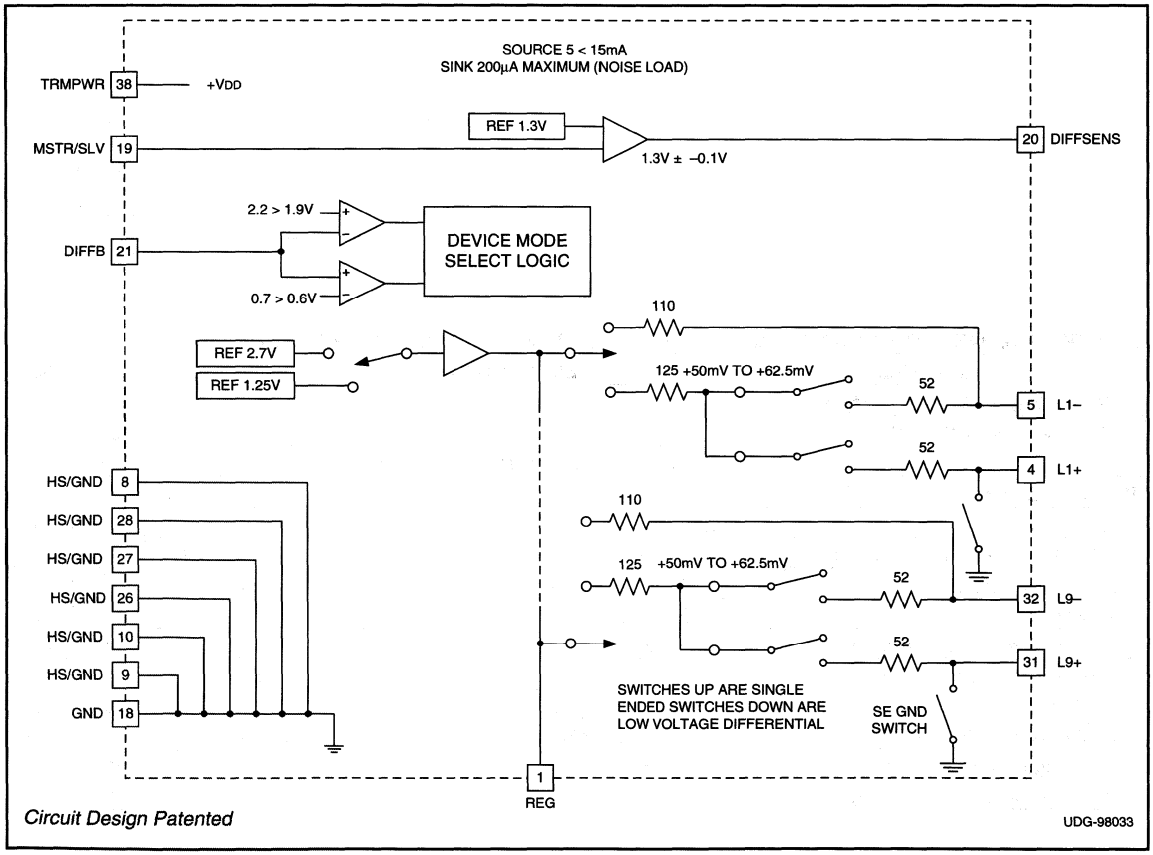
FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 3.0V to 5.25V Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF
- Master/Slave Inputs
- Supports Active Negation
- 3pF Channel Capacitance

DESCRIPTION

The UCC5510 Multi-Mode Low Voltage Differential and Single Ended Terminator is specially designed for automatic termination of Single-Ended or Low Voltage Differential SCSI Bus. The Multi-Mode operation of this device allows for a transition system design for the next generation SCSI Parallel Interface (SPI-2). Compliant with SPI-2, with SPI and Fast-20 the UCC5510 incorporates all the functions necessary to properly terminate the SCSI Bus and has internal thermal shut down and short circuit limiting.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Power Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

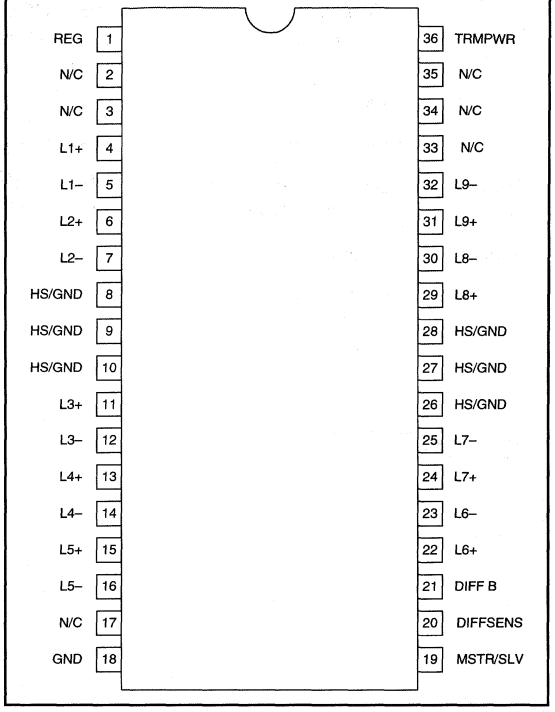
RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 3.0V TO 5.25V

All voltages are with respect to pin 1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-36 (Top View)
MWP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current				20	mA
	Disable Terminator, in DISCNCT mode.			35	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	LVD Mode, Differential Sense Floating	–80	–100		mA
1.25V Regulator Sink Current	LVD Mode, Differential Sense Floating	80	100		mA
1.3V Regulator	DIFFSENS	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFFSENS	–5		–15	mA
1.3V Regulator Sink Current	DIFFSENS	50		200	µA
2.7V Regulator	Single Ended Mode	2.5	2.7	3	V
2.7V Regulator Source Current	Single Ended Mode	–200	–400	–800	mA
2.7V Regulator Sink Current	Single Ended Mode	100	200	400	mA
2.7V Regulator Dropout Voltage	$V_{TRMPWR} - (V_{REG} - 3.0\ Min)$			200	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance		110	125	165	Ω
Differential Bias Voltage	Drivers Tri-stated	100		125	mV
Common Mode Bias			1.25		V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance		102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V	–21	–23	–24	mA
	Signal Level 0.5V			–22.4	mA
Output Leakage	Disabled, TRMPWR = 0V to 5.25V			400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SW Impedance				60	Ω
Differential Sense (DIFF B) Input Sections					
DIFFB Single Ended Threshold		0.6		0.7	V
DIFFB Sense LVD Threshold		1.9		2.2	V
DIFFB Input Current	V_{DIFFB} = 0V and 3.3V	–10		10	µA
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold		0.8		2	V
MSTR/SLV Input Current		–30		30	µA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

DIFFB: DIFF SENSE filter pin should be connected to a 0.1µF capacitor to GND and 20k resistor to SCSI/Bus DIFF SENSE Line.

DIFFSENS: The SCSI bus DIFF SENSE line is driven to 1.3V to detect what type of devices are connected to the SCSI bus.

HS/GND: Heat Sink GND. Connect to large area PC board traces to increase power dissipation capability.

GND: Power Supply Return.

L1– thru L9–: Signal line/active line for single ended or negative line in differential applications for the SCSI bus.

L1+ thru L9+: Ground line for single ended or positive line for differential applications for the SCSI bus.

MSTR/SLV: Mode select for the non-controlling terminator. MSTR enables the 1.3V regulator, when the terminator is enabled. ***Note:*** *This function will be removed on further generations of the multimode terminators.*

REG: Regulator bypass, must be connected to a 4.7µF capacitor.

TRMPWR: V_{IN} 3.0V to 5.25V supply.

APPLICATION INFORMATION

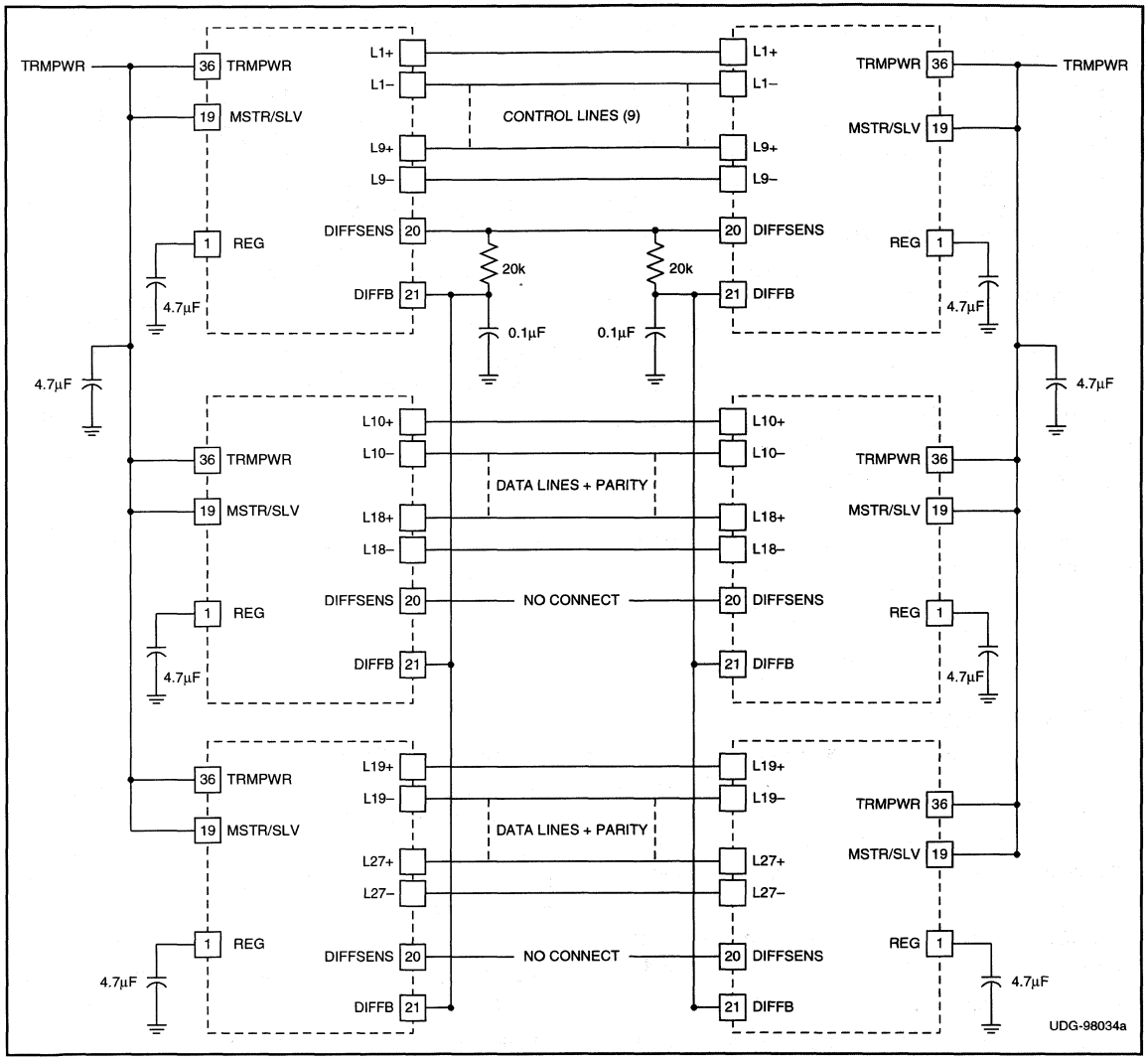


Figure 1. Application Drawing

The master is selected by placing TRMPWR on MSTR/SLV and enabling the 1.3V regulator. The master is the only terminator connected directly to the DIFFSENS bus line. All the other terminators receive a mode signal by connecting the DIFFB pins together.

The balancing capacitor is very important during high speed operation. The typical capacitor balance between the positive (+) and negative (–) signals is 0.1pF, except in the MWP package where between L8 and L9 the balance is 0.23pF and 0.4pF respecitvely The negative (–) signal line has a higher capacitance than the positive (+) signal line. The FQP package has typically 0.2pF less capacitance than the MWP package, where the typical balance is 0.1pF except for L8 and L3, where the balance is 0.4pF.

Note: The master/slave function will not be included in future Unitrode terminators.

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 10pF Channel Capacitance During Disconnect
- Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- 110 Ohm Termination
- Meets SCSI Hot Plugging

DESCRIPTION

The UC5601 provides precision resistive pull-up to a 2.9V reference for all 18 lines in a Small Computer Systems Interface (SCSI) bus cable. The SCSI-2 standard recommends active termination at both ends of every cable segment utilizing single ended drivers and receivers.

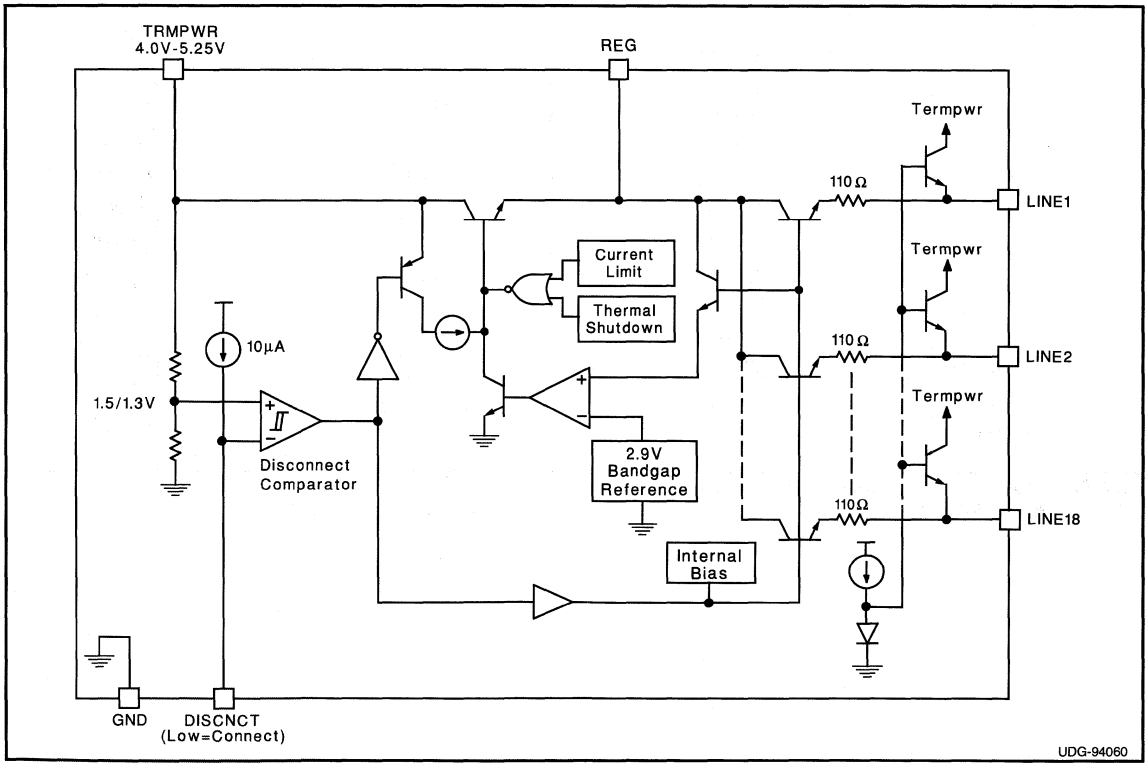
Internal circuit trimming is utilized, first to reduce resistor tolerances to ±3% and then to adjust the regulator's output voltage to insure termination current accuracy of ±3%.

The UC5601 provides a disconnect feature which, upon a logic command, disconnects all terminating resistors, and turns off the regulator; greatly reducing standby power.

Other features include negative clamping on all signal lines, 20mA of active negation sink current capability, regulator current limiting, and thermal shutdown protection.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

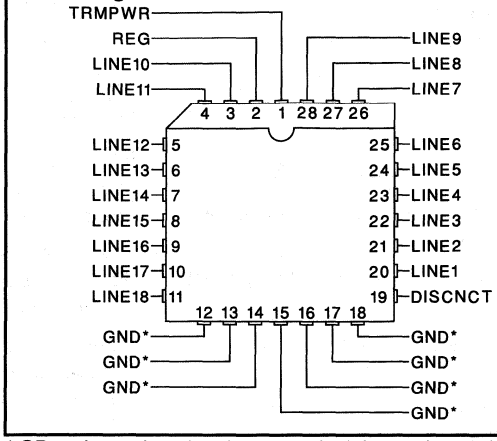
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 4.0V to 5.25V
Signal Line Voltage..... 0V to +3V
Disconnect Input Voltage ..... 0V to Termpwr

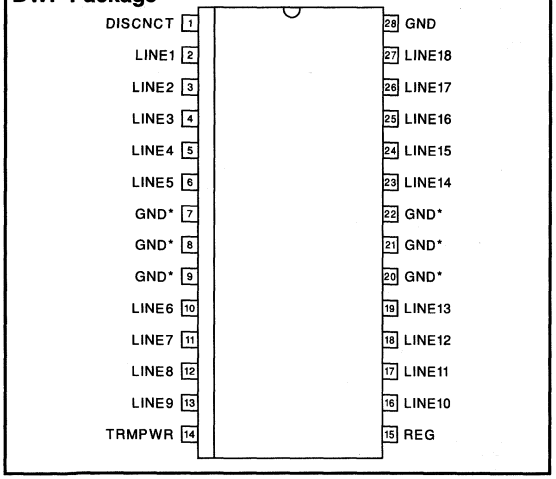
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



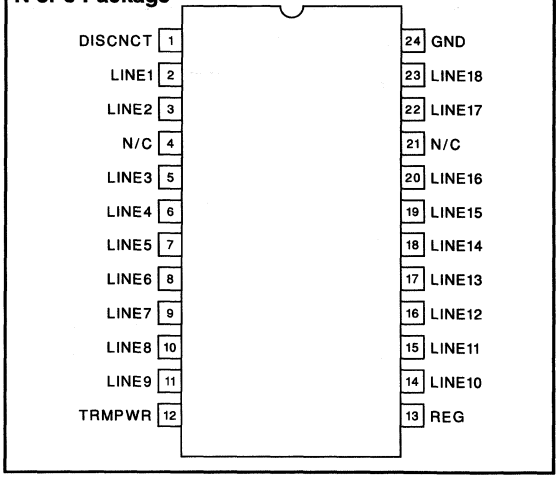
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Termination Impedance	ΔI_{LINE} = -5mA to -15mA			107	110	113	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9		V
Max Output Current	V_{LINE} = 0.5V			-21.1	-21.7	-22.4	mA
	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)			-19.8	-21.7	-22.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				10	12	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3.0	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = 0 to -400mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-850	mA
Current Sink Capability	V_{REG} = 3.5V			8	20	25	mA
Thermal Shutdown					170		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV
Input Current	DISCNCT = 0V				10	15	µA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

THERMAL DATA

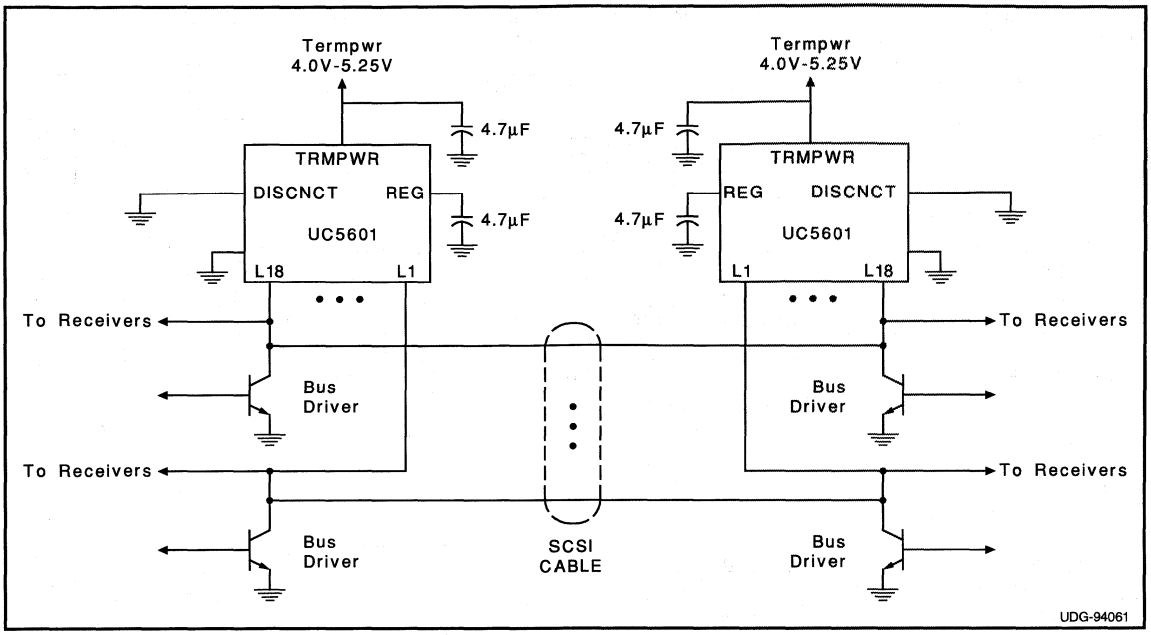
QP package: (see packaging section of UICC data book for more details on thermal performance)
- Thermal Resistance Junction to Leads, θjL ..... 15°C/W
- Thermal Resistance Junction to Ambient, θja ..... 30°-40°C/W

DWP package:
- Thermal Resistance Junction to Leads, θjL ..... 18°C/W
- Thermal Resistance Junction to Ambient, θja ..... 33°-43°C/W

J package:
- Thermal Resistance Junction to Leads, θjL ..... 40°C/W
- Thermal Resistance Junction to Ambient, θja ..... 75°-85°C/W

N package:
- Thermal Resistance Junction to Leads, θjL ..... 50°C/W
- Thermal Resistance Junction to Ambient, θja ..... 95°-105°C/W

Note: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.



Typical SCSI Bus Configuration Using the UC5601

A Look at the Response of a SCSI-2 Cable

Figure 1 shows a single line of a SCSI cable. The driver is an open colletor type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage V_{STEP} is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL} = Driver Output Low Voltage
I_O = Current from Receiving Terminator
Z_0 = Cable Characteristic Impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling culd occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5601 is trimmed so that the output current (I_O) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

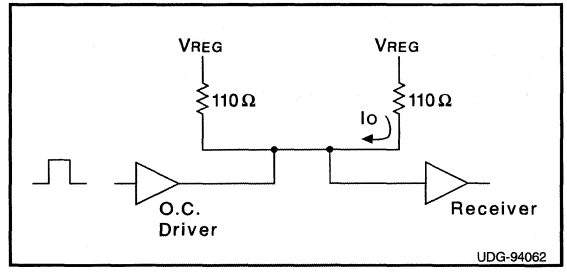


Figure 1. A Single Line of a SCSI Cable

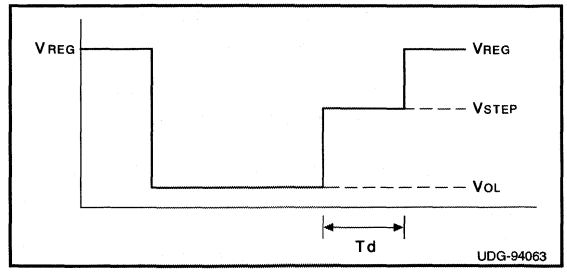


Figure 2. A Typical Response of a SCSI Cable

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UNITRODE

SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 10pF Channel Capacitance During Disconnect
- Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- 110 Ohm Termination
- Meets SCSI Hot Plugging

DESCRIPTION

The UC5602 is a pin compatible version of its predecessor, the UC5601, and is targeted for high volume applications which require active termination, but not the high performance of the UC5601. The major differences are relaxed output current and termination tolerances, and the absence of low side clamps.

The UC5602 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI-2 standard recommends active termination at both ends of the cable segment, and SCSI-3 will make it a requirement.

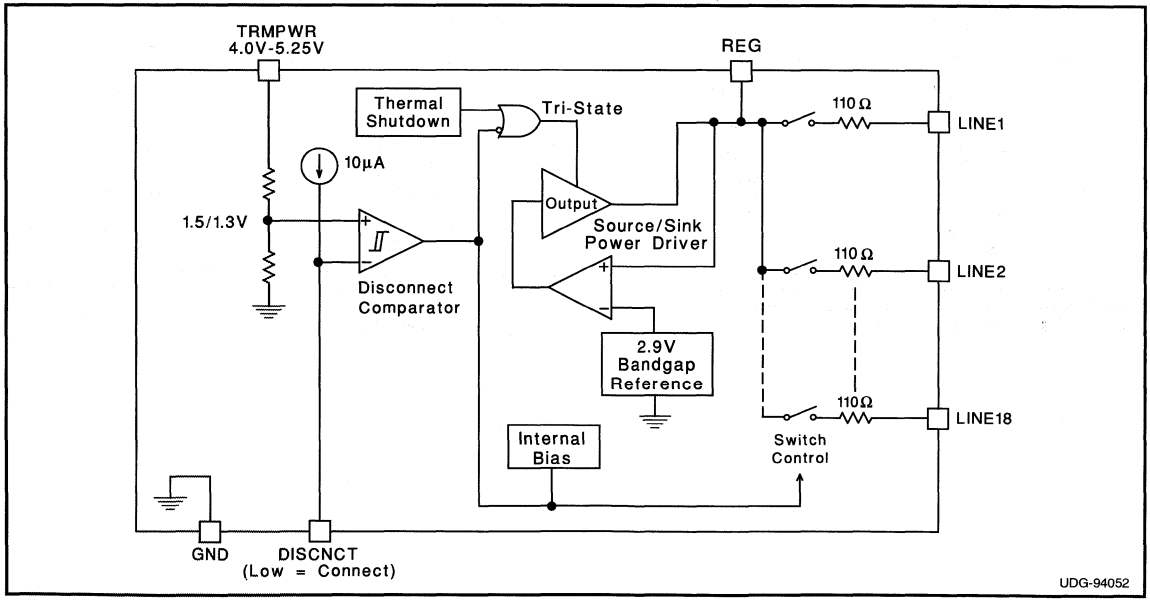
The UC5602 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance; and then most importantly, to trim the output current 7% tolerance, as close to the max SCSI as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown, current limit, and 40mA of active negation sink current capability.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

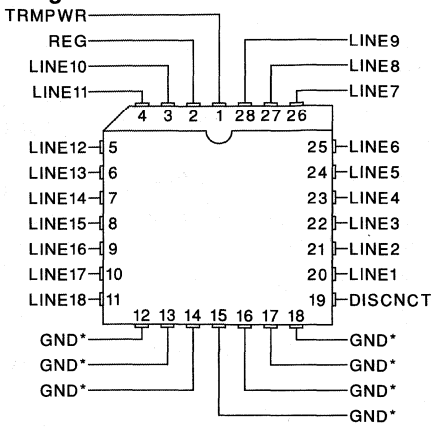
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 4.0V to 5.25V
Signal Line Voltage..... 0V to +3V
Disconnect Input Voltage ..... 0V to Termpwr

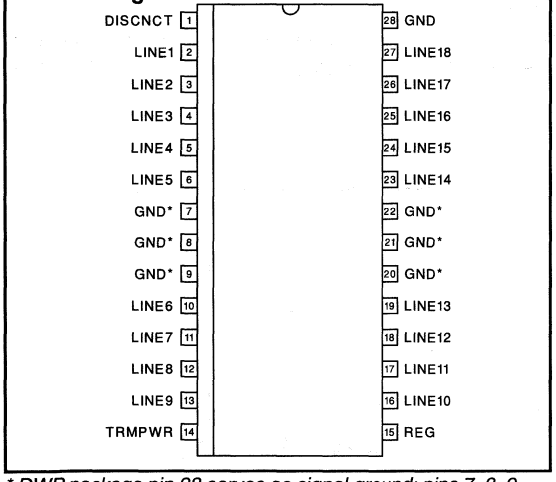
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



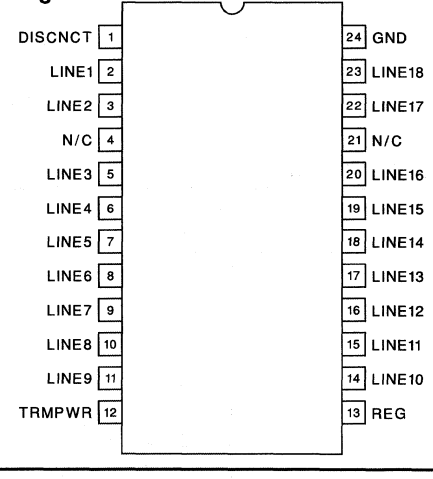
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				20	29	mA
	All termination lines = 0.5V				400	435	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Termination Impedance	ΔI_{LINE} = -5mA to -15mA		T_J = 25°C	102	110	118	Ω
			0°C < T_J < 70°C	97		129	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)		T_J = 25°C	2.6	2.9	3.1	V
			0°C < T_J < 70°C	2.55		3.2	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-19.5	-21.4	-22.4	mA
			0°C < T_J < 70°C	-18.5		-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-18.0	-21.5	-22.4	mA
			0°C < T_J < 70°C	-17.0		-22.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V, REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open, V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				10	13	pF
Regulator Section							
Regulator Output Voltage			T_J = 25°C	2.7	2.9	3.1	V
			0°C < T_J < 70°C	2.55		3.2	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = 0 to -400mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-850	mA
Sinking Current Capability	V_{REG} = 3.5V			20	40		mA
Thermal Shutdown					170		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V
Threshold Hysteresis					100		mV
Input Current	DISCNCT = 0V				150	200	µA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

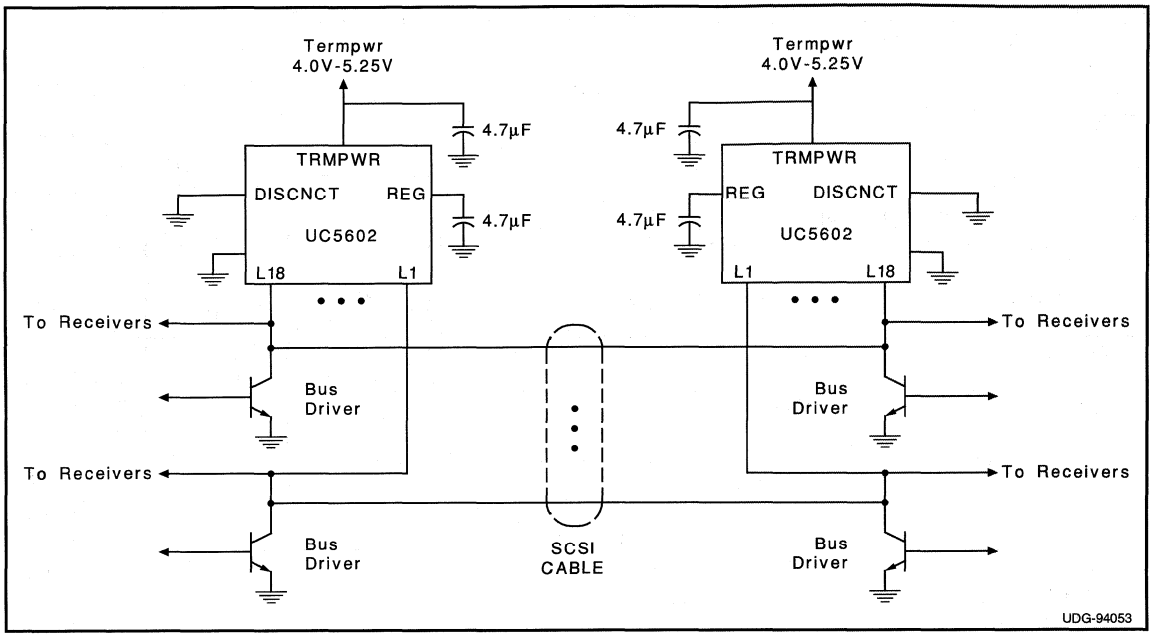
THERMAL DATA

DWP package: (see packaging section of UICC data book for more details on thermal performance)
- Thermal Resistance Junction to Leads, θjL ..... 18°C/W
- Thermal Resistance Junction to Ambient, θja ..... 33°-43°C/W

N package:
- Thermal Resistance Junction to Leads, θjL ..... 50°C/W
- Thermal Resistance Junction to Ambient, θja ..... 95°-105°C/W

QP package:
- Thermal Resistance Junction to Leads, θjL ..... 15°C/W
- Thermal Resistance Junction to Ambient, θja ..... 30°-40°C/W

Note: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.



Typical SCSI Bus Configuration Using the UC5602

A Look at the Response of a SCSI-2 Cable

Figure 1 shows a single line of a SCSI cable. The driver is an open colletor type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage V_{STEP} is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL} = Driver Output Low Voltage
I_O = Current from Receiving Terminator
Z_0 = Cable Characteristic Impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling could occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5602 is trimmed so that the output current (I_O) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

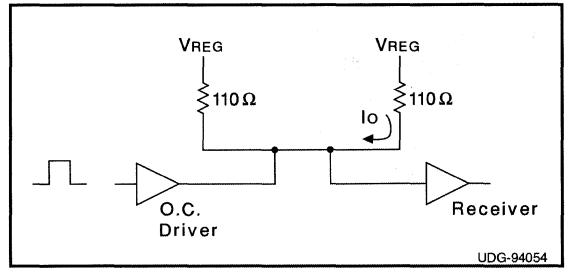


Figure 1. A Single Line of a SCSI Cable

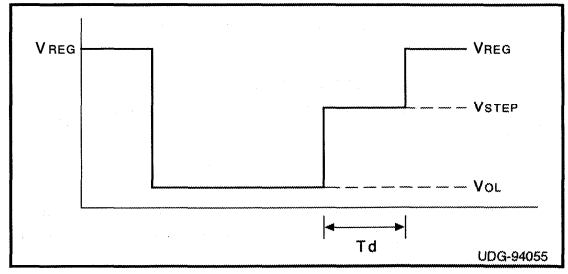
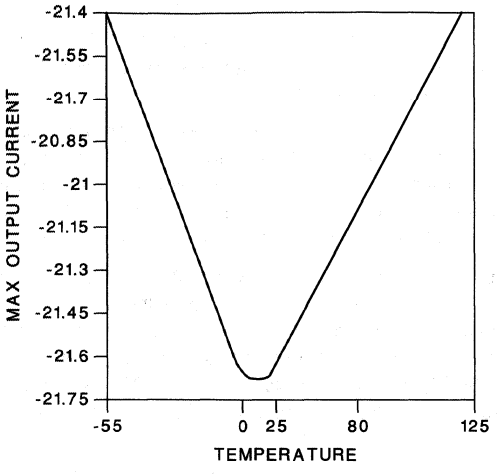
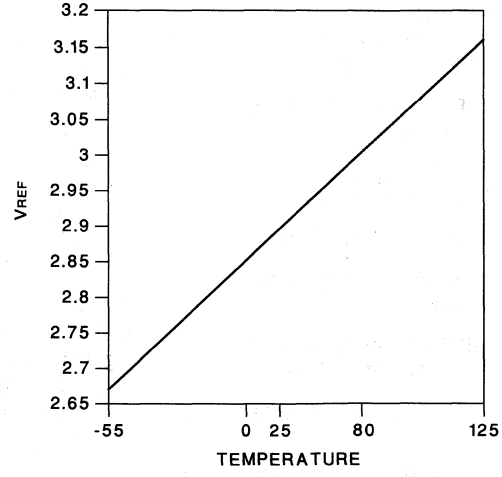


Figure 2. A Typical Response of a SCSI Cable

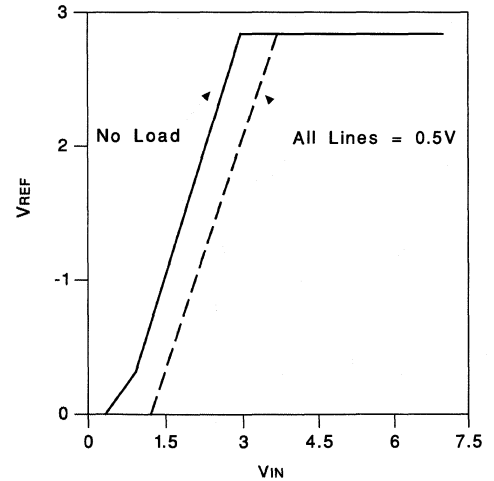
Max Output Current vs. Temperature



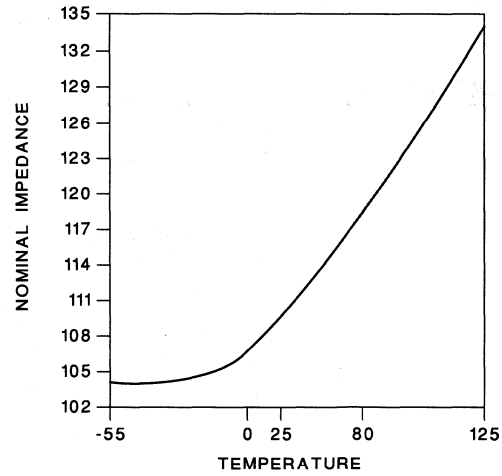
VREF vs. Temperature



VREF vs. VIN



Output Impedance vs. Temperature



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UNITRODE

9-Line SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 3%
- Trimmed Impedance to 3%
- Negative Clamping on all Signal Lines
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5603 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5603 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 6pF allows units at interim points of the bus to have little to no effect on the signal integrity.

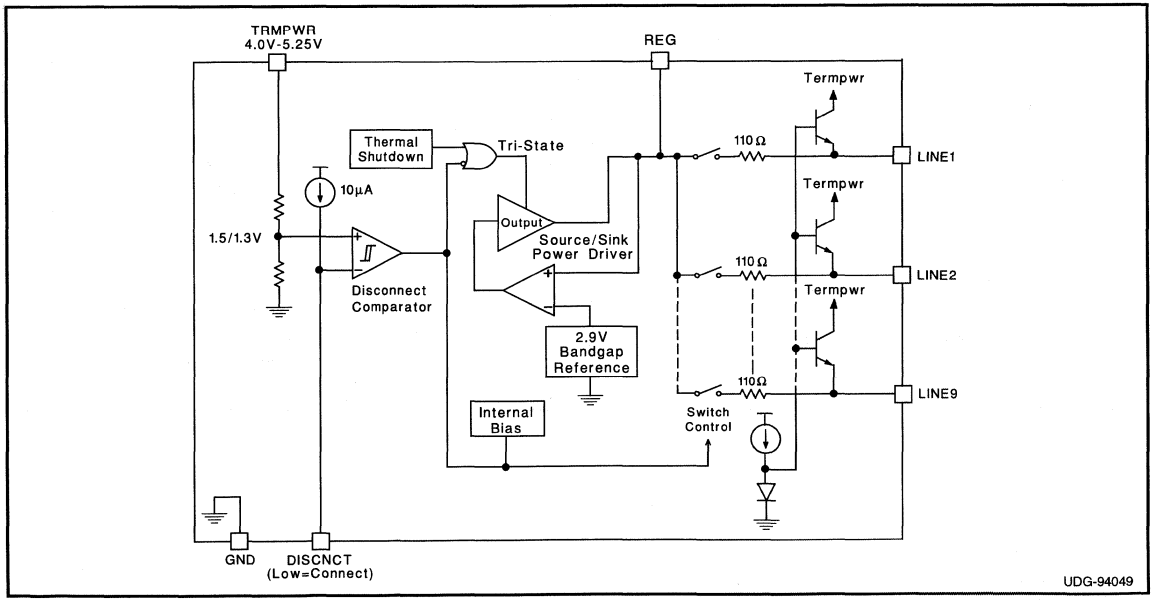
Functionally the UC5603 is similar to its predecessor, the UC5601 - 18 line Active Terminator. Several electrical enhancements were incorporated in the UC5603, such as a sink/source regulator output stage to accommodate all signal lines at +5V, while the regulator remains at its nominal value, reduced channel capacitance to 6pF typical, and as with the UC5601, custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 3% tolerance, and then most importantly, to trim the output current to a 3% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include negative clamping on all signal lines to protect external circuitry from latch-up, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

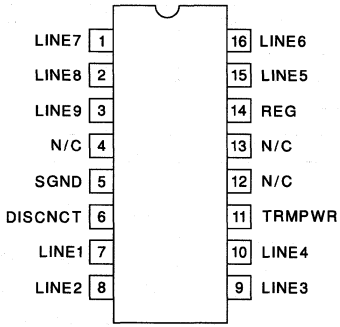
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

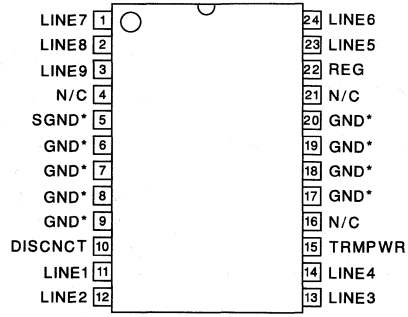
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

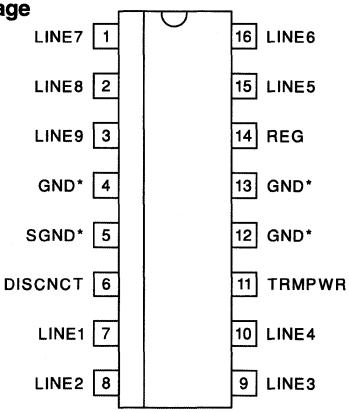


TSSOP-24 (Top View)
PWP Package



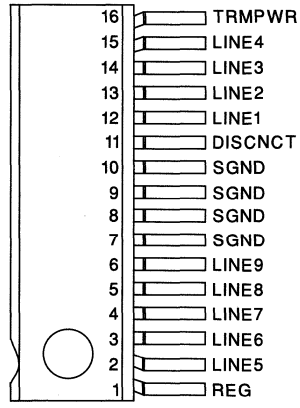
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A= 0°C to 70°C. TRMPWR = 4.75V DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				12	18	mA
	All termination lines = 0.5V				200	220	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			107	110	113	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.7	2.9		V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-21.1	-21.9	-22.4	mA
			0°C < T_J < 70°C	-20.5	-21.9	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-20.3	-21.9	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.9	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4.0V to 5.25V		0°C < T_J < 70°C	–22.0	–24.0	–25.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)				6	8	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 5V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				0.7	1	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			200	400	600	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

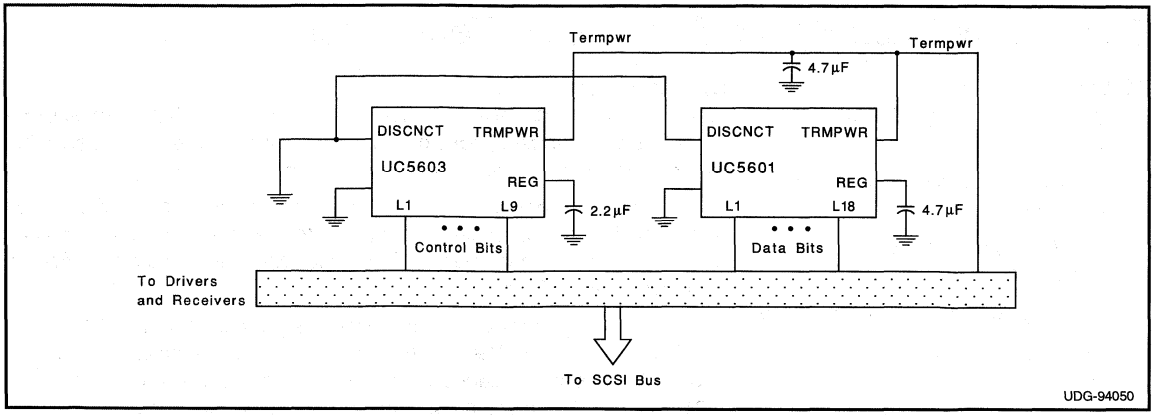


Figure 1: Typical Wide SCSI Bus Configurations Utilizing 1 UC5601 and 1 UC5603 Device

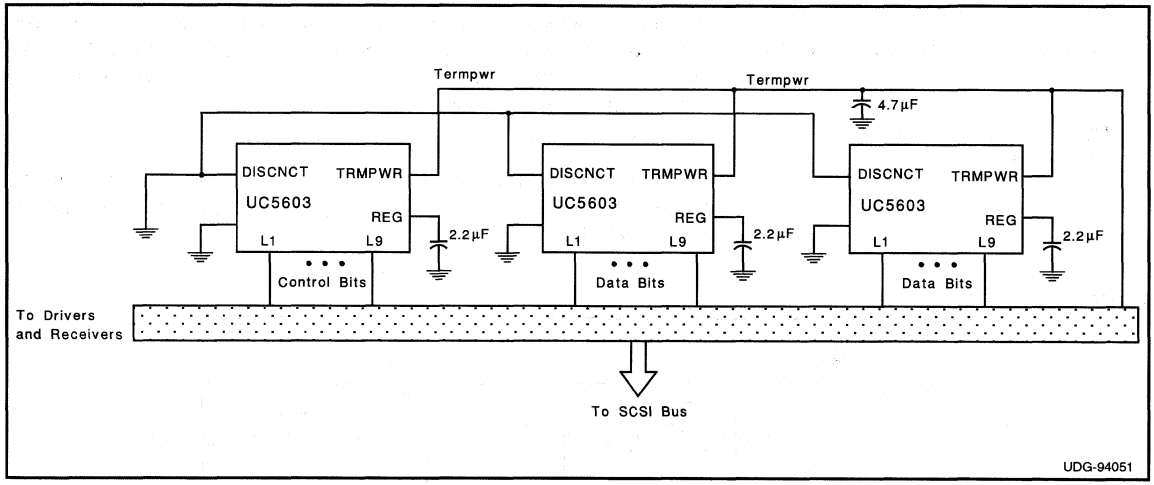


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5603 Devices.

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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 9pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –300mA Sourcing Current for Termination
- +40mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 7%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5604 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5604 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

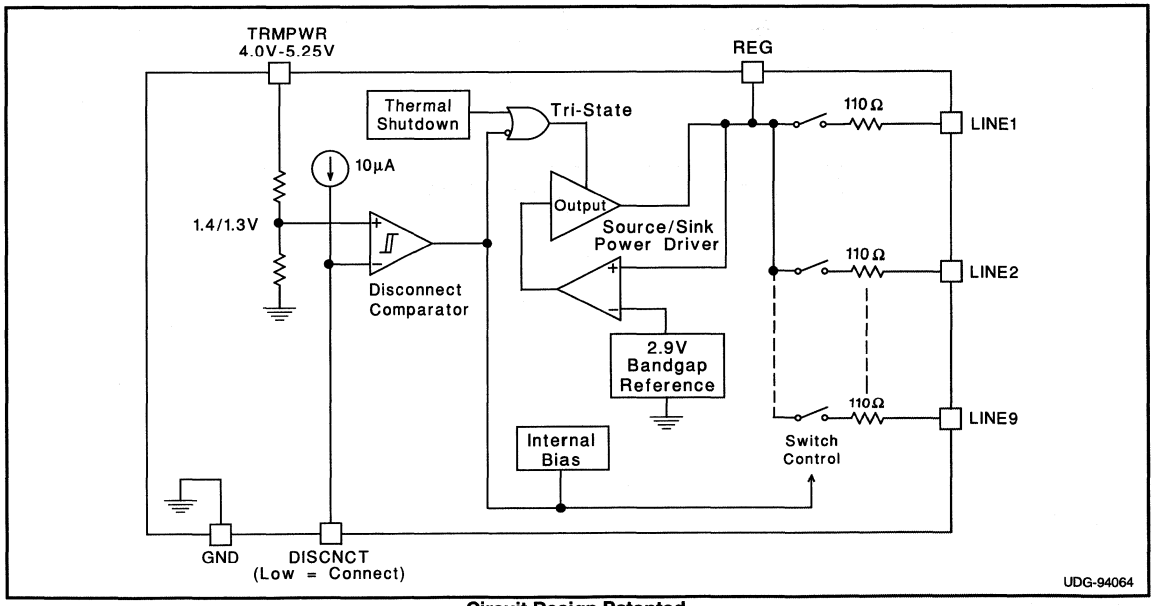
The UC5604 is pin-for-pin compatible with its predecessor, the UC5603 - 9 line Active Terminator. The only functional difference between the UC5604 and UC5603 is the absence of the negative clamps. Parametrically, the UC5604 has a 7% tolerance on impedance and current compared to a 3% tolerance on the UC5603 and the sink current is reduced from 300mA to 40mA. Custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance, and then most importantly, to trim the output current to a 7% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

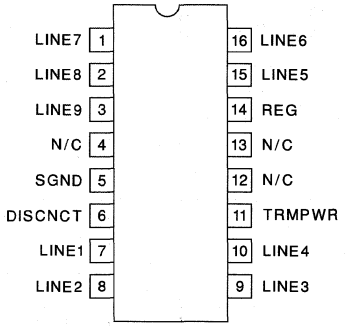
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

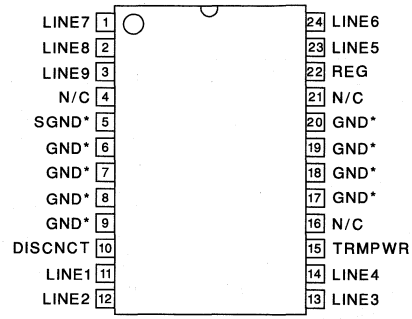
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

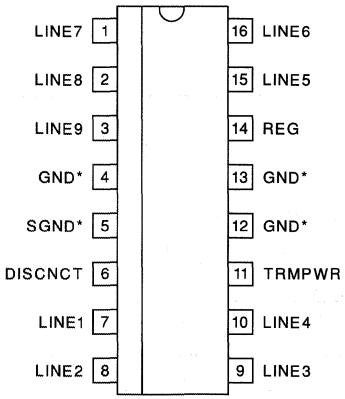


TSSOP-24 (Top View)
PWP Package



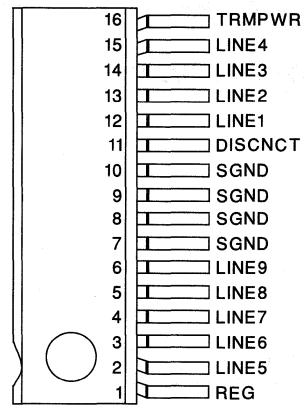
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				14	20	mA
	All termination lines = 0.5V				200	220	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			97	110	129	Ohms
Output High Voltage	TRMPWR = 4V (Note 1)		0°C < T_J < 70°C	2.55		3.2	V
			T_J = 25°C	2.6	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-19.5	-21.9	-22.4	mA
			0°C < T_J < 70°C	-18.5	-21.9	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-18.0	-21.9	-22.4	mA
			0°C < T_J < 70°C	-17.0	-21.9	-22.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				9	12	pF
Regulator Section							
Regulator Output Voltage				2.5	2.9	3.2	V
Regulator Output Voltage	All Termination Lines = 5V			2.55	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			20	40		mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V
Threshold Hysteresis					100		mV
Input Current	DISCNCT = 0V				150	200	µA

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

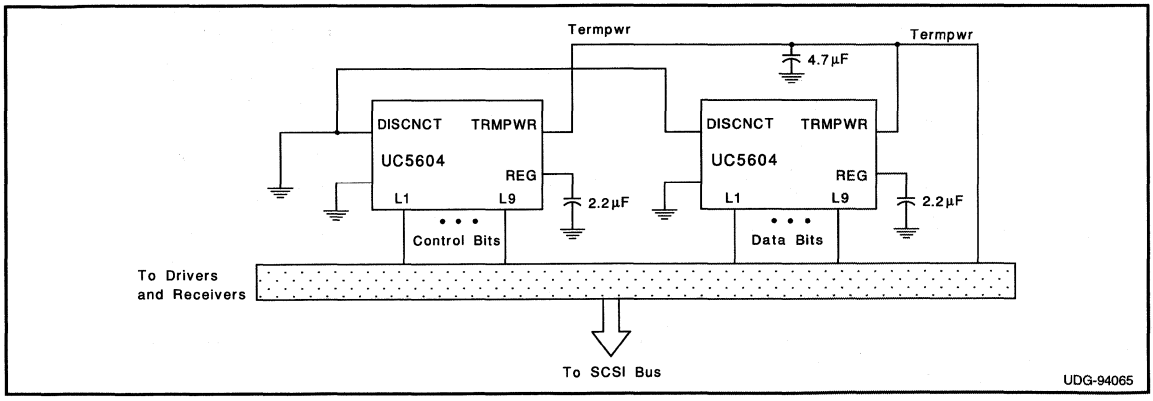


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5604 Devices

APPLICATION INFORMATION (cont.)

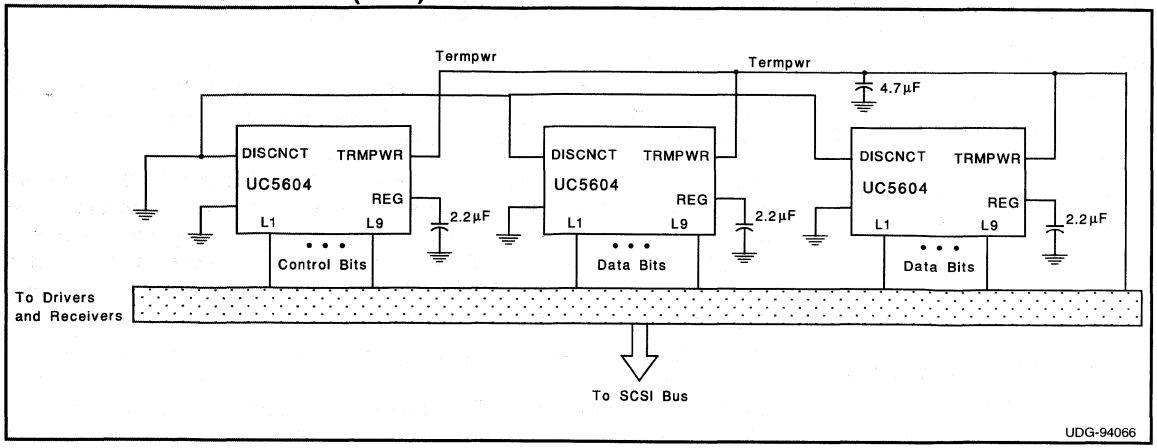


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5604 Devices.

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9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Reverse Disconnect
- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 5pF Channel Capacitance during Disconnect
- Hot Plugging Capability
- –400mA Sourcing Current for Termination
- +100mA Sinking Current for Active Negation
- 1V Dropout Voltage Regulator
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5605 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

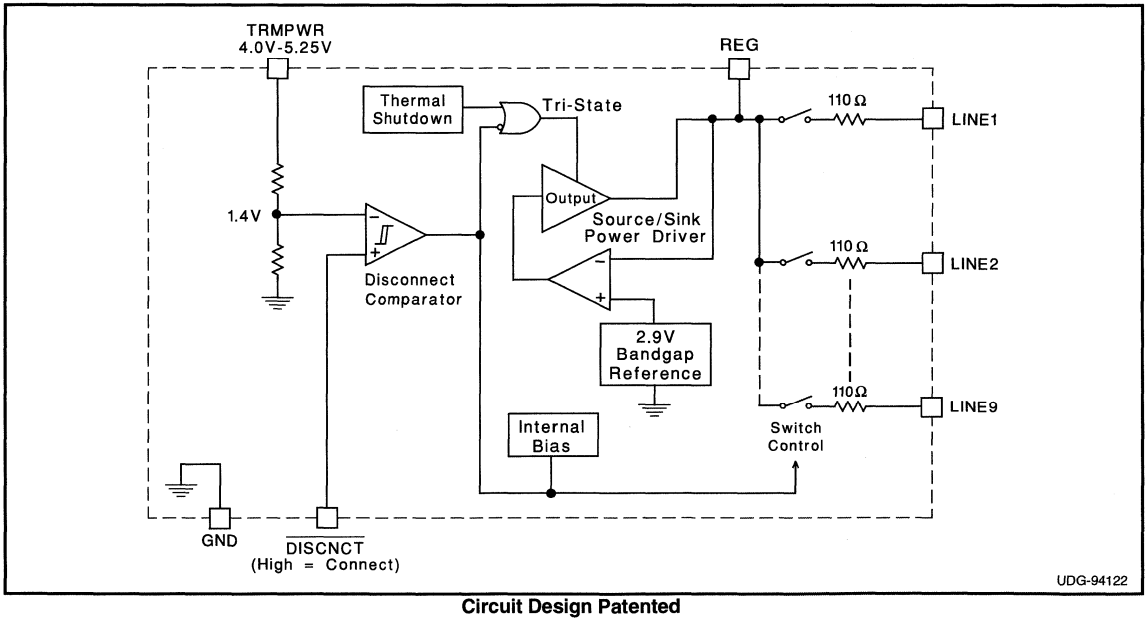
The only functional differences between the UC5603 and UC5605 is the absence of the negative clamps on the output lines and the disconnect input must be at a logic-low for the terminating resistors to be disconnected. Parametrically, the UC5605 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (2 Watts).

The UC5605 provides a disconnect feature which, when driven low, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 5pF allows interim points of the bus to have little to no effect on the signal integrity.

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.6A
Storage Temperature..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

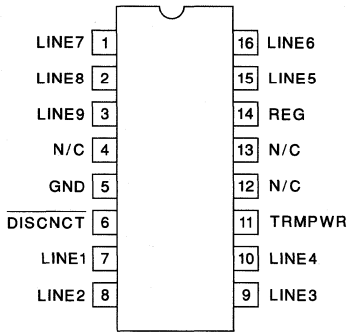
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

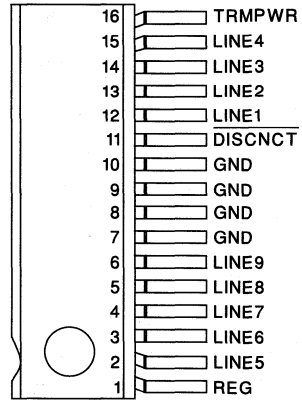
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

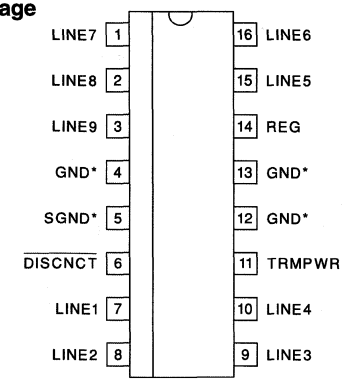
DIL-16 (Top View)
N or J Package



ZIP-16 (Top View)
Z Package

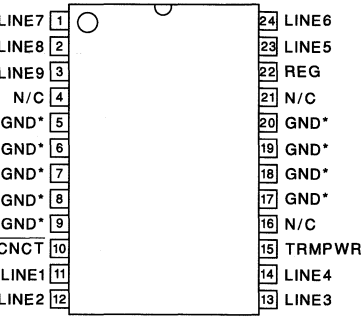


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package



** PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{DISCNCT}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	$\overline{DISCNCT}$ = 0V				100	150	µA
Output Section (Termination Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	TRMPWR = 4V			2.65	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4.0V to 5.25V		0°C < T_J < 70°C	–21.6	–24.0	–25.4	mA
Output Leakage	$\overline{DISCNCT}$ = 0V TRMPWR = 0V to 5.25V	REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		REG = Open	V_{LINE} = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 0V (Note 2) (DP Package)				5	6	pF
Regulator Section							
Regulator Output Voltage				2.7	2.9	3.1	V
	All Termination Lines = 4V			2.7	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	REG = 0V			-200	-400	-600	mA
Sinking Current Capability	REG = 3.5V			75	100	400	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 8 are low.
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

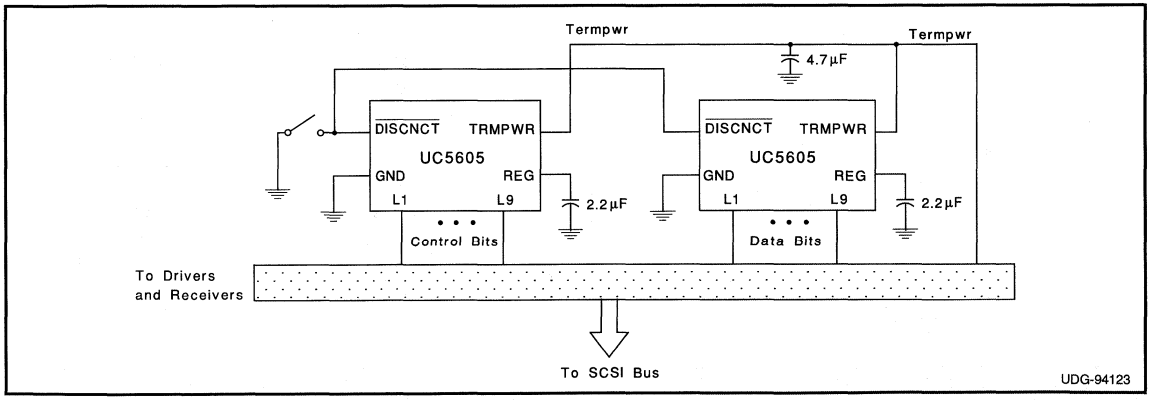


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5605 Devices

APPLICATION INFORMATION (cont.)

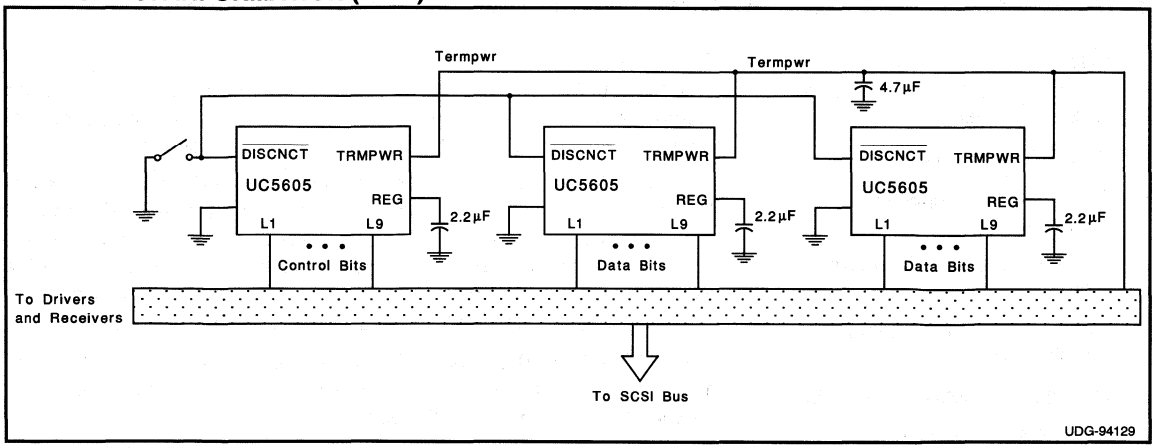


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5605 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

9-Line 3-5 Volt SCSI Active Terminator, Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2 and SCSI-3 Standards
- 2.7V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 1μA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5606 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

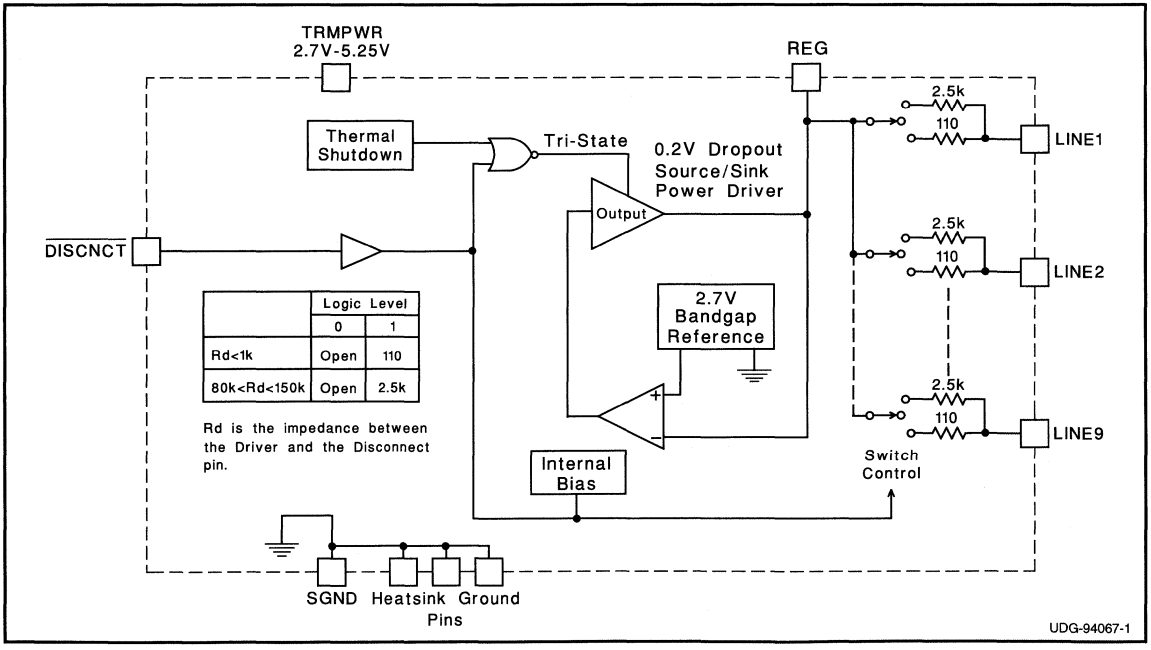
The UCC5606 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.7V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 1μA, which makes the IC attractive for battery powered systems.

The UCC5606 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5606 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible $\overline{\text{DISCNCT}}$ pin directly, the 110 ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when low. When the $\overline{\text{DISCNCT}}$ pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when driven low.

continued

BLOCK DIAGRAM



	Logic Level	
	0	1
Rd<1k	Open	110
80k<Rd<150k	Open	2.5k

Rd is the impedance between the Driver and the Disconnect pin.

Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5606 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5606 is pin for pin compatible with Unitrode's other 9 line SCSI terminators, except that $\overline{\text{DISCNCT}}$ is now active low, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5606, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (Zig-Zag In Line package), 24 pin TSSOP and 28 pin PLCC.

3

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.6A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

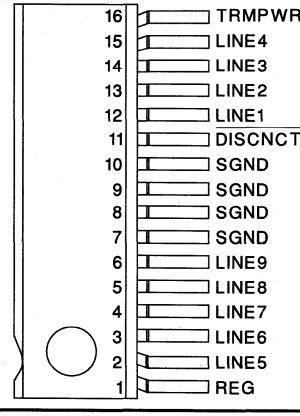
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

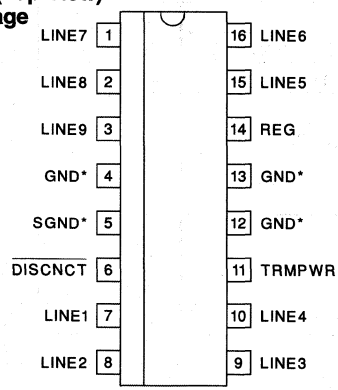
Termpwr Voltage ..... 2.7V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

ZIP-16 (Top View)
Z Package

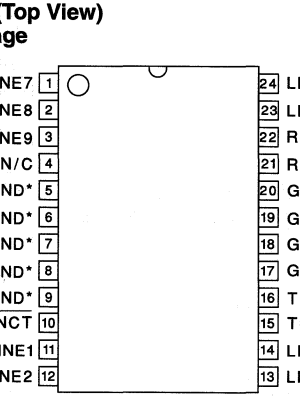


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package

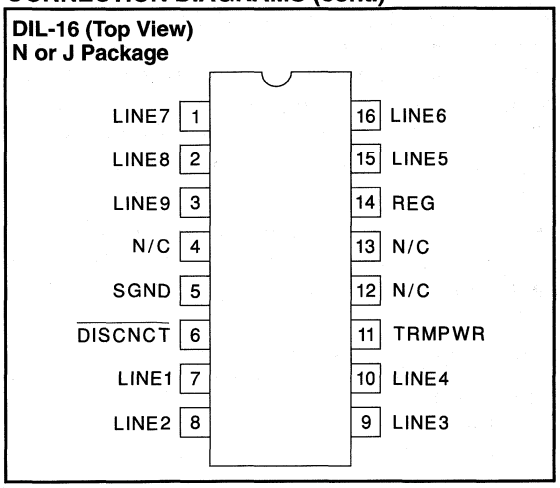


** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

CONNECTION DIAGRAMS (cont.)

DIL-16 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, $\overline{\text{DISCNCT}}$ = 3.3V, $R_{DISCNCT}$ = 0 ohms. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	218	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance		102.3	110	117.7	Ohms
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V, T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V, DP Package (Note 2)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V, DP Package (Note 2)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A=0°C to 70°C. TRMPWR = 3.3V, $\overline{DISCNCT}$ = 3.3V, $R_{DISCNCT}$ = 0 ohms. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (cont.)					
Short Circuit Current	V_{REG} = 0V	–200	–400	–800	mA
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	$\overline{DISCNCT}$ = 3.3V		30	50	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

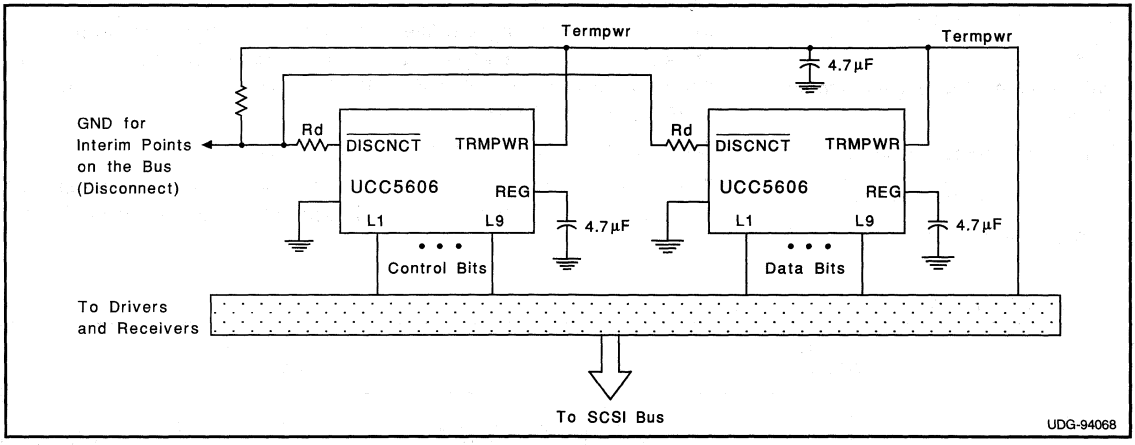


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UCC5606 Devices

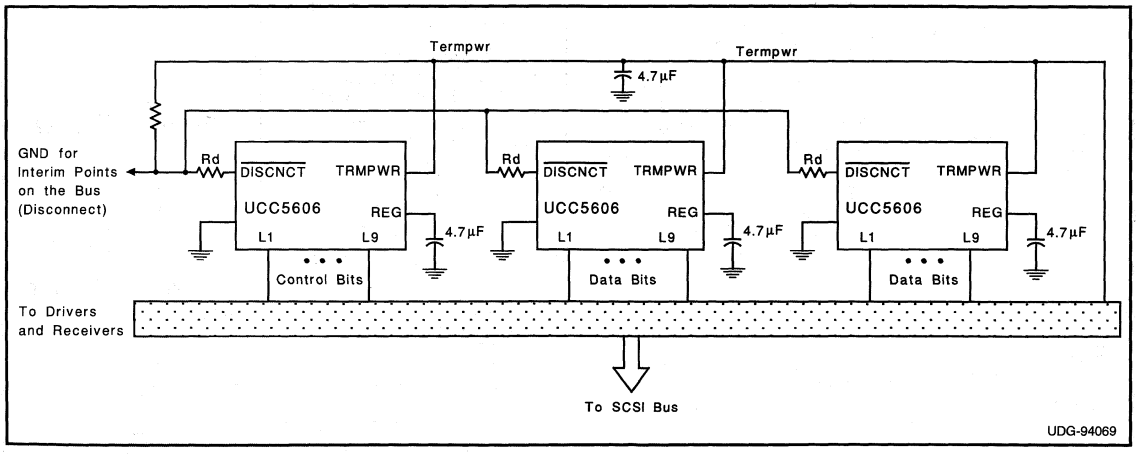


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UCC5606 Devices.

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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Plug and Play, 18-Line SCSI Active Terminator

FEATURES

- Complies with SCSI and SCSI-2 Standards
- 8pF Channel Capacitance during Disconnect
- SCSI Plug and Play, Dual Low Disconnect, Logic Low Command Disconnects All Termination Lines
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- 200µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 7%
- Trimmed Impedance to 7%
- Provides Active Termination for 18 Lines

DESCRIPTION

The UC5607 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5607 provides a low disconnect feature which will disconnect all terminating resistors, and will disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

The UC5607 terminator is specially designed with two disconnect pins for full SCSI Plug and Play (PnP) applications.

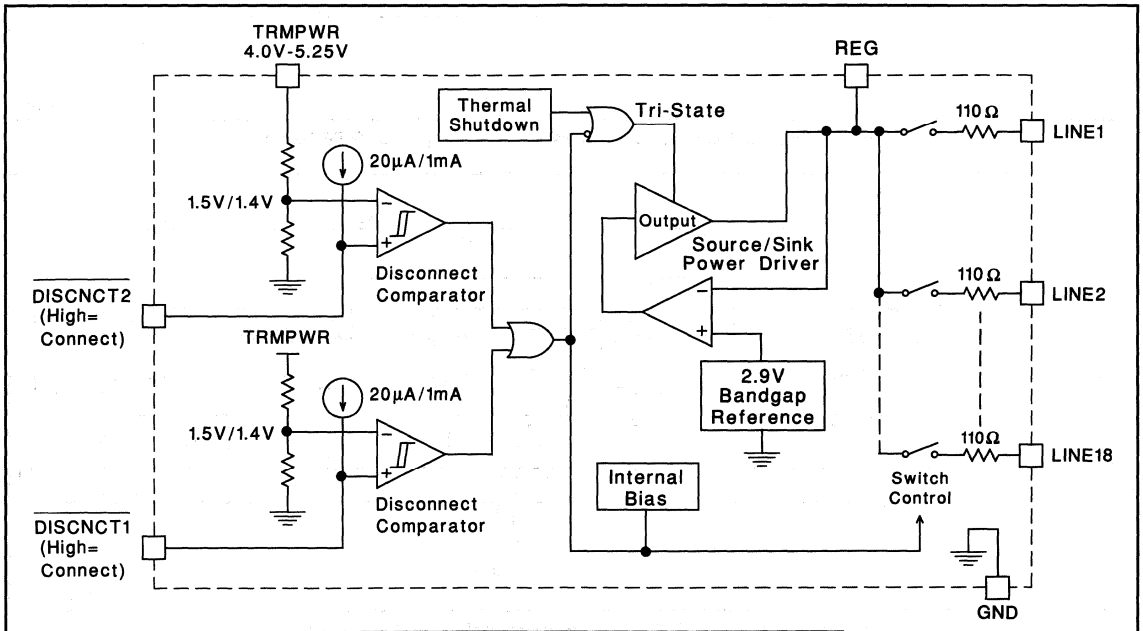
Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance, and then most importantly, to trim the output current to a 7% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



	Connect	Connect	Connect	Disc
$\overline{\text{DISCNCT1}}$	1	0	1	0
$\overline{\text{DISCNCT2}}$	0	1	1	0

UDG-94124

Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

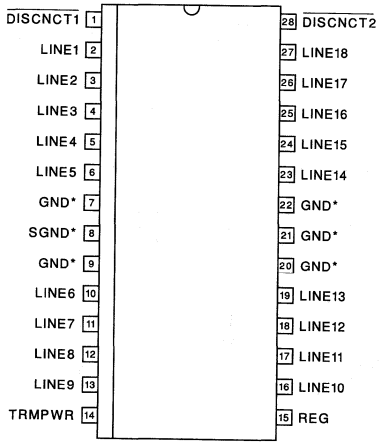
Termpwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage . . . . . 3.8V to 5.25V
Signal Line Voltage . . . . . 0V to +5V
Disconnect Input Voltage . . . . . 0V to Termpwr

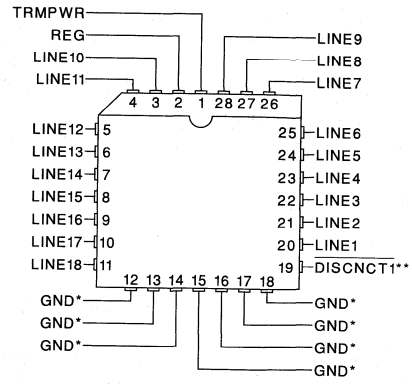
SOIC-28 (Top View)
DWP Package



** DWP package pin 8 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

CONNECTION DIAGRAMS

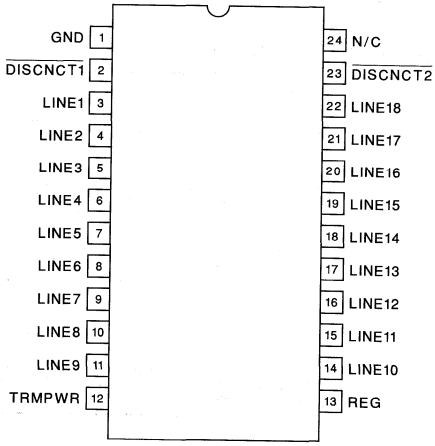
PLCC-28 (Top View)
QP Package



** QP package pins 12 - 18 serve as both heatsink and signal ground.*

*** $\overline{\text{DISCNCT2}}$ is internally tied to ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 2.2V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current Section						
Termpwr Supply Current	All termination lines = Open			30	45	mA
	All termination lines = 0.5V			420	470	mA
Power Down Mode	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V			300	500	µA
Output Section (Terminator Lines)						
Terminator Impedance	ΔI_{LINE} = –5mA to –15mA	T_J = 25°C	102	110	118	Ohms
		0°C < T_J < 70°C	97	110	129	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	T_J = 25°C	2.6	2.9	3.1	V
		0°C < T_J < 70°C	2.55	2.9	3.2	V
Max Output Current	V_{LINE} = 0.5V	T_J = 25°C	–19.5	–21.9	–22.4	mA
		0°C < T_J < 70°C	–18.5	–21.9	–22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)	T_J = 25°C	–18.0	–21.9	–22.4	mA
		0°C < T_J < 70°C	–17.0	–21.9	–22.4	mA
Output Leakage	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V, TRMPWR = 0V to 5.25V			10	400	nA
Output Capacitance	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V (Note 2)			8	10	pF
Regulator Section						
Regulator Output Voltage	All Termination Lines = 5V	TJ = 25°C	2.7	2.9	3.1	V
		0°C < T_J < 70°C	2.55	2.9	3.2	V
Line Regulation	TRMPWR = 4V to 6V			10	20	mV
Load Regulation	I_{REG} = +100mA to –100mA			20	50	mV

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

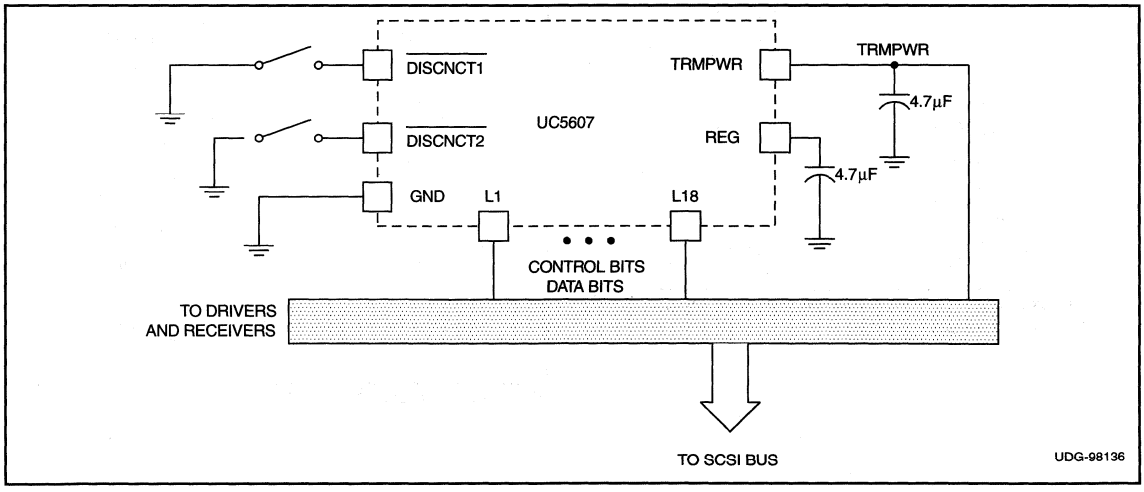


Figure 1: Typical SCSI Bus Configuration Utilizing UC5607 Device

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

18-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- Provides Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5608 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the bus cable.

The UC5608 is pin-for-pin compatible with its predecessors, the UC5601 and UC5602 - 18 Line Active Terminator. Parametrically the UC5608 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5601 and the sink current is increased from 20 to 200mA. The low side clamps have been removed. Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

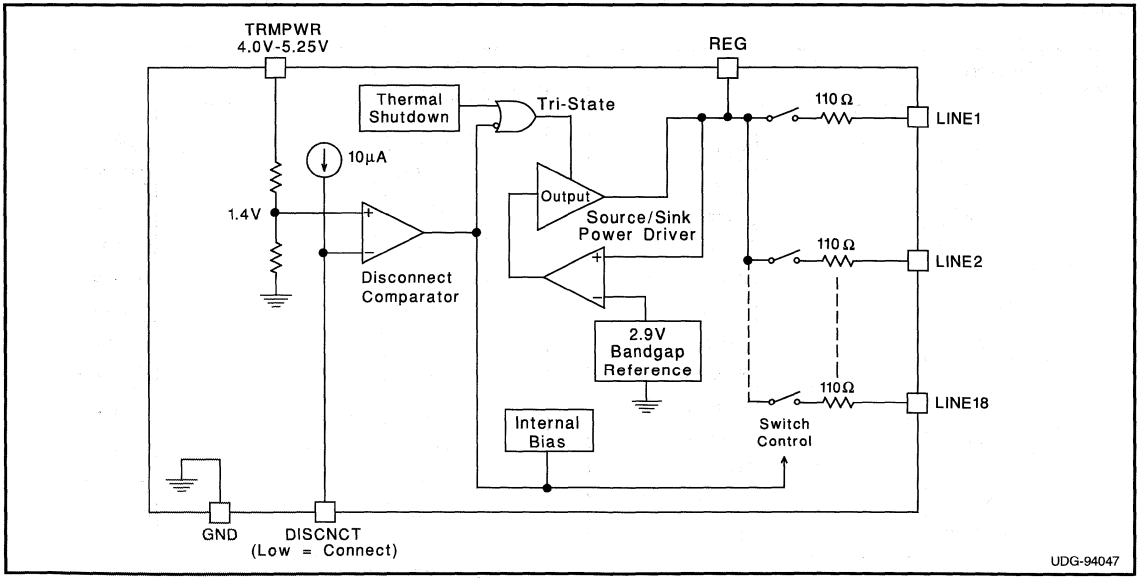
When in disconnect mode the terminator will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized to trim the impedance to a 5% tolerance and, most importantly, to trim the output current to a 5% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include 4.0 to 5.25V Termpwr, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 28 pin wide body TSSOP, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

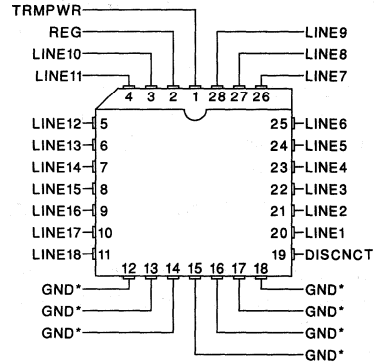
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

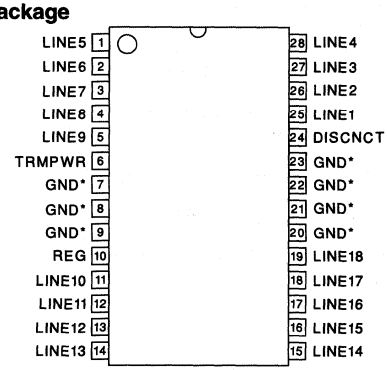
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



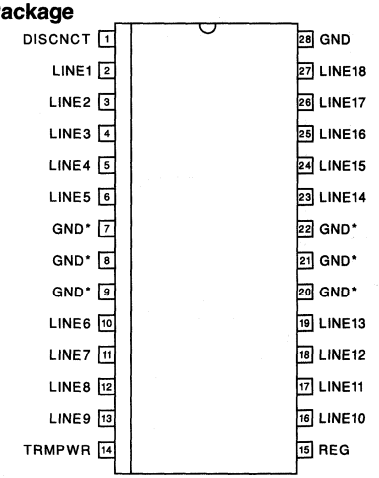
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



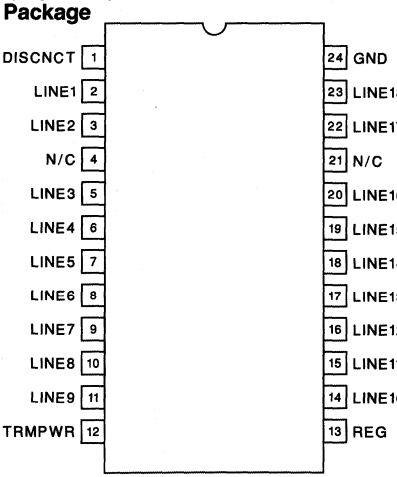
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21 and 22 serve as heatsink/ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = Ground. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9	3.0	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V, REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open, V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				6	7	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 4V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-950	mA
Sinking Current Capability	V_{REG} = 3.5V			100	200	500	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

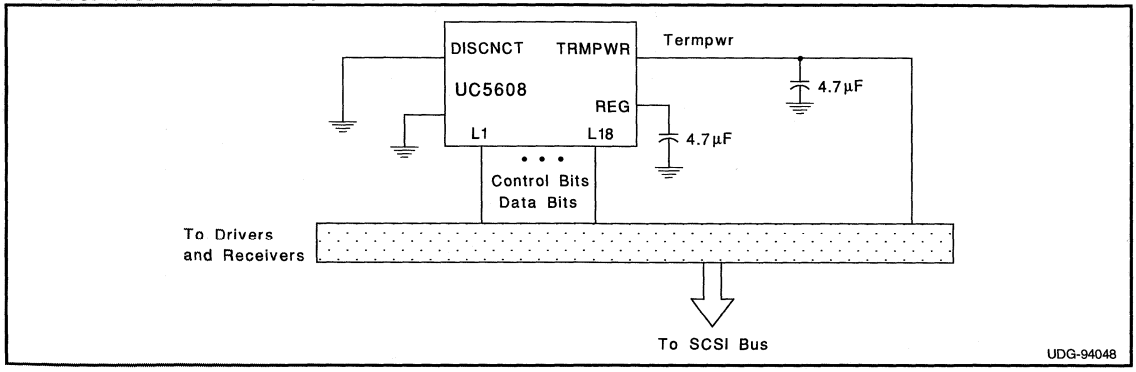


Figure 1: Typical SCSI Bus Configuration

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UNITRODE

18-Line Low Capacitance SCSI Active Terminator

FEATURES

- Reverse Disconnect
- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- Provides Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5609 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the bus cable.

The UC5609 is pin-for-pin compatible with its predecessors, the UC5601, UC5602 and UC5608 - 18 Line Active Terminators, except for the reverse disconnect sense. Parametrically the UC5609 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5601 and the sink current is increased from 20 to 200mA. The low side clamps have been removed. Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

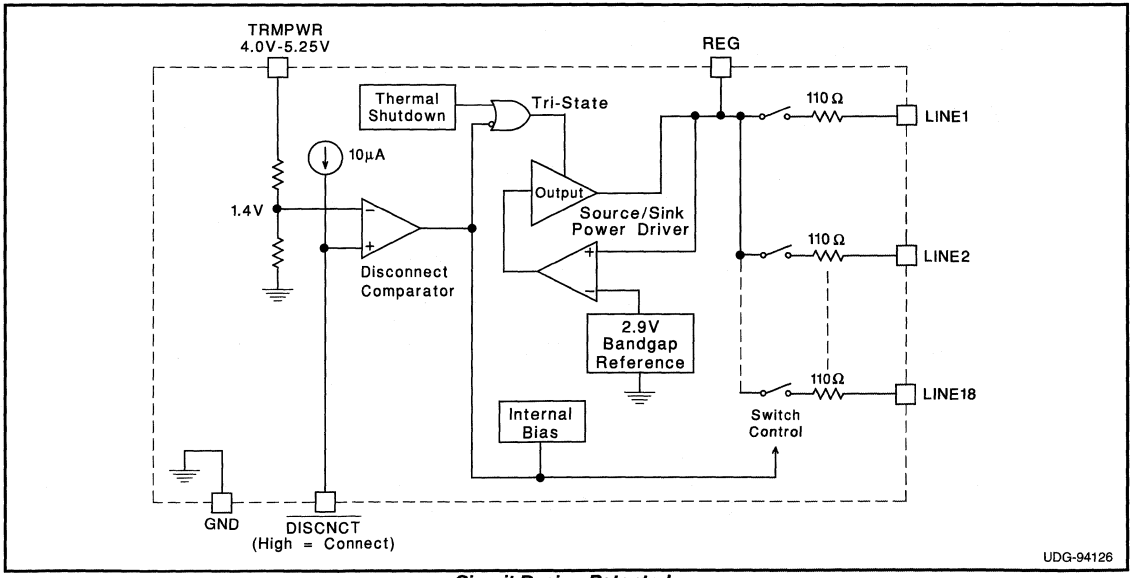
When in disconnect mode the terminator will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized to trim the impedance to a 5% tolerance and, most importantly, to trim the output current to a 5% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include 4.0 to 5.25V Termpwr, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 28 pin wide body TSSOP, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

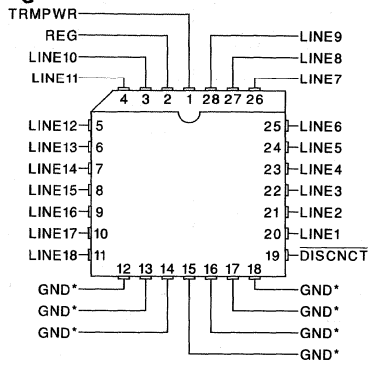
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

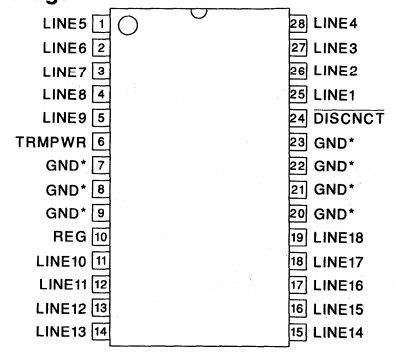
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



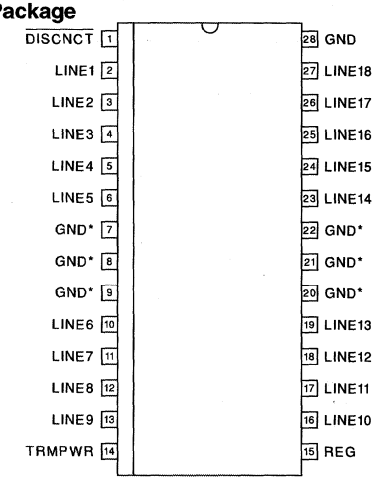
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



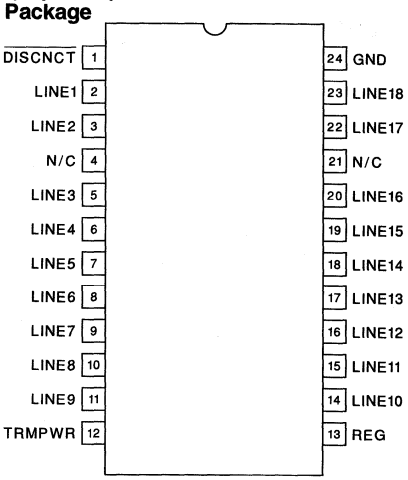
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21 and 22 serve as heatsink/ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{DISCNCT}$ = 2.4V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = GND				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9	3.0	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	$\overline{DISCNCT}$ = GND	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = GND (Note 2)				6	7	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 4V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-950	mA
Sinking Current Capability	V_{REG} = 3.5V			100	200	500	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

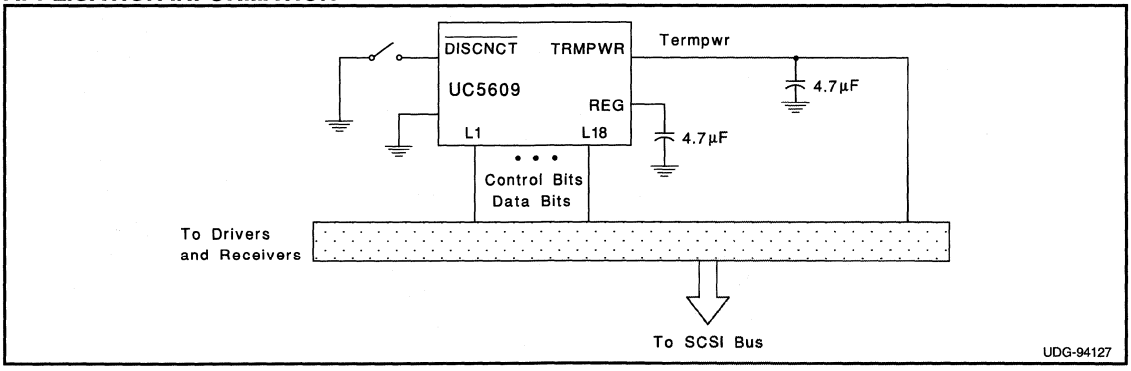


Figure 1: Typical SCSI Bus Configuration

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UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 5pF Channel Capacitance during Disconnect
- Meets SCSI Hot Plugging
- –400mA Sourcing Current for Termination
- +100mA Sinking Current for Active Negation
- 1V Dropout Voltage Regulator
- Logic High Command Disconnects all Termination Lines
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5612 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

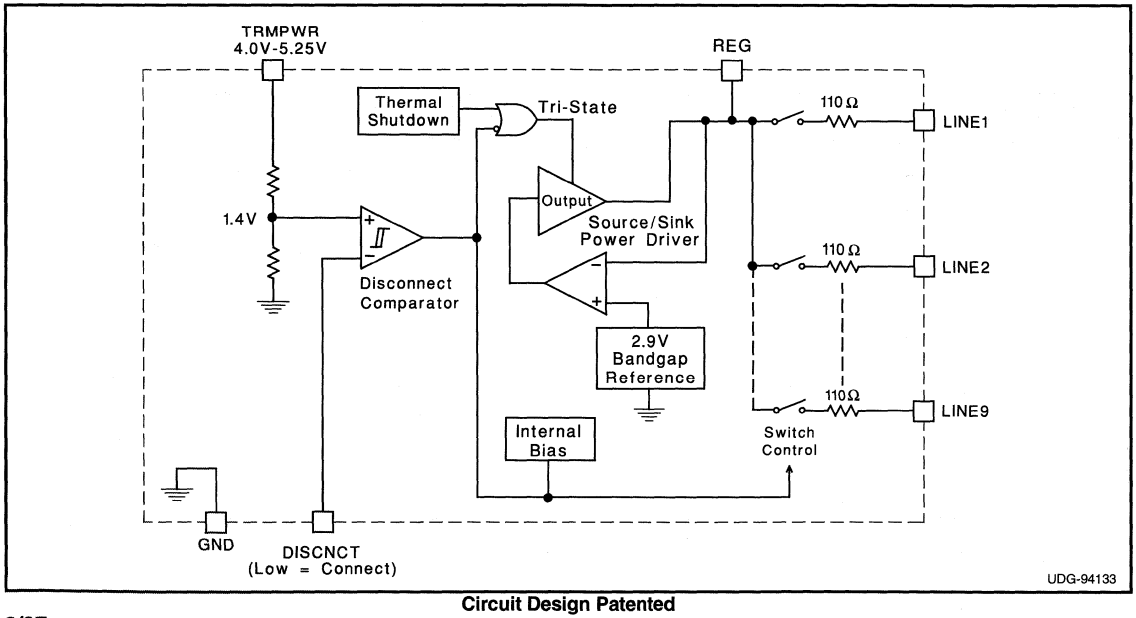
The only functional differences between the UC5603 and UC5612 is the absence of the negative clamps on the output lines. Parametrically, the UC5612 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (2 Watts).

The UC5612 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 5pF allows interim points of the bus to have little to no effect on the signal integrity.

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.6A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

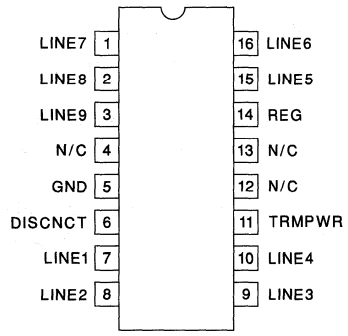
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

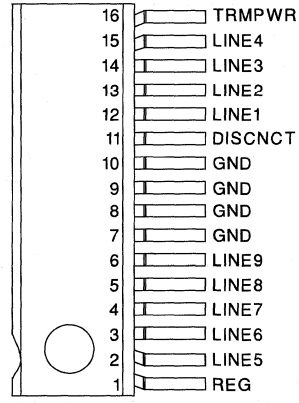
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

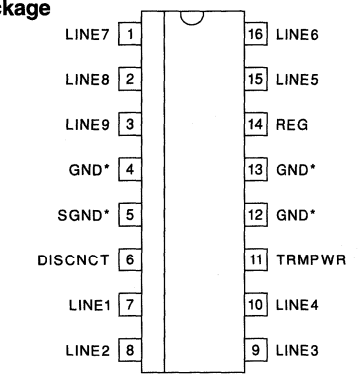
DIL-16 (Top View)
N or J Package



ZIP-16 (Top View)
Z Package

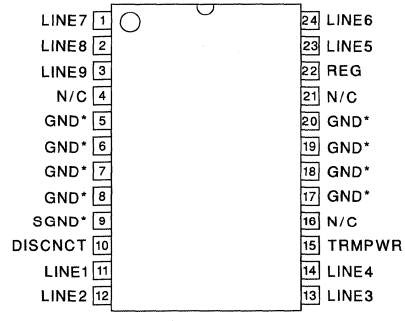


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package



** PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage				2.65	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V TRMPWR = 0V to 5.25V	REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		REG = Open	V_{LINE} = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)				5	6	pF
Regulator Section							
Regulator Output Voltage				2.7	2.9	3.1	V
	All Termination Lines = 4V			2.7	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	REG = 0V			-200	-400	-600	mA
Sinking Current Capability	REG = 3.5V			75	100	400	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 8 are low.
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

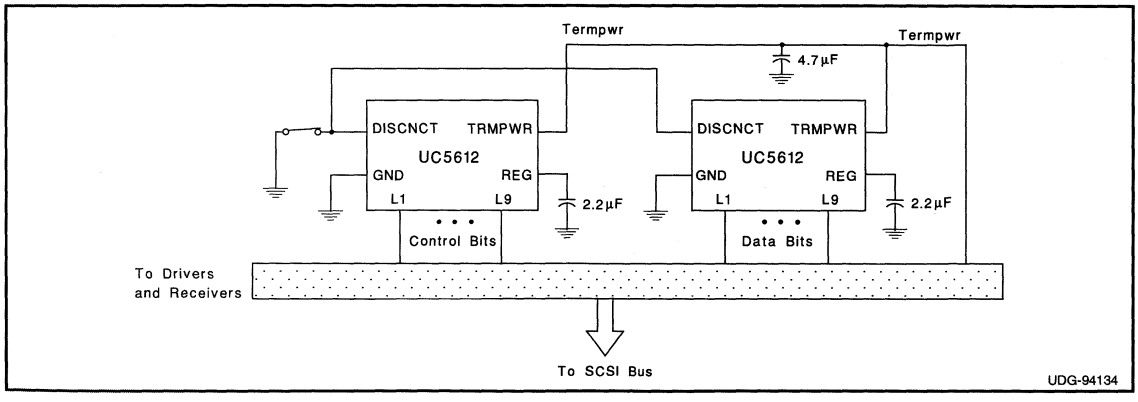


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5612 Devices

APPLICATION INFORMATION (cont.)

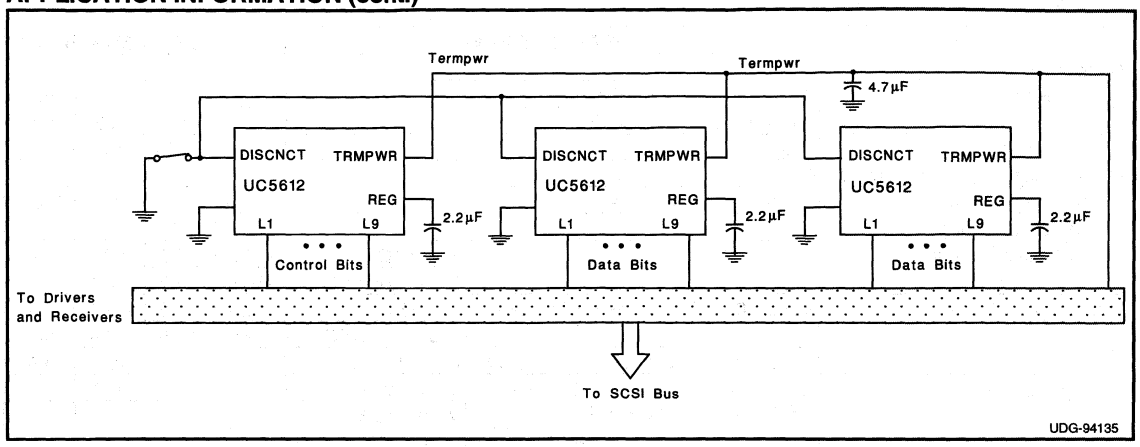


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5612 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 3pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5613 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5613 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors and disables the regulator greatly reducing standby power. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 3pF allows units at interim points of the bus to have little or no effect on the signal integrity.

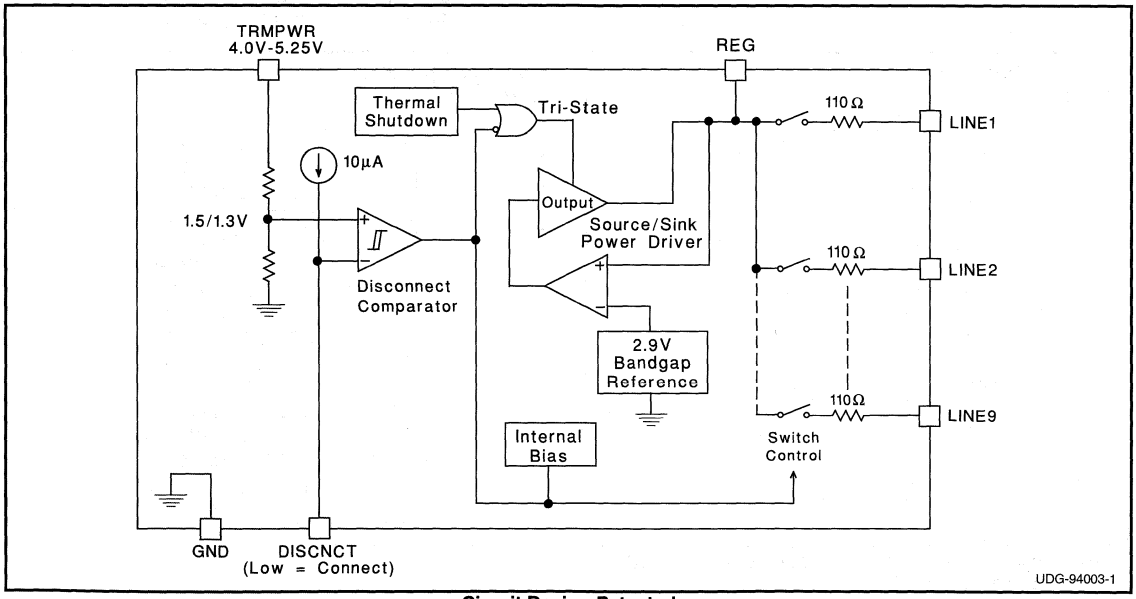
The UC5613 is pin-for-pin compatible with its predecessor, the UC5603 - 9 line Active Terminator. The only functional difference between the UC5613 and UC5603 is the absence of the negative clamps. Parametrically, the UC5613 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance; then, the output current is trimmed to a 5% tolerance. The output current trim is set as close as possible to the maximum value of the SCSI specification which maximizes the noise margin for fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package), and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

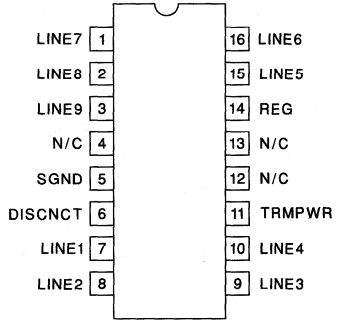
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

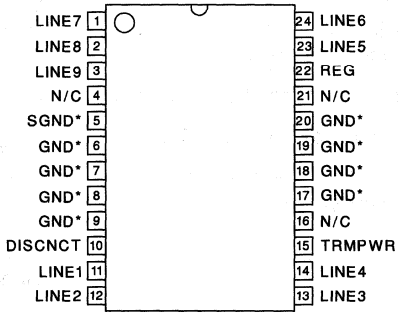
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

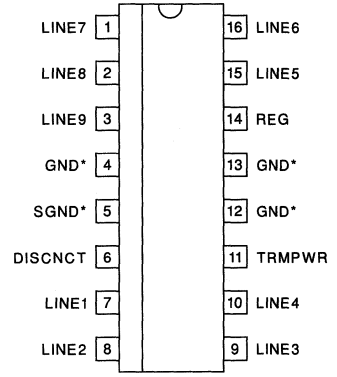


TSSOP-24 (Top View)
PWP Package



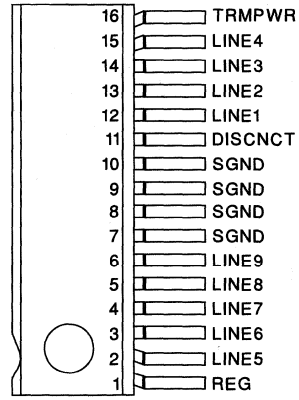
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	TRMPWR = 4V (Note 1)			2.7	2.9		V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V, REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open, V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open, DP Package (Note 2)				3	4.5	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 5V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				0.7	1	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			200	400	600	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

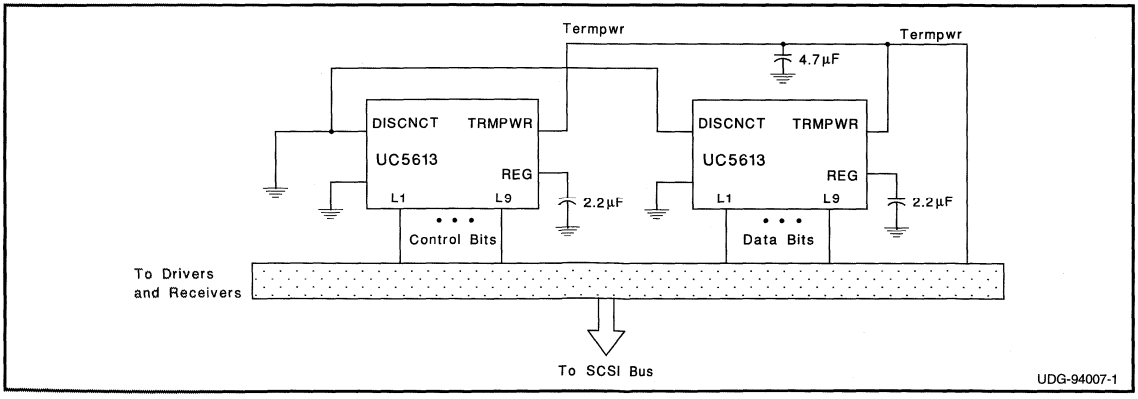


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5613 Devices

APPLICATION INFORMATION (cont.)

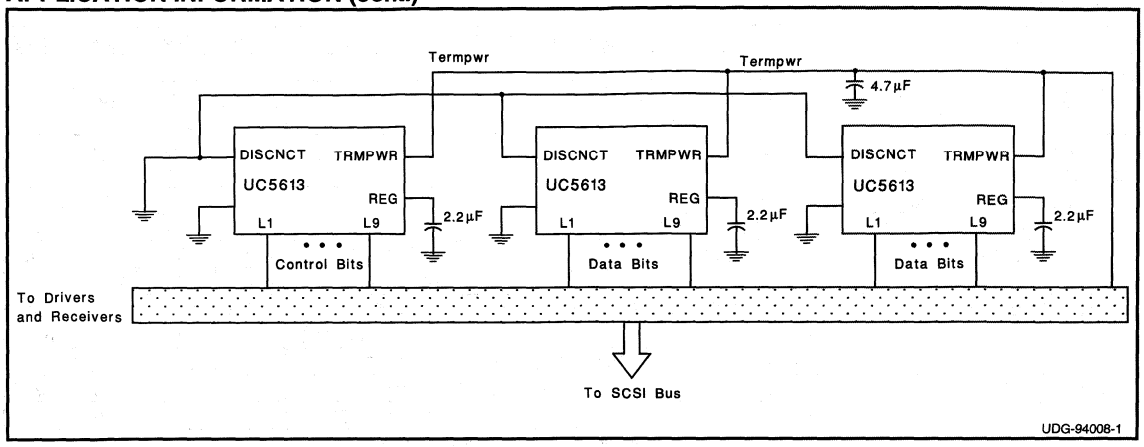


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5613 Devices.

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UNITRODE

9-Line 3-5 Volt Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SCSI-3 Standards
- 2.7V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 0.5µA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5614 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

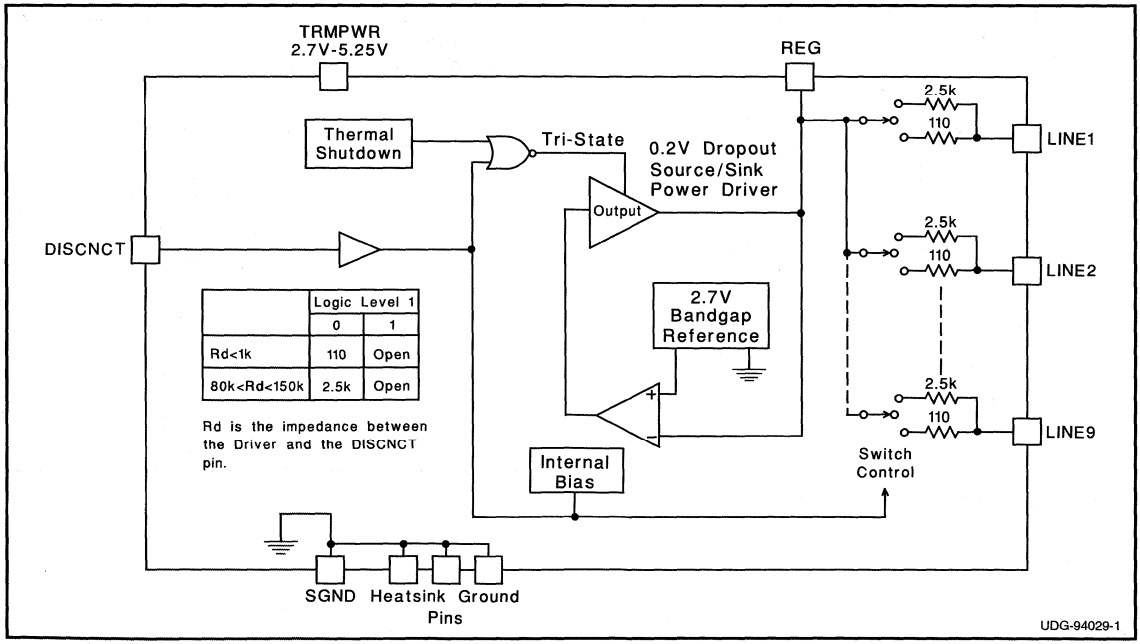
The UCC5614 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.7V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 0.5µA, which makes the IC attractive for battery powered systems.

The UCC5614 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5614 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible DISCNCT pin directly, the 110 ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high. When the DISCNCT pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high.

continued

BLOCK DIAGRAM



	Logic Level 1	
	0	1
Rd<1k	110	Open
80k<Rd<150k	2.5k	Open

Rd is the impedance between the Driver and the DISCNCT pin.

Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5614 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5614 is pin for pin compatible with Unitrode's other 9 line SCSI terminators, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5614, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (Zig-Zag In Line package), 24 pin TSSOP and 28 pin PLCC.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.6A
Storage Temperature..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

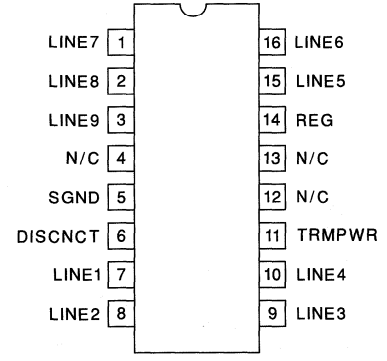
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

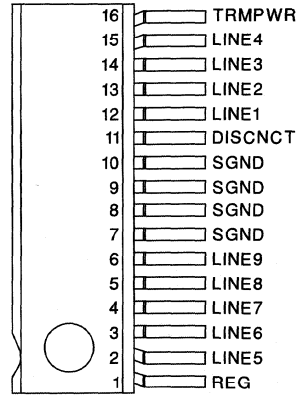
Termpwr Voltage ..... 2.7V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package



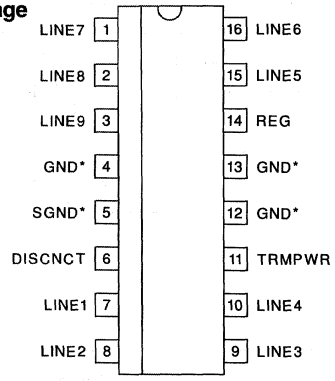
ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

CONNECTION DIAGRAMS (cont.)

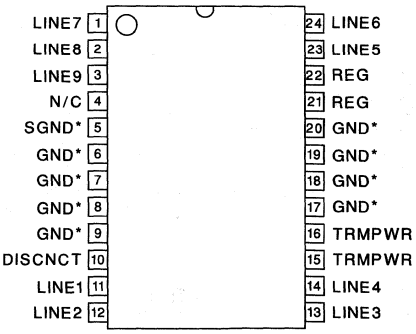
SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

Note: Drawings are not to scale.

TSSOP-24 (Top View)
PWP Package



** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

3

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, DISCNCT = 0V, $R_{DISCNCT}$= 0 ohms. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	218	mA
Power Down Mode	DISCNCT = Termpwr		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance		102.3	110	117.7	Ohms
Output High Voltage	(Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2) (DP Package)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2) (DP Package)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V
Short Circuit Current	V_{REG} = 0V	–200	–400	–800	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, DISCNCT = 0V, $R_{DISCNCT}$= 0 ohms. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (cont.)					
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	DISCNCT = 0V		30	50	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

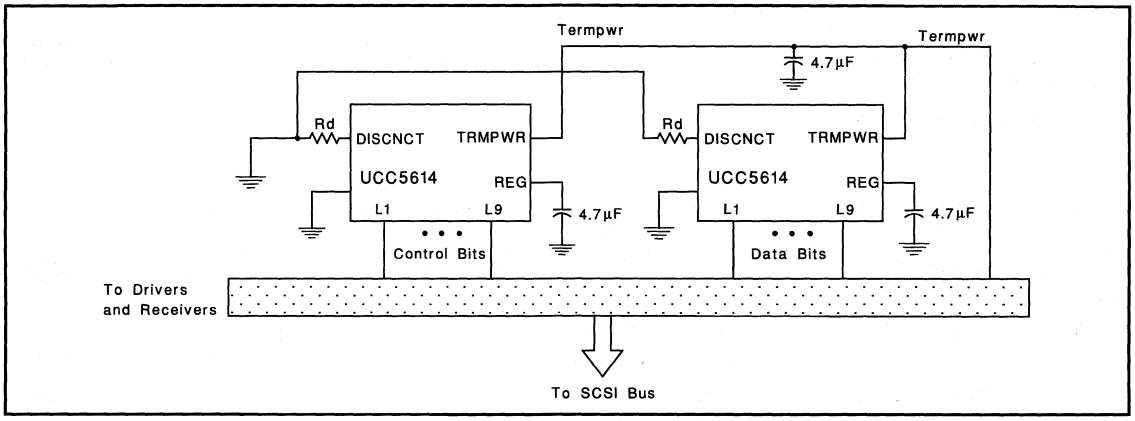


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UCC5614 Devices

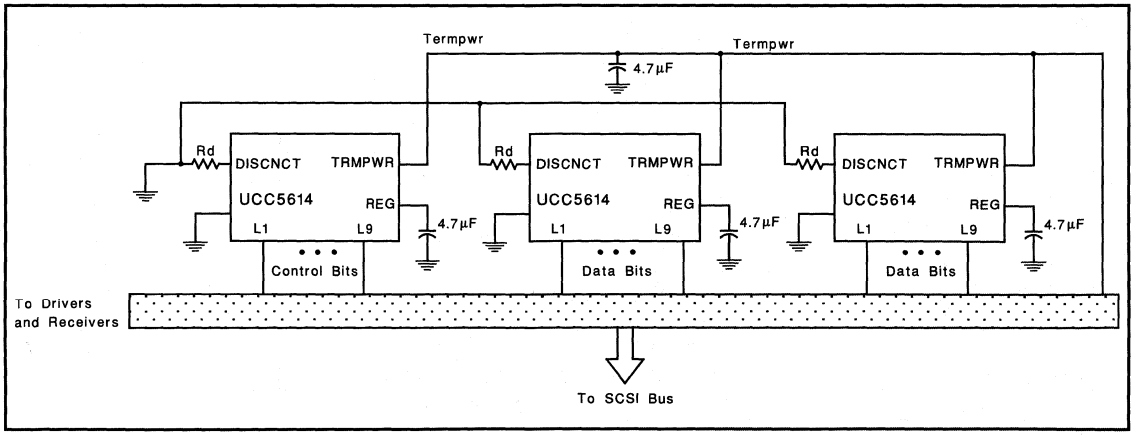


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UCC5614 Devices.

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UNITRODE

18-Line SCSI Terminator (Reverse Disconnect)

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50mA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- –650mA Sourcing Current for Termination
- Trimmed Impedance to 5%
- Thermal Shutdown
- Current Limit

DESCRIPTION

The UCC5617 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5609, the UCC5617 is ideal for high performance 5V SCSI systems, Termpwr 4.0-5.25V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5617 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

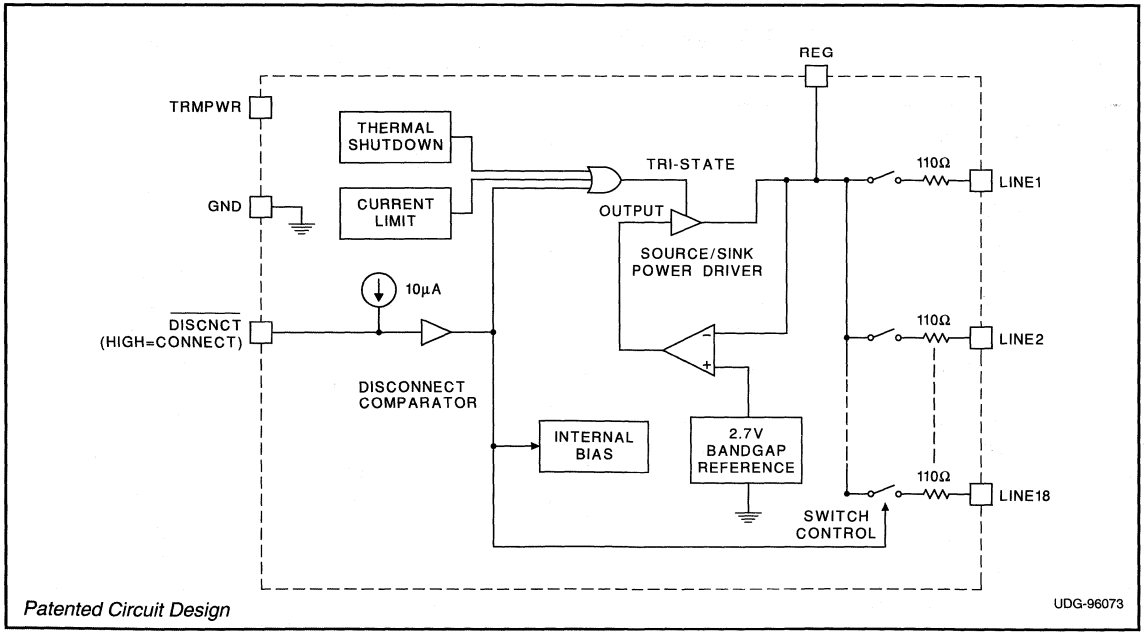
The power amplifier output stage allows the UCC5617 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5617, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, TSSOP and PLCC.

BLOCK DIAGRAM



Patented Circuit Design

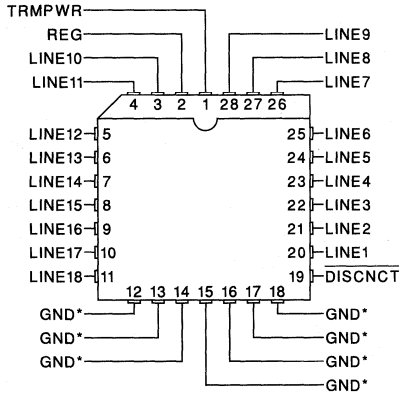
ABSOLUTE MAXIMUM RATINGS

TEMPWR. . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

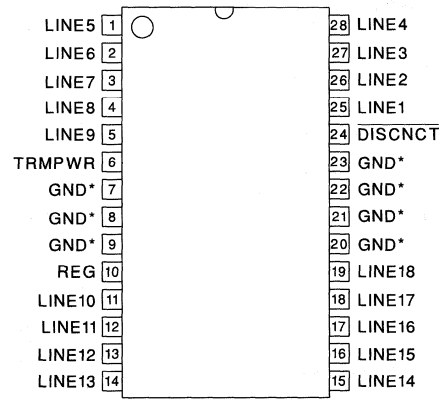
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



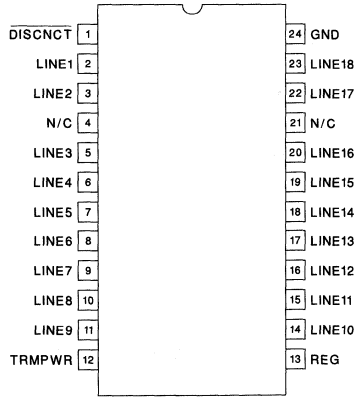
** DWP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



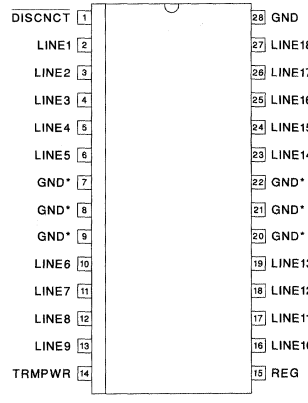
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21, and 22 serve as heatsink ground.*

DIL-24 (Top View)
N Package



Note: Drawings are not to scale.

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TERMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		420	440	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		50	100	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TERMPWR = 4V, T_J = 25°C (Note 1)	–21	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 2.4V, TRMPWR = 0V to 5.25V, REG = 0.2V, V_{LINE} = 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 2.4V (Note 2)		2	3.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–475	–650	–850	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	800	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	$\overline{\text{DISCNCT}}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculating: $Z = \frac{V_{OUT}\ N.L. - 0.2V}{I_{OUT}\ at\ 0.2V}$

PIN DESCRIPTIONS

$\overline{\text{DISCNCT}}$: Taking this pin low causes the 18 channels to become high impedance and the chip to go into low-power mode; a high or open state allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1–LINE18: 110Ω termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

Procedure:

1) Measure V_{REG} N.L.

2) Set $V_L = 0.2V$

3) Measure I_{MAX} at 0.2V

4) Impedance = $\frac{V_{REG}\ N.L. - 0.2V}{I_{MAX}}$

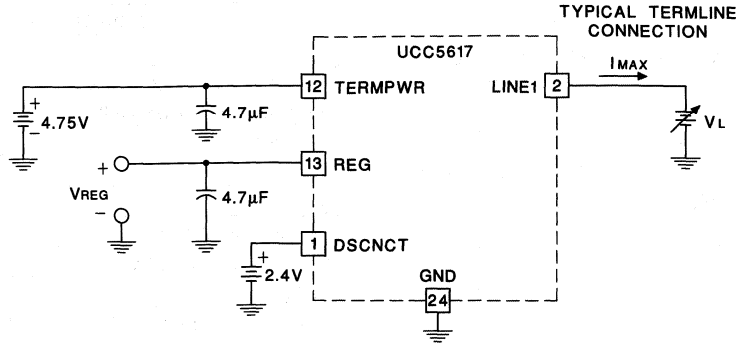
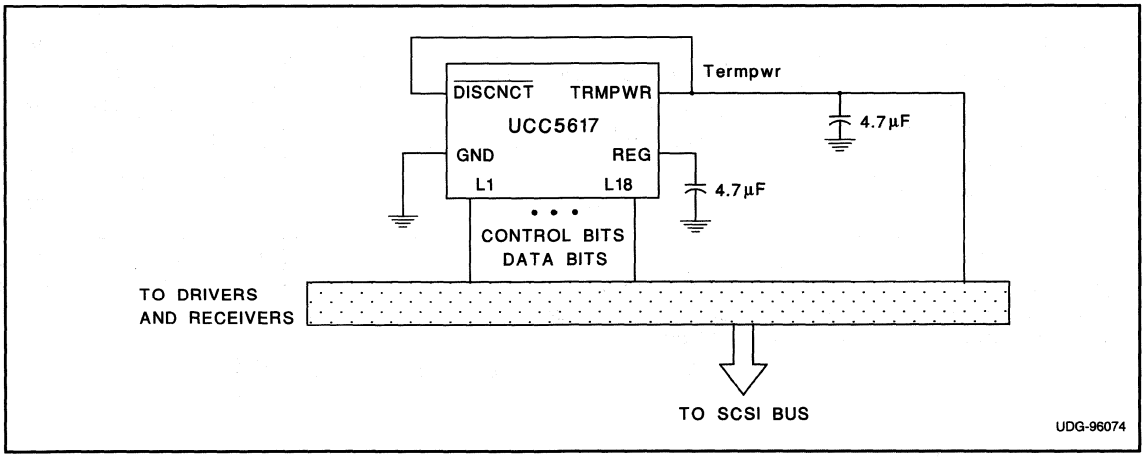


Figure 1. Termline Impedance Measurement Circuit

APPLICATION INFORMATION



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UNITRODE

18-Line SCSI Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50µA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- –650mA Sourcing Current for Termination
- Trimmed Impedance to 5%
- Thermal Shutdown
- Current Limit

DESCRIPTION

The UCC5618 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5601 and UC5608, the UCC5618 is ideal for high performance 5V SCSI systems, Termpwr 4.0-5.25V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5618 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

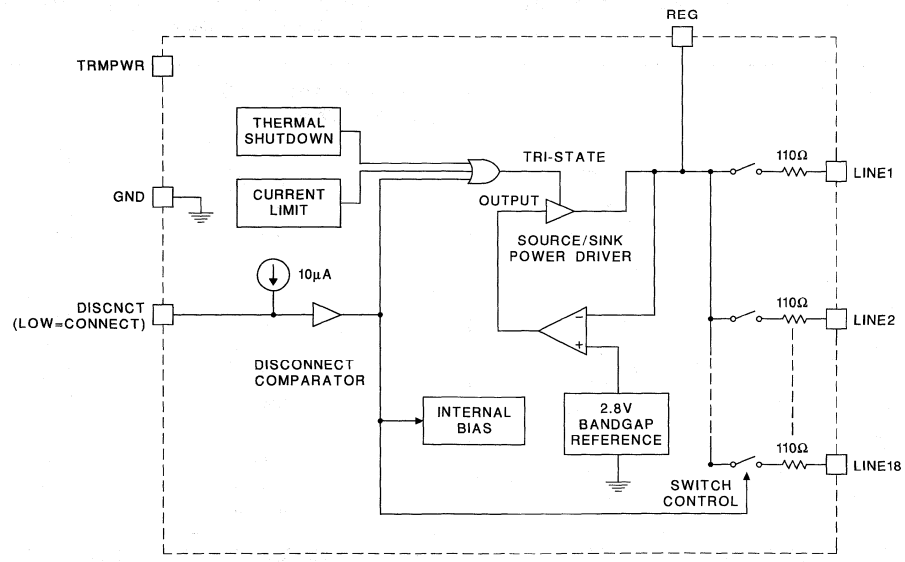
The power amplifier output stage allows the UCC5618 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5618, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, TSSOP and PLCC.

BLOCK DIAGRAM



Patented Circuit Design

UDG-96005-1

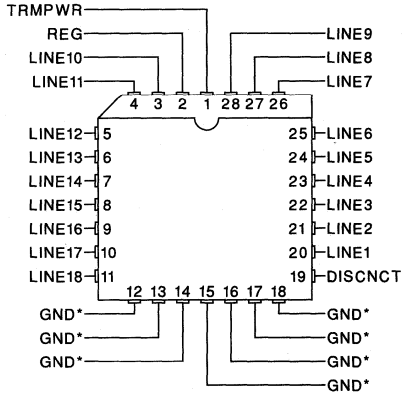
ABSOLUTE MAXIMUM RATINGS

TEMPWR. . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

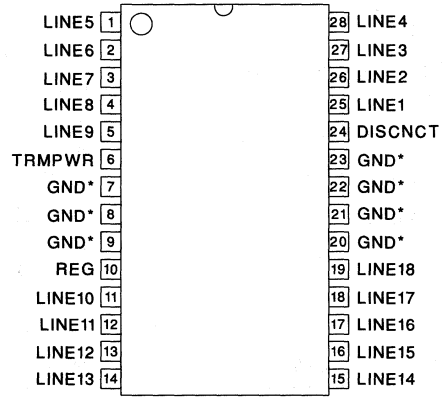
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



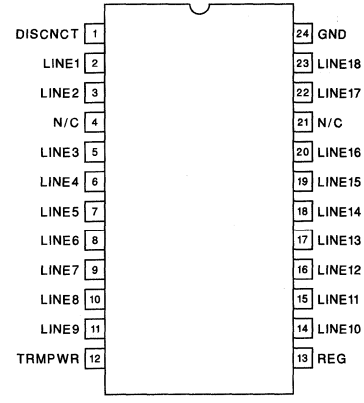
** DWP package pins 12–18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



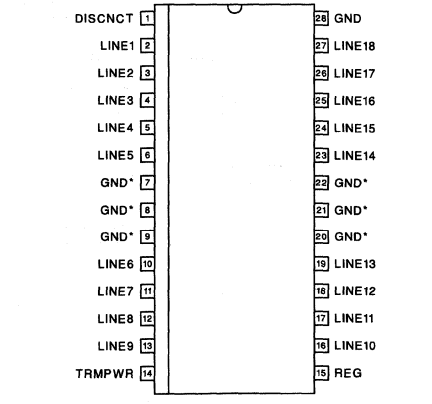
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21, and 22 serve as heatsink ground.*

DIL-24 (Top View)
N Package



Note: Drawings are not to scale.

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TERMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		420	440	mA
Power Down Mode	DISCNCT = TRMPWR		50	100	µA
Output Section (Termination Lines)					
Termination Impedance	See Figure 1	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TERMPWR = 4V, T_J = 25°C (Note 1)	–21	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V, REG = 0.2V, V_{LINE} = 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2)		2	3.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–475	–650	–950	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	800	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	DISCNCT = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

Procedure:

1) Measure V_{REG} N.L.
2) Set V_L = 0.2V
3) Measure I_{MAX} at 0.2V
4) Impedance = $\frac{V_{REG}\ N.L. - 0.2V}{I_{MAX}}$

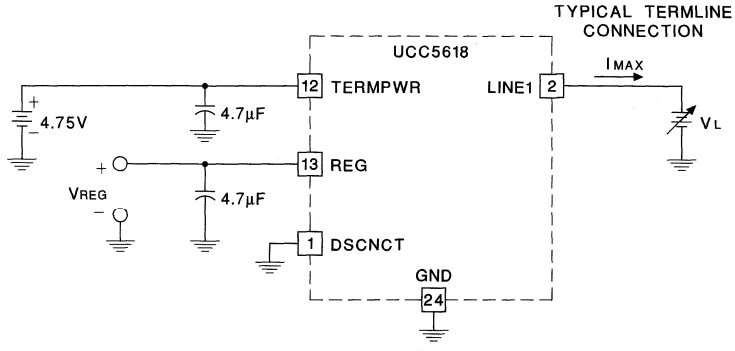


Figure 1. Termline Impedance Measurement Circuit

PIN DESCRIPTIONS

DISCNCT: Taking this pin high or leaving it open causes the 18 channels to become high impedance and the chip to go into low-power mode; a low state allows the channels to provide normal termination.

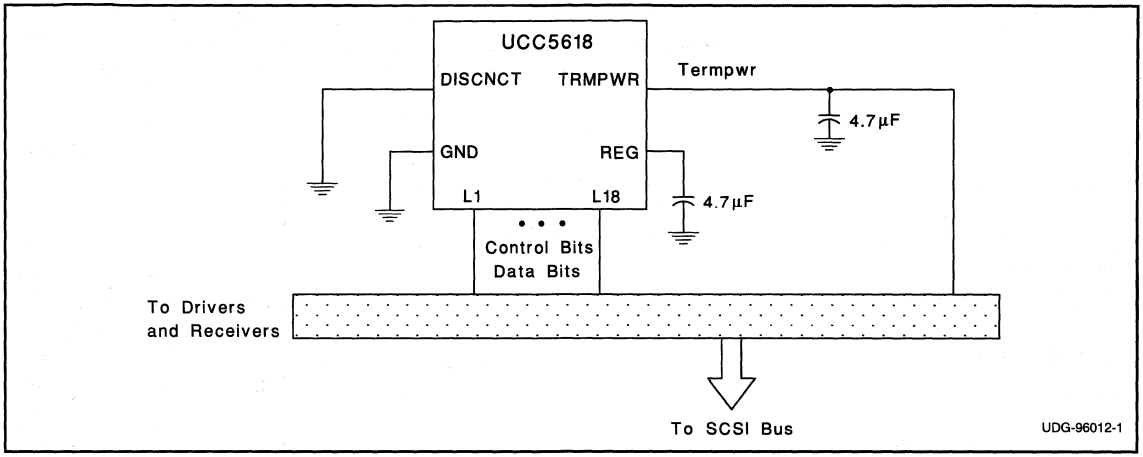
GND: Ground reference for the IC.

LINE1–LINE18: 110Ω termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

27-Line SCSI Terminator With Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5619 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5619 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5619 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5619 to source full termination current and sink active negation current when all termination lines are actively negated.

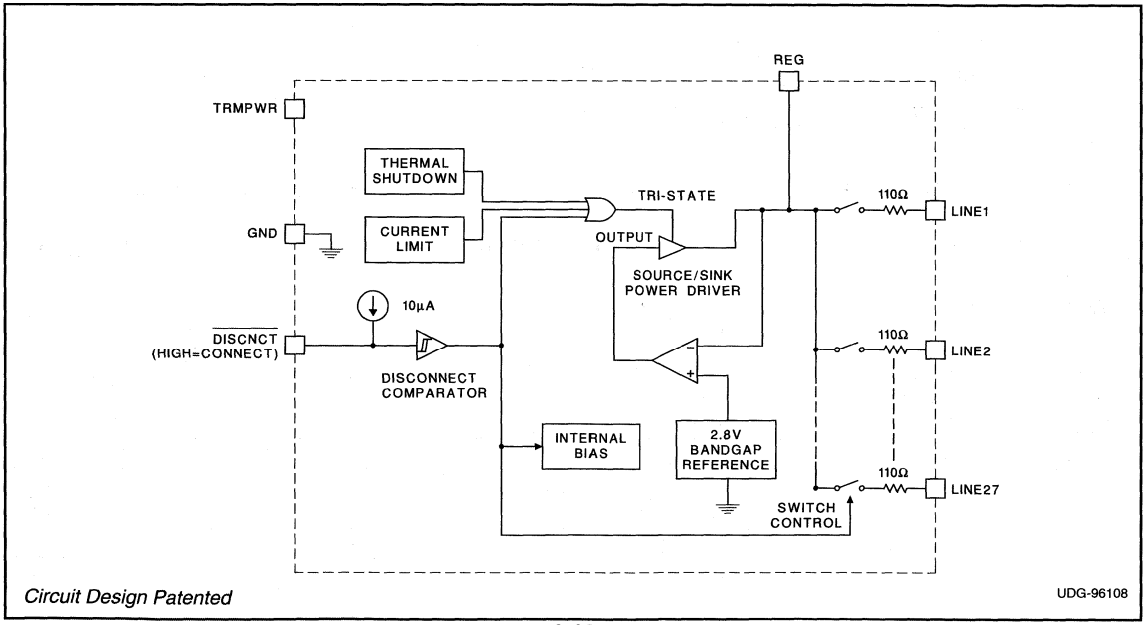
The UCC5619, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 36 pin wide body QSSOP (MWP) and 48 pin LQFP (FQP).

Consult SSOP-36 (MWP QSSOP-36) and FQP-48 Packaging Diagram for exact dimensions.

BLOCK DIAGRAM



Circuit Design Patented

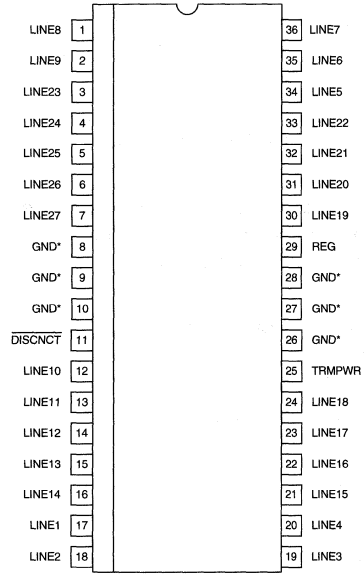
UDG-96108

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

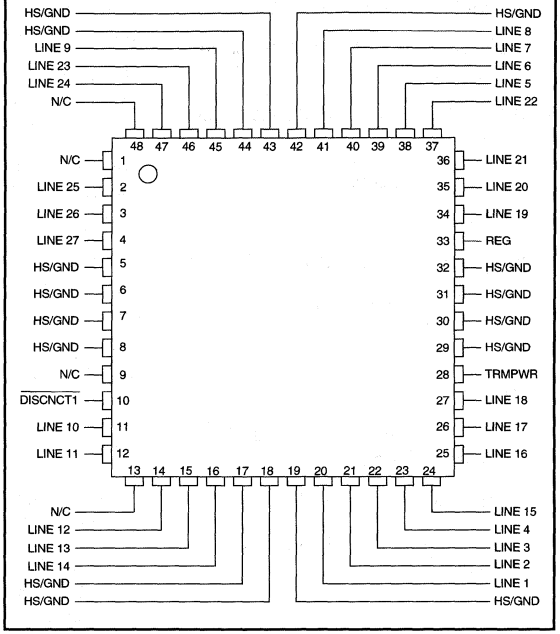
QSSOP-36 (Top View)
MWP Package



** MWP package pins 8 - 10 and 26 - 28 serve as heatsink/ground.*

CONNECTION DIAGRAM

LFQP-48 (Top View)
FQP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TRMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		100	200	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (CONT.)					
	V_{LINE} = 0.5V			22.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2.0	V
Input Current	$\overline{\text{DISCNCT}}$ = 0V		–20	–60	µA

PIN DESCRIPTIONS

DISCNCT: Taking this pin low causes all channels to become high impedance, and the chip to go into low-power mode; a high state or leaving it open allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1 - LINE27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator; bypass with a 4.7µF capacitor to GND.

TRMPWR: Power for the IC; bypass with a 4.7µF capacitor to GND.

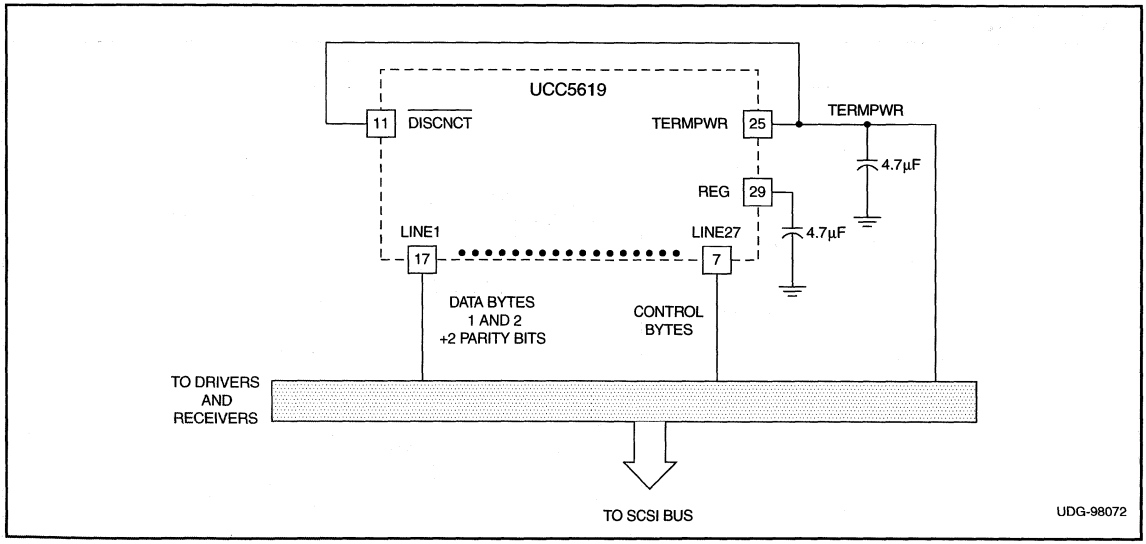


Figure 1. Typical wide SCSI bus configuration using the UCC5619

UNITRODE CORPORATION
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TEL. (603) 424-2410 FAX (603) 424-3460

27-Line SCSI Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance during Disconnect
- 100mA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5620 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5620 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5620 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5620 to source full termination current and sink active negation current when all termination lines are actively negated.

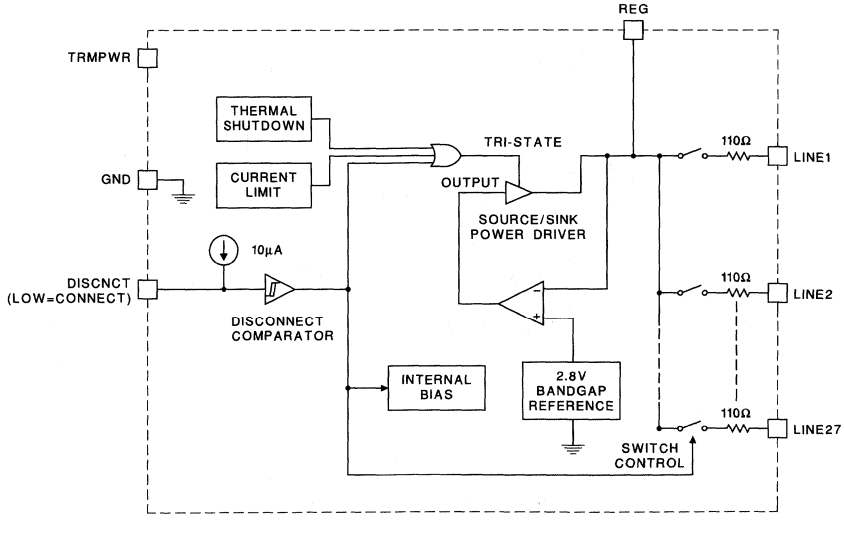
The UCC5620, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 36-Pin Wide Body QSOP (MWP) and 48-Pin LQFP (FQP).

Consult QSOP-36 or LQFP-48 packaging diagram for exact dimensions.

BLOCK DIAGRAM



Circuit Design Patented

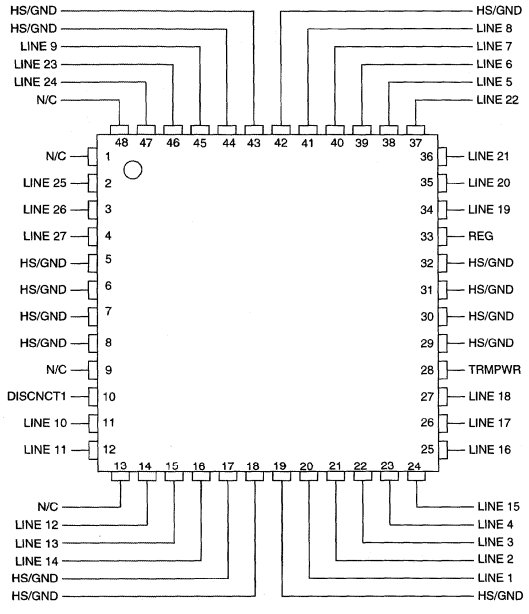
UDG-96109

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

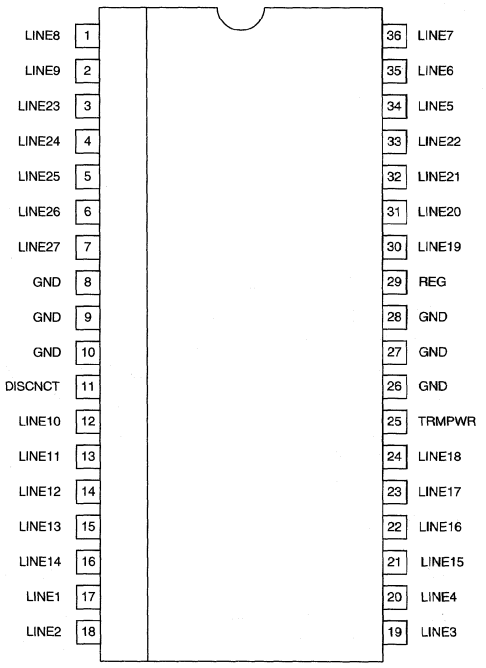
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

LFQP-48 (Top View)
FQP Package



CONNECTION DIAGRAM

SSOP-36 (Top View)
MWP Package



3

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TRMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	DISCNCT = TRMPWR		100	200	µA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		C°
Thermal Shutdown Hysteresis			10		C°
Disconnect Section					
Disconnect Threshold		0.8	1.5	2.0	V
Input Current	DISCNCT = 0V		–20	–60	µA

Note 1:*Measuring each termination line while other 26 are low (0.2V).*

Note 2:*Guaranteed by design. Not 100% tested in production.*

Note 3:*Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:* $Z = \frac{(V_{OUT}\ N.L - 0.2V)}{I_{OUT}\ at\ 0.2V}$

PIN DESCRIPTIONS

DISCNCT: Taking this pin high or leaving it open causes all channels to become high impedance, and the chip to go into low-power mode; a low state allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1 - LINE27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION

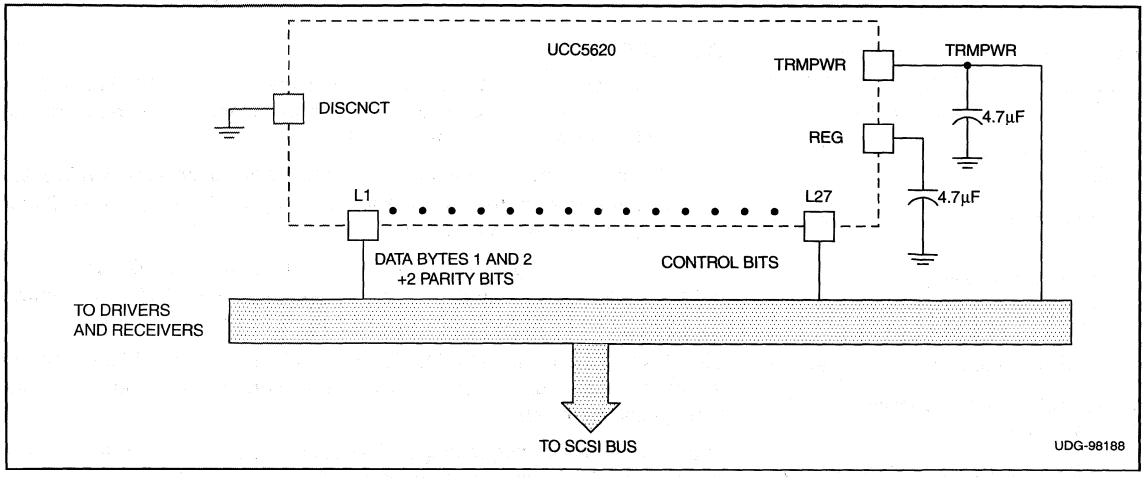


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5620

UNITRODE CORPORATION
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TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

27 - Line SCSI Terminator With Split Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance During Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Split Reverse Controls Lines 1 to 9 and 10 to 27 Separately
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5621 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5621 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5621 features a split reverse disconnect allowing the user to control termination lines 10 to 27 with disconnect one, $\overline{\text{DISCNCT1}}$, and control terminiation lines 1 to 9 with disconnect two, $\overline{\text{DISCNCT2}}$.

The UCC5621 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

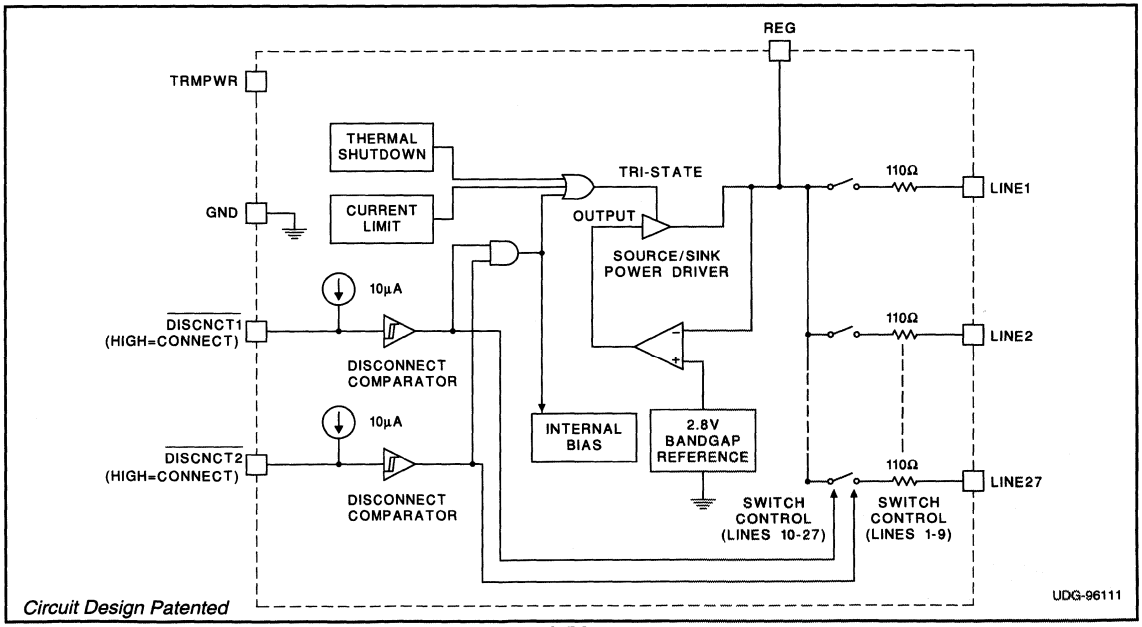
The power amplifier output stage allows the UCC5621 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5621, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

(continued)

BLOCK DIAGRAM



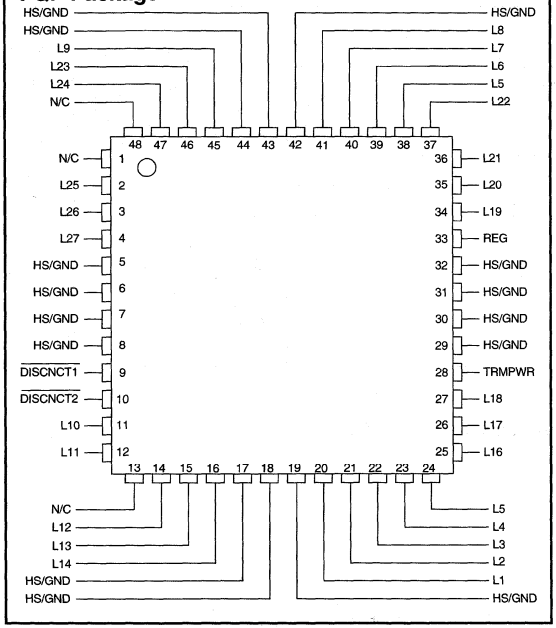
Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

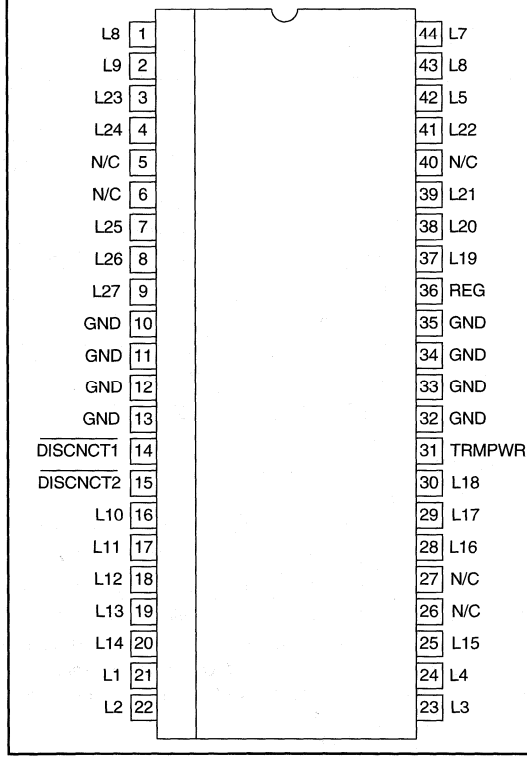
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

LQFP-48 (Top View)
FQP Package



CONNECTION DIAGRAM

QSOP-44 (Top View)
MWP Package



DESCRIPTION (cont.)

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 44 pin wide body QSOP (MWP) and 48 pin LQFP. Consult QSOP-44 and FQP-48 Packaging Diagrams for exact dimensions.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT1}}$ = $\overline{\text{DSCNCT2}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TRMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DSCNCT2}}$ = 0V		100	200	µA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{DISCNCT1}$ = $\overline{DSCNCT2}$ = 4.75V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 0V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold $\overline{DISCNCT1}$	Controls Lines 10 to 27	0.8	1.5	2.0	V
Input Current $\overline{DISCNCT1}$	$\overline{DISCNCT1}$ = 0V		–10	–30	µA
Disconnect Threshold $\overline{DISCNCT2}$	Controls Lines 1 to 9	0.8	1.5	2	V
Input Current $\overline{DISCNCT2}$	$\overline{DISCNCT2}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:

$$Z = \frac{V_{OUT}\ N.L - 0.2V}{I_{OUT}\ at\ 0.2V}$$

PIN DESCRIPTIONS

$\overline{DISCNCT1}$: Disconnect one controls termination lines L10 – L27. Taking this pin low causes termination lines L10 – L27 to become high impedence, taking this pin high or leaving it open allows the channels to provide normal termination.

$\overline{DISCNCT2}$: Disconnect two controls termination lines L1 – L9. Taking this pin low causes termination lines L1 – L9 to become high impedence. Taking this pin high or leaving it open allows the channels to provide normal terminiation. Taking both disconnect pins low will put the chip in to sleep mode where it will be in low-power mode.

GND: Ground reference for the IC.

L1 - L27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

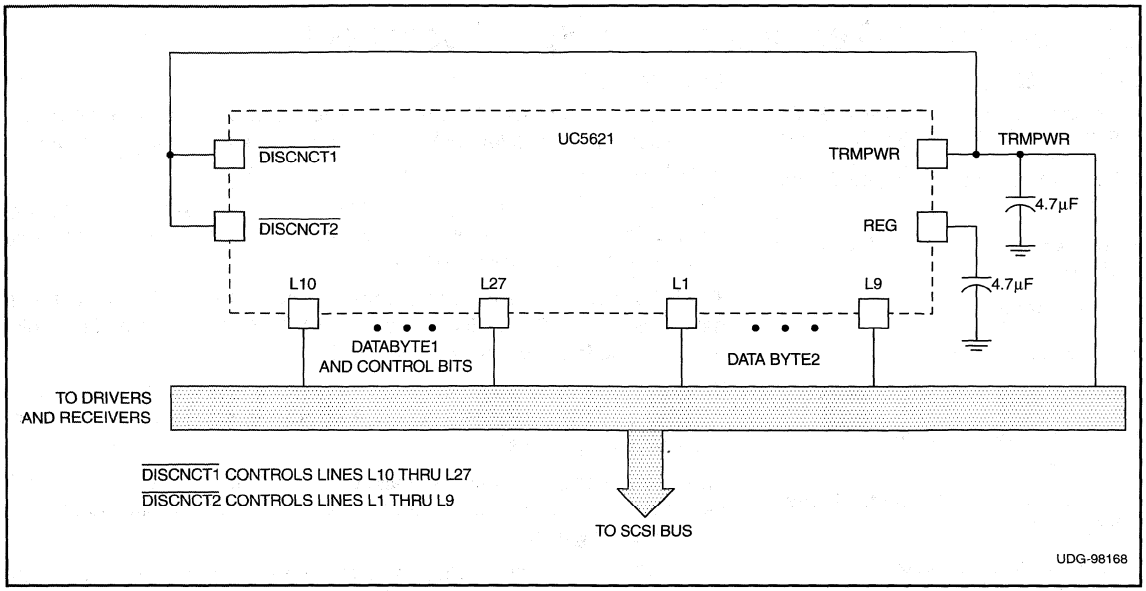


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5621

UNITRODE CORPORATION
7 CONTINENTAL BOULEVARD • MERRIMACK, NH 03054
TEL (603) 424-2410 • FAX (603) 424-3460

27 - Line SCSI Terminator With Split Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance During Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Split Disconnect Controls Lines 1 to 9 and 10 to 27 Separately
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5622 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5622 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5622 features a split disconnect allowing the user to control termination lines 10 to 27 with disconnect one, DISCNCT1, and control terminiation lines 1 to 9 with disconnect two, DISCNCT2.

The UCC5622 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

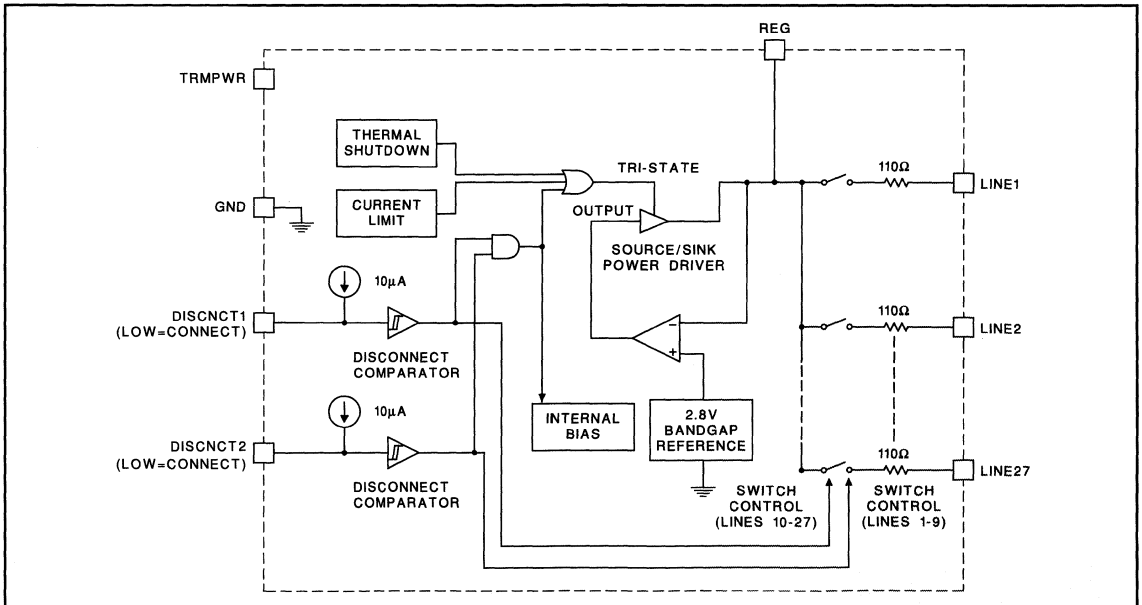
The power amplifier output stage allows the UCC5622 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5622, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

(continued)

BLOCK DIAGRAM



Circuit Design Patented

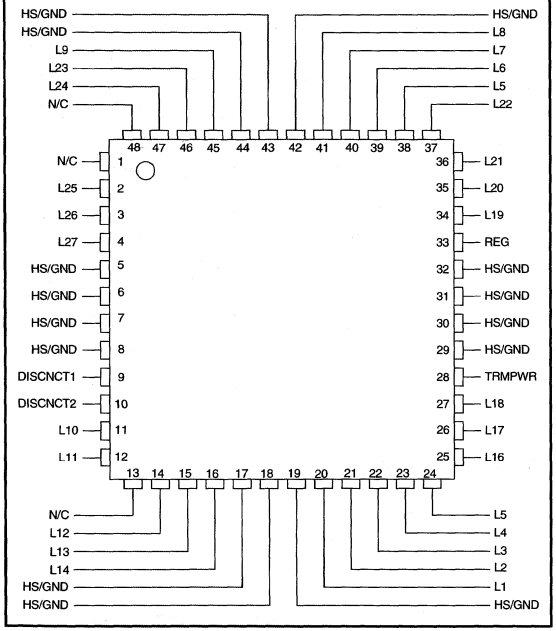
UDG-96113

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

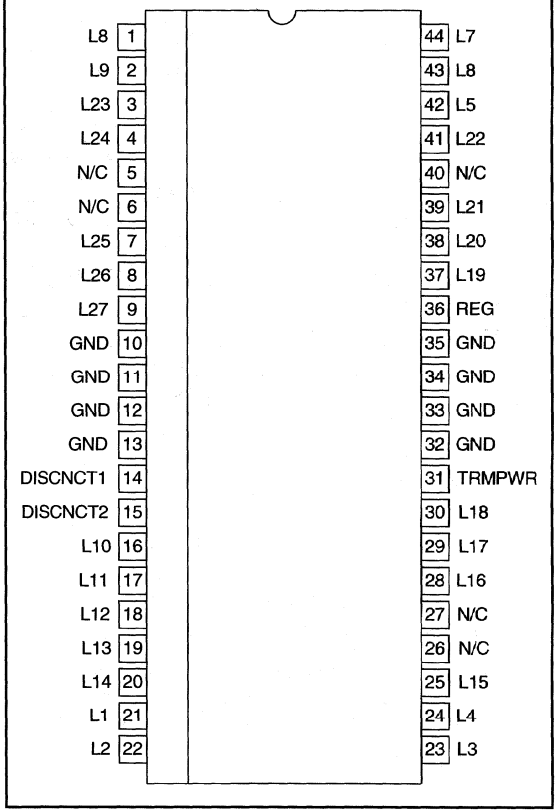
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

LQFP-48 (Top View)
MWP Package



CONNECTION DIAGRAM

QSOP-44 (Top View)
MWP Package



DESCRIPTION (cont.)

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 44 pin wide body QSOP (MWP) and 48 pin LQFP (FQP). Consult QSOP-44 and LQFP-48 Packaging Diagram for exact dimensions.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT1 = DSCNCT2 = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TRMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	DISCNCT1 = DSCNCT2 = TRMPWR		100	200	µA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT1 = DSCNCT2 = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	-22.1	-23.3	-24	mA
	V_{LINE} = 0.2V	-20.7	-23.3	-24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	-21	-23	-24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	-20	-23	-24	mA
	V_{LINE} = 0.5V			-22.4	mA
Output Leakage	DISCNCT1 = DISCNCT2 = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT1 = DISCNCT2 = 2.4V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	-650	-900	-1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold DISCNCT1	Controls Lines 10 to 27	0.8	1.5	2.0	V
Input Current DISCNCT1	DISCNCT1 = 0V		-10	-30	µA
Disconnect Threshold DISCNCT2	Controls Lines 1 to 9	0.8	1.5	2	V
Input Current DISCNCT2	DISCNCT2 = 0V		-10	-30	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:

$$Z = \frac{V_{OUT}\ N.L - 0.2V}{I_{OUT}\ at\ 2.0V}$$

PIN DESCRIPTIONS

DISCNCT1: Disconnect one controls termination lines 10 – 27. Taking this pin high or leaving it open causes termination lines 10 - 27 to become high impedence, taking this pin low allows the channels to provide normal termination.

DISCNCT2: Disconnect two controls termination lines 1 – 9. Taking this pin high or leaving it open causes termination lines 1 - 9 to become high impedence. Taking this pin low allows the channels to provide normal terminiation. Taking both disconnect pins high or leaving them open will put the chip in to sleep mode where it will be in low-power mode.

GND: Ground reference for the IC.

L1 – L27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

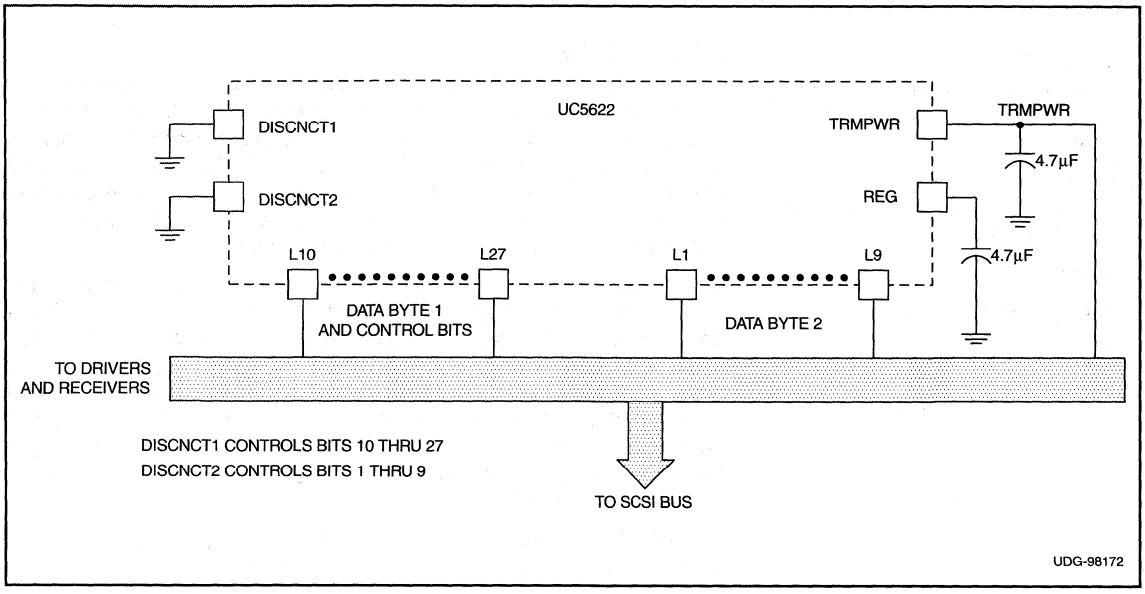


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5622

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Multimode SCSI 14 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD) and Ultra3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF.

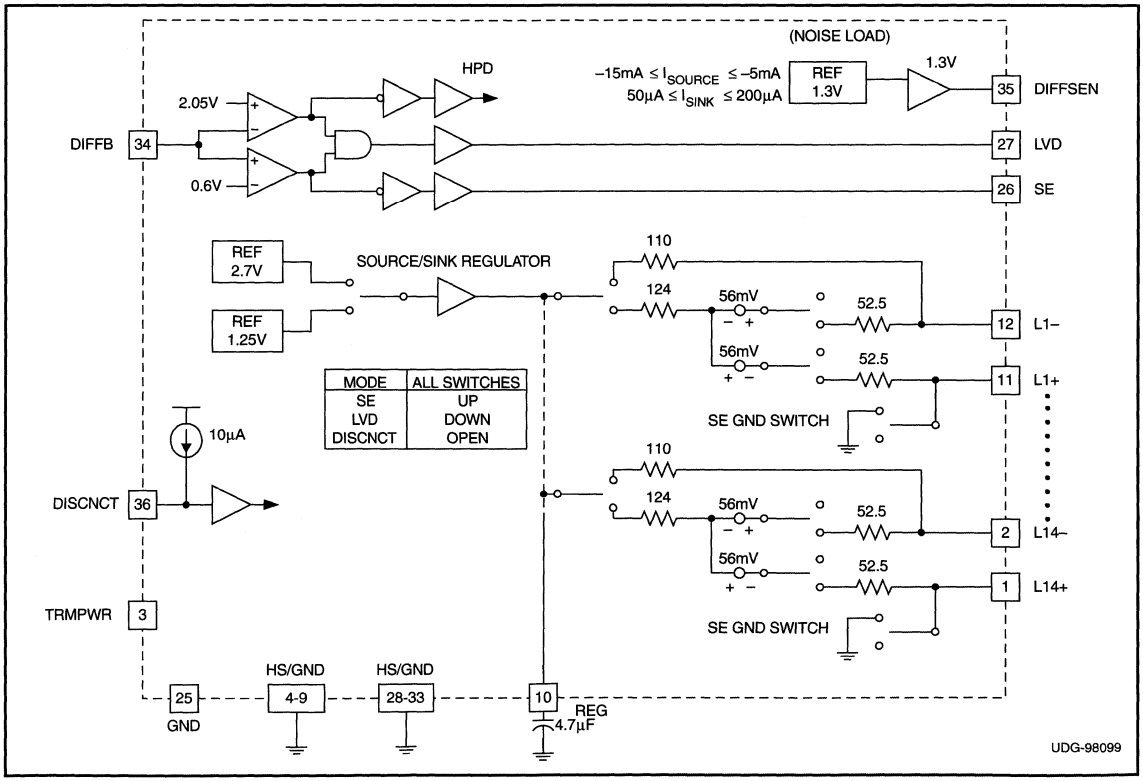
DESCRIPTION

The UCC5628 Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5628 can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5628 detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5628 is offered in a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Recommended Operating Conditions . . . . . 2.7V to 5.25V

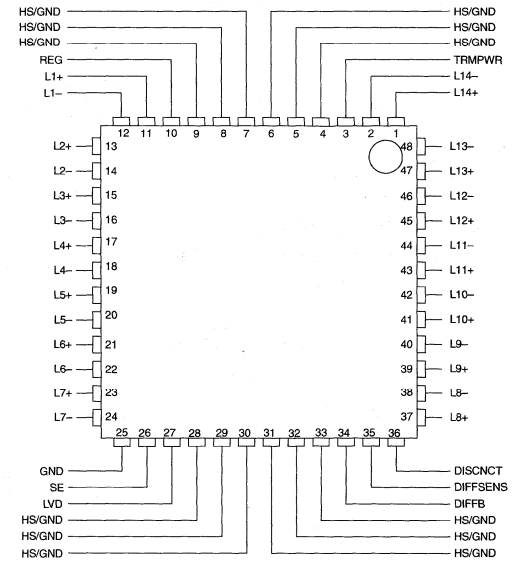
Currents are positive into negative out of the specified terminal.
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 2.7V to 5.25V
Temperature Ranges . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

(TOP VIEW)
FQP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode		20	25	mA
	SE Mode		1.6	10	mA
	Disabled Terminator		250	400	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
1.25V Regulator Sink Current	V_{REG}= 3.3V	170	300	700	mA
1.3V Regulator	Diff Sense	1.2	1.3	1.4	V
1.3V Regulator Source Current	V_{REG}= 0V	–15		–5	mA
1.3V Regulator Sink Current	V_{REG}= 3.3V	50		200	µA
2.7V Regulator	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
2.7V Regulator Sink Current	V_{REG}= 3.3V	170	300	700	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedence	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Single Ended Termination Section					
Impedance	$Z = (VL_X - 0.2V)/IL_X$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–21	–24	–25.4	mA
	Signal Level 0.5V	–18		–22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I= 10mA		20	60	Ω
Disconnect and Diff Buffer Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			10	30	µA
Diff Buffer Single Ended to LVD Threshold		0.5		0.7	V
Diff Buffer LVD to HPD Threshold		1.9		2.2	V
DIFFB Input Current		–10		10	µA
Status Bits (SE, LVD) Output Section					
I_{SOURCE}	V_{LOAD} = 2.4V	–4	–6		mA
I_{SINK}	V_{LOAD} = 0.4V	2	5		mA

Note 1: *Guaranteed by design. Not 100% tested in production.*

Note 2: $Z_{CM} = \frac{1.2V}{\left[I_{(VCM+0.6V)} - I_{(VCM-0.6V)}\right]}$ *where VCM=voltage measured with L+ tied to L– and zero current applied*

Note 3: *VL_X= Output voltage for each terminator minus output pin (L1– through L14–) with each pin unloaded.*
IL_X = Output current for each terminator minus output pin (L1– through L14–) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Diff sense filter pin should be connected at a 0.1µF capacitor.

DIFFSENS: The SCSI bus Diff Sense line to detect what types of devices are connected to the SCSI bus.

DISCNCT: Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.

LINE*n*–: Signal line active line for single ended or negative line in differential applications for the SCSI bus.

LINE*n*+: Ground line for single ended or positive line for differential applications for the SCSI bus.

LVD: TTL Compatible status bit indicating that the device has detected the bus in LVD mode. If the terminator is conected it is in LVD mode.

REG: Regulator bypass pin, must be connected to a 4.7µF capacitor.

SE: TTL Compatible status bit indicating that the device has detected the bus in single ended mode. If the terminator is conected it is in single ended mode.

TRMPWR: V_{IN} 2.7V to 5.25V supply.

APPLICATION INFORMATION

The UCC5628 is a Multi-mode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the "diff sense" signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. A LVD or multi-mode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If a HVD device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5V is single ended, between 0.7V and 1.9V is LVD and above 2.2V is HVD.

In the single ended mode, a multi-mode terminator has a 110Ω terminating resistor connected to a 2.7V termination voltage regulator. The 2.7V regulator is used on all Unitrode terminators designed for 3.3V systems. This requires the terminator to operate in specification down to 2.7V TRMPWR voltage to allow for the 3.3V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD or disconnect mode. The device requirements call for 1.5pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

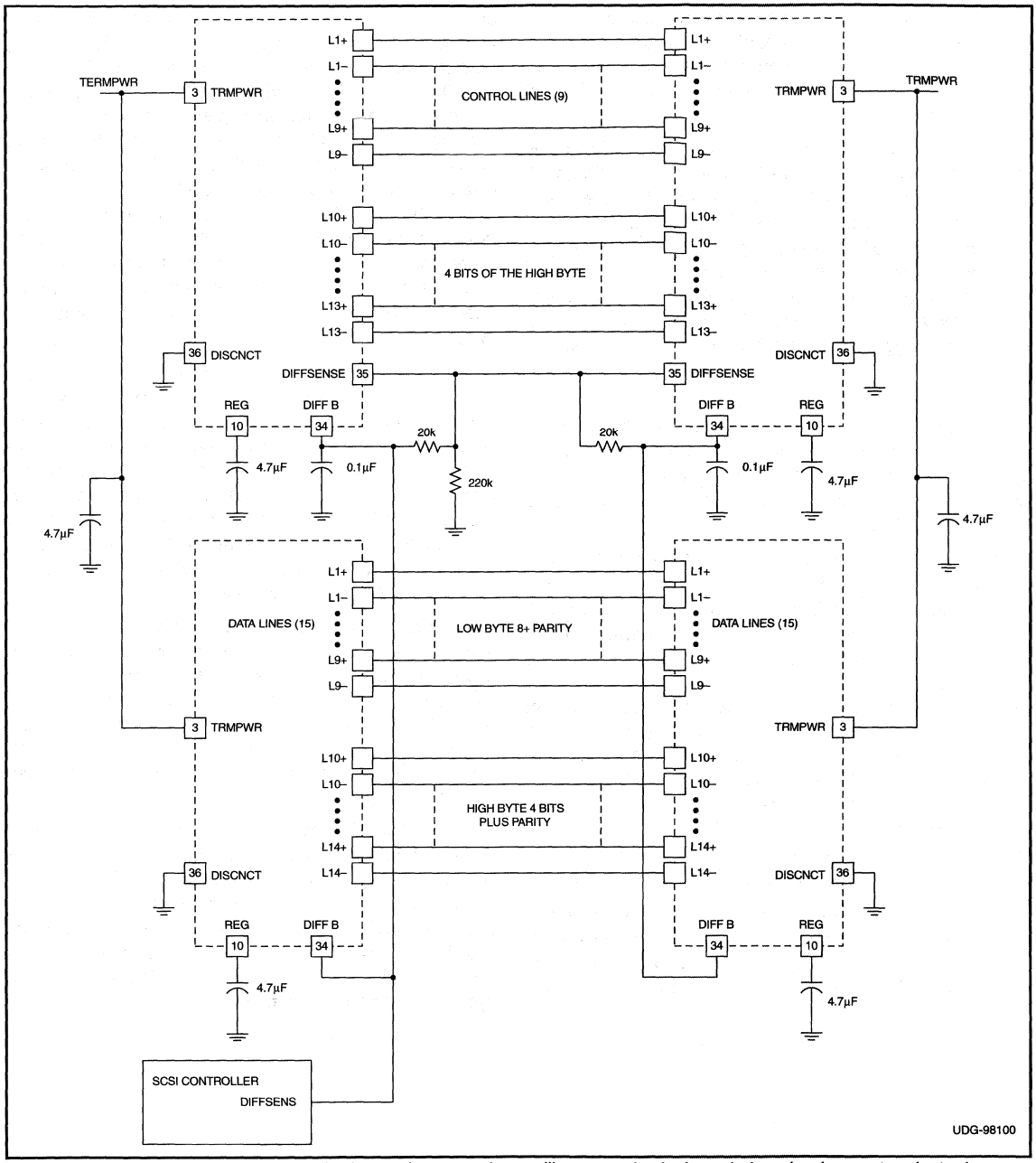
Layout is very critical for Ultra2 and Ultra3 systems. Multi-layer boards need to adhere to the 120Ω impedance standard, including connector and feed-through. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between the runs within a pair, and a minimum of 8 mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems.

Capacitance balance is critical for Ultra2 and Ultra3. The balance capacitance standard is 0.5pF per line with the balance between pairs of 2pF. The components are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multi-mode terminators need to consider power dissipation; the UCC5628 is offered in a power package with heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

In 3.3V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3V battery systems normally have a 10% tolerance. The UCC3912 is 150mV drop under LVD loads, allowing 150mV drop in the cable system. All Unitrode LVD and multi-mode terminators are designed for 3.3V systems, operating down to 2.7V.

TYPICAL APPLICATION



Note: *A 220k resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFFSENS ties to the DIFFB pin on the terminators, only one RC network should be on a device.*

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UNITRODE

Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator

FEATURES

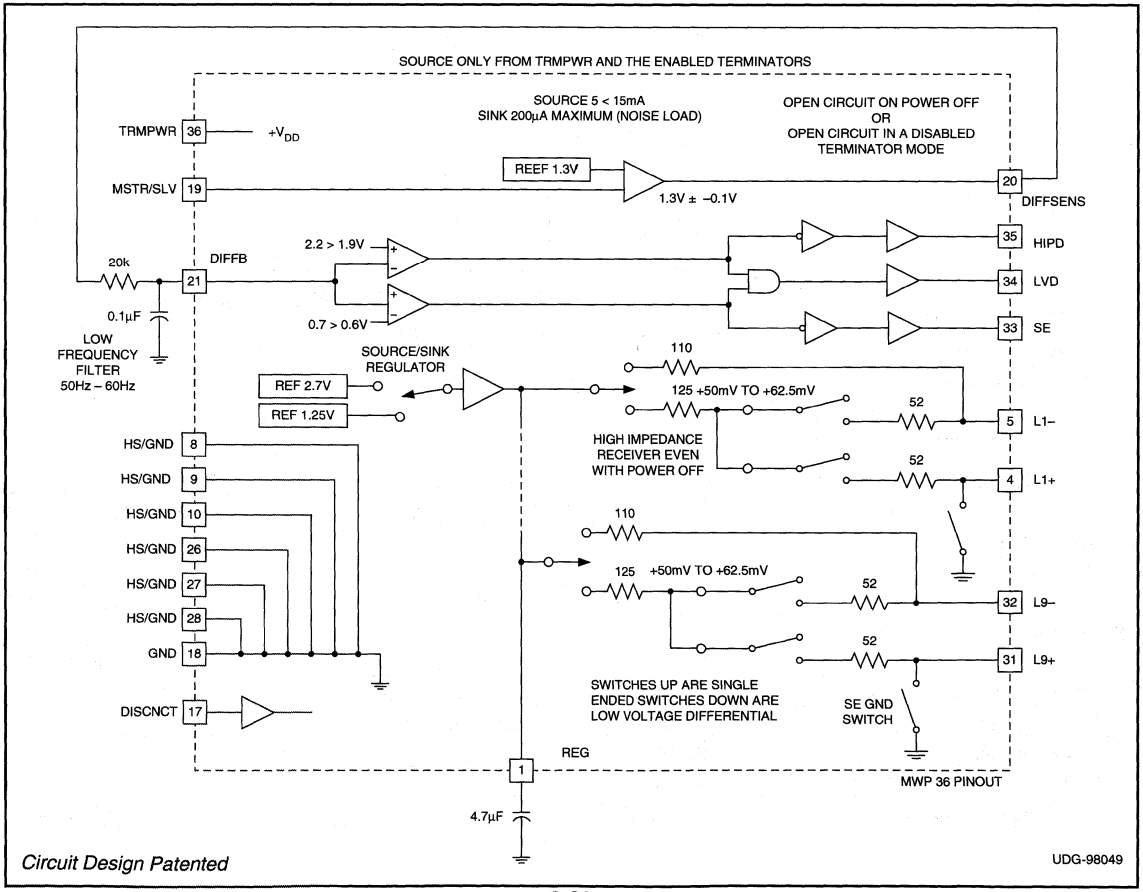
- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF
- Master/Slave Inputs
- Supports Active Negation
- Standby (Disable Mode) 5µA
- 3pF Channel Capacitance

DESCRIPTION

The UCC5630 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for Fast-40 and Fast-80, but has the potential of speeds up to Fast-320. The UCC5630 is SPI-2, SPI and Fast-20 compliant. Consult QSOP-36 and LQFP-48 Package Diagram for exact dimensions.

The UCC5630 can not be used with SCSI high voltage differential (HVD) EIA485. It will shut down when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD or single ended and the bias voltage, current and power are also different for EIA485 differential.

BLOCK DIAGRAM



Circuit Design Patented

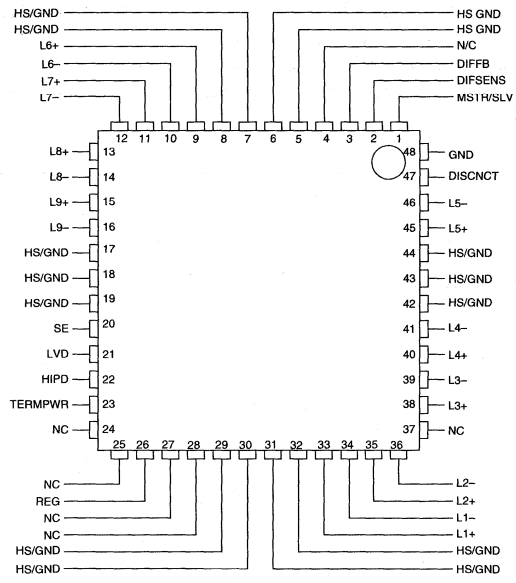
UDG-98049

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Power Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

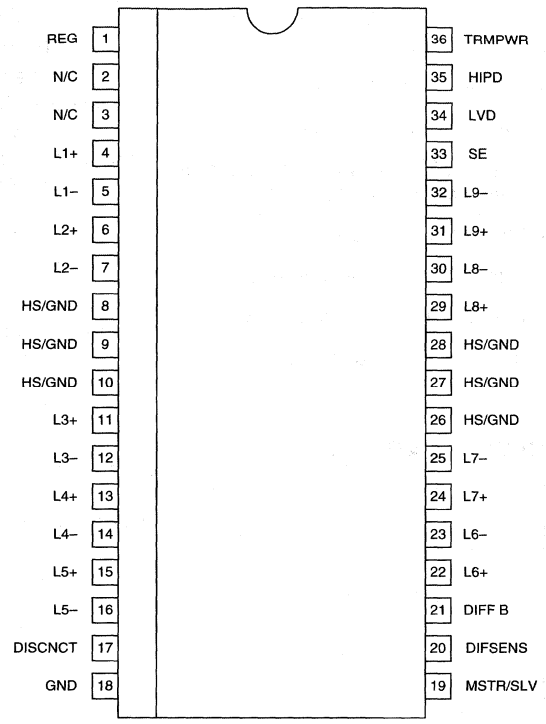
All voltages are with respect to PIN1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

LQFP-48 (Top View)
FQP Package



CONNECTION DIAGRAM

QSOP-36 (Top View)
MWP Package



RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 2.7V TO 5.25V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current				20	mA
	Disable Terminator, in DISCNCT mode.			35	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	LVD Mode, Differential Sense Floating	–80	–100		mA
1.25V Regulator Sink Current	LVD Mode, Differential Sense Floating	80	100		mA
1.3V Regulator	DIFSENS	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFSENS	–5		–15	mA
1.3V Regulator Sink Current	DIFSENS	50		200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
2.7V Regulator	Single Ended Mode	2.5	2.7	3	V
2.7V Regulator Source Current	Single Ended Mode	–200	–400	–800	mA
2.7V Regulator Sink Current	Single Ended Mode	100	200	400	mA
2.7V Regulator Dropout Voltage	V_{TRMPWR} – (V_{REG} – 2.7 Min)			200	mV
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance		110	125	165	Ω
Differential Bias Voltage	Drivers Tri-stated	100		125	mV
Common Mode Bias			1.25		V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3.5	pF
Single Ended Termination Section					
Impedance		102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V	–21	–23	–25.4	mA
	Signal Level 0.5V			–22.4	mA
Output Leakage	Disabled, TRMPWR = 0V to 5.25V			400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SW Impedance				60	Ω
Disconnect (DISCNCT) Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current	$V_{DISCNCT}$ = 0V and 3.3V	–30		30	µA
Differential Sense (DIFFB) Input Sections					
DIFFB Single Ended Threshold		0.6		0.7	V
DIFFB Sense LVDS Threshold		1.9		2.2	V
DIFFB Input Current	V_{DIFFB} = 0V and 3.3V	–30		30	µA
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold		0.8		2	V
MSTR/SLV Input Current		–30		30	µA
Status Bits (SE, LVD, HIPD) Output Section					
I_{SOURCE}	V_{LOAD} = 2.4V	–4	–8.7		mA
I_{SINK}	V_{LOAD} = 0.5V	3	6		mA
	V_{LOAD} = 0.4V	2	5		mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

DIFFB: DIFSENS filter pin should be connected to a 0.1µF capacitor to GND and 20k resistor to SCSI/Bus DIFSENS Line.

DIFSENS: The SCSI bus DIFSENS line is driven to 1.3V to detect what type of devices are connected to the SCSI bus.

DISCNCT: Disconnect shuts down the terminator when it is not at the ended of the bus. The disconnect pin low enables the terminator.

HIPD: TTL compatible status bit indicating high voltage differential has been detected on DIFFB. The terminator is in shutdown. (Not valid in disconnect mode.)

HS/GND: Heat Sink GND. Connect to large area PC board traces to increase power dissipation capability.

GND: Power Supply Return.

L1– thru L9–: Signal line/active line for single ended or negative line in differential applications for the SCSI bus.

L1+ thru L9+: Ground line for single ended or positive line for differential applications for the SCSI bus.

LVD: TTL compatible status bit indicating low voltage differential level on DIFFB. The terminator is in LVD mode.(Not valid in disconnect mode.)

PIN DESCRIPTIONS (cont.)

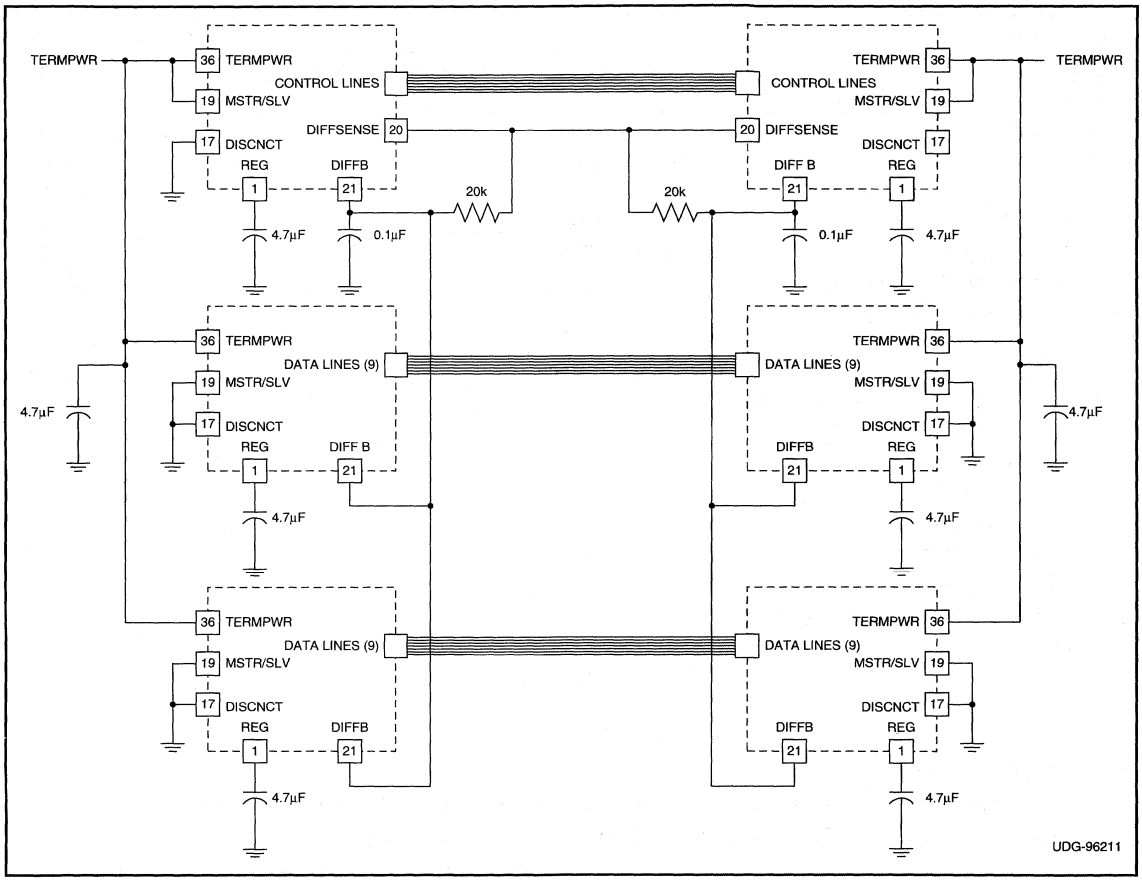
MSTR/SLV: Mode select for the non-controlling terminator. MSTR enables the 1.3V regulator, when the terminator is enabled. Note: Theis function will be removed on further generations of the multimode terminators.

REG: Regulator bypass, must be connected to a 4.7µF capacitor.

SE: TTL compatible status bit indicating single ended device has been detected on DIFFB. The terminator is in single ended mode.

TRMPWR: VIN 2.7V to 5.25V supply.

APPLICATION INFORMATION



Balancing capacitor is very important in high speed operation. The typical balance between the positive (+) and negative (–) signals is 0.1pF except for L8 and L9, 0.23pF and 0.4pF respecitvely on the MWP package. The negative (–) signal has higher capacitance than the positive (+) signal. The FQP package is typically 0.2pF less than the MWP. Typical balance is 0.1pF except for L8 and L3, where it is 0.4pF.

The master is selected by placing TRMPWR on MSTR/SLV and the terminator enabled by grounding DISCNCT, enabling the 1.3V regulator. The master is the only terminator connected directly to DIFSENS bus line, all the other terminators receive the mode signal by connecting the DIFFB pins together.

Note: The Master/Slave function will not be on future terminators.

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Multimode SCSI 9 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD) and Ultra3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF
- Master/Slave Input
- Supports Active Negation
- 3pF Channel Capacitance

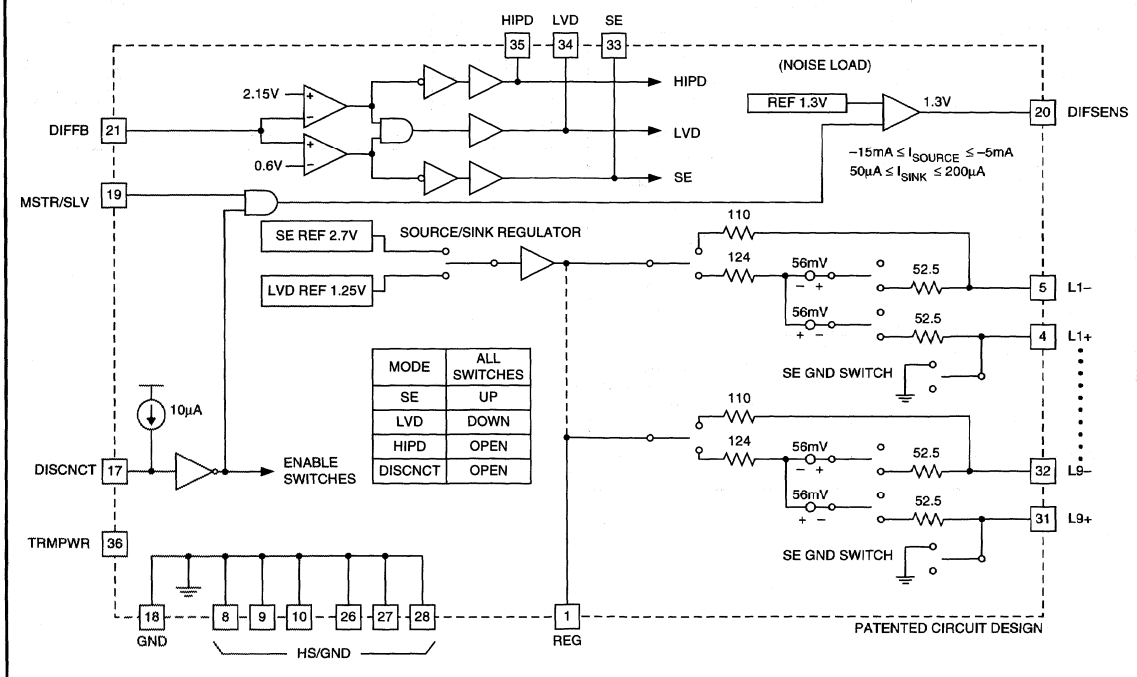
DESCRIPTION

The UCC5630A Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5630A can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5630A detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5630A is offered in a 36 pin SSOP package, as well as a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



Note: Indicated pinout is for 36 pin SSOP package.

ABSOLUTE MAXIMUM RATINGS

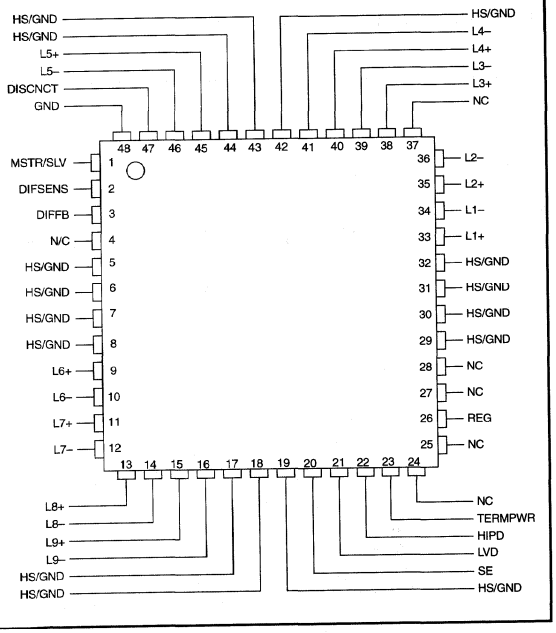
TRMPWR Voltage 6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Power Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are with respect to pin 18. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

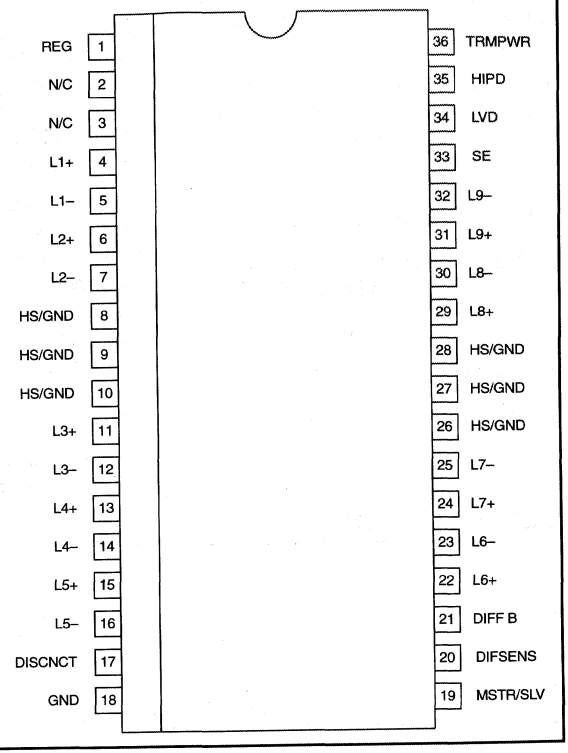
TRMPWR Voltage . . . . . 2.7V to 5.25V

LQFP-48 (Top View)
FQP Package



CONNECTION DIAGRAM

QSOP-36 (Top View)
MWP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode		13	20	mA
	SE Mode		1.6	10	mA
	Disabled Terminator		250	400	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG}= 0V	–600	–420	–225	mA
1.25V Regulator Sink Current	V_{REG}= 3.3V	100	180	420	mA
2.7V Regulator	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG}= 0V	–600	–420	–225	mA
2.7V Regulator Sink Current	V_{REG}= 3.3V	100	180	420	µA
Diff Sense Driver (DIFSENS) Section					
1.3V DIFSENS Output	DIFSENS	1.2	1.3	1.4	V
1.3V DIFSENS Source Current	$V_{DIFSENS}$ = 0V	–15		–5	mA
1.3V DIFSENS Sink Current	$V_{DIFSENS}$ = 2.75V	50		200	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedence	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance	$Z = {(VL_X - 0.2V)}/{IL_X}$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–25.4	–24	–21	mA
	Signal Level 0.5V	–22.4		–18	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I= 10mA		20	60	Ω
Disconnect (DISCNCT) and Diff Buffer (DIFFB) Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current		–30	10		µA
DIFFB Single Ended to LVD Threshold		0.5		0.7	V
DIFFB LVD to HPD Threshold		1.9		2.4	V
DIFFB Input Current		–10		10	µA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold		0.8		2	V
MSTR/SLV Input Current		–30		30	µA
Status Bits (SE, LVD, HIPD) Output Section					
I_{SOURCE}	V_{LOAD} = 2.4V		–8.7	–4	mA
I_{SINK}	V_{LOAD} = 0.5V	3	6		mA
	V_{LOAD} = 0.4V	2	5		mA

Note 1: *Guaranteed by design. Not 100% tested in production.*

Note 2: $Z_{CM} = \dfrac{1.2V}{I_{(V_{CM}+0.6V)} - I_{(V_{CM}-0.6V)}}$;

Where VCM = Voltage measured with L+ tied to L– and zero current applied;

Note 3: *VL_x= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.*
IL_x= Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Input pin for the comparators that select SE, LVD, or HIPD modes of operation. This pin should be decoupled with a 0.1µF capacitor to ground and then coupled to the DIFSENS pin through a 20kΩ resistor.

DIFSENS: Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

DISCNCT: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to activate the terminator or open pin to disable the terminator.

HIPD: TTL compatible status bit. This output pin is high when a high voltage differential device is detected on the bus.

HS/GND: Heat sink ground pins. These should be connected to large area PC board traces to increase the power dissipation capability.

GND: Power Supply return.

L1– thru L9–: Termination lines. These are the active lines in SE mode and are the negative lines for LVD mode. In HIPD mode, these lines are high impedance.

L1+ thru L9+: Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD mode. In HIPD mode, these lines are high impedance.

MSTR/SLV: If the terminator is enabled, this input pin enables / disables the DIFSENS driver, when connected to TRMPWR or ground respectively. When the terminator is disabled, the DIFSENS driver is off, independent of this input.

LVD: TTL compatible status bit. This output pin is high when the SCSI bus is in LVD mode.

REG: Regulator output bypass pin. This pin must be connected to a 4.7µF capacitor to ground.

SE: TTL compatible status bit. This output pin is high when the SCSI bus is in SE mode.

TRMPWR: 2.7V to 5.25V power input pin.

APPLICATION INFORMATION

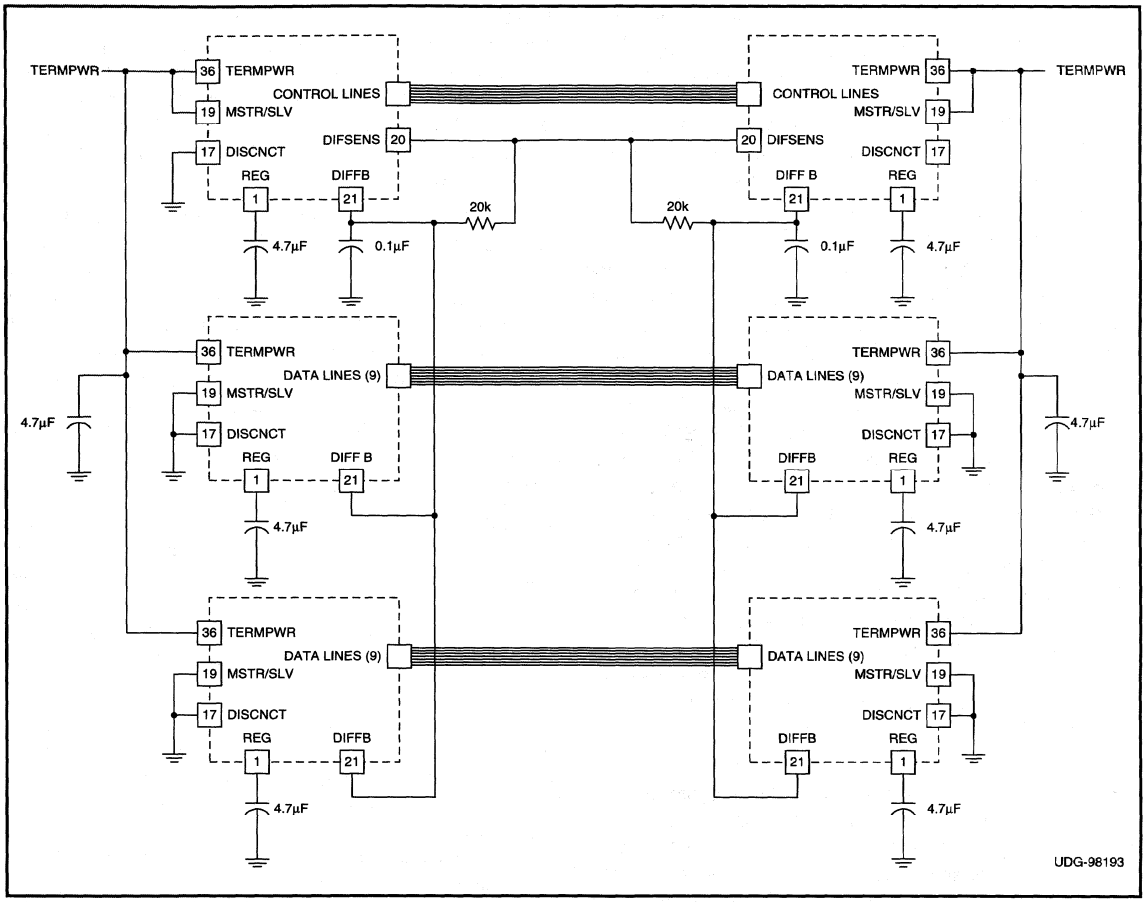


Figure 2. Application diagram.

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5630A is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) devices might coexist. The UCC5630A has both SE and LVD termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5630A DIFSENS drivers will try to deliver 1.3V to the DIFSENS line. If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5630A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

APPLICATION INFORMATION (cont.)

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termination for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is SE. Between 0.7V and 1.9V, the termination network switches to LVD, and above 2.4V is HVD, causing the terminators to disconnect from the bus. The thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5630A multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. A MSTR/SLV input pin is provided to disable the other two. The "master" part must have its' MSTR/SLV pin connected to TRMPWR and the two "slave" parts must have the MSTR/SLV inputs grounded. Only the "master" is connected directly to the SCSI bus DIFSENS line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems, with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3916 is recommended in place of the fuse and diode. The UCC3916's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2 and Ultra3 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5630A is offered in a 36 pin SSOP and a 48 lead LFQP. Both packages include heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. All of the HS/GND pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

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UNITRODE

ADVANCE INFORMATION

Multi-mode (LVD/SE) SCSI 9 Line Terminator w/ 2.85V Regulator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3 SPI, Ultra Fast-20, Ultra-2 (SPI-2 LVD) and Ultra 3 Standards
- 2.7V to 5.25V Termpwr Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and

DESCRIPTION

The UCC5632 Multi-mode SCSI Terminator, both Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for Ultra-2 (Fast-40) and Ultra-3 (Fast-80), but has the potential of speeds up to Fast-320.

The UCC5630 cannot be used with SCSI differential EIA485, it will shutdown when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD SCSI or single ended and the bias voltage, current and power are also different for EIA485 differential.

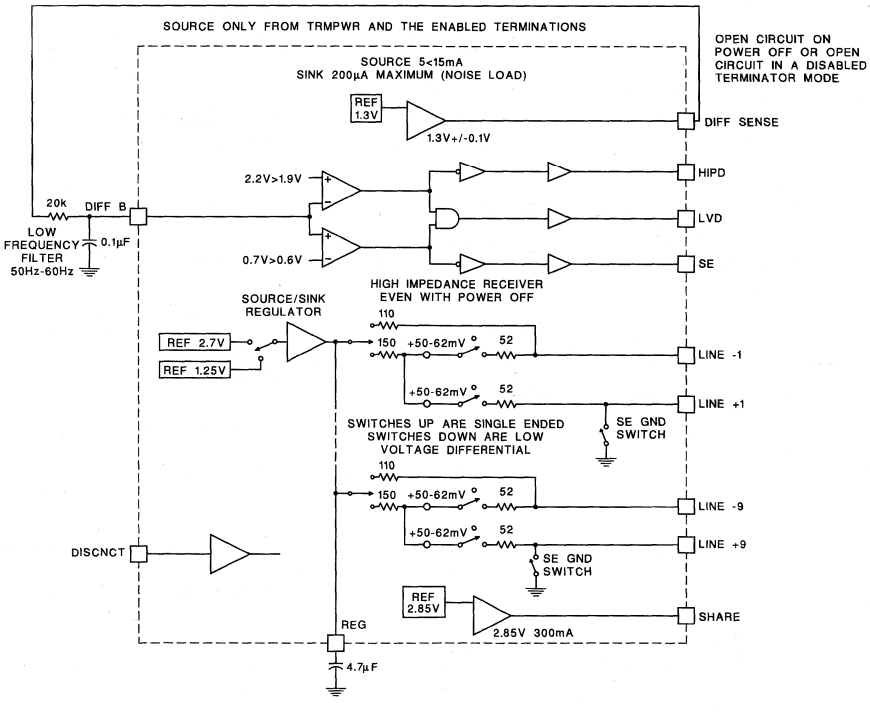
ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage ..... +6V
Signal Line Voltage..... 0V to TERMPWR
Package Power Dissipation 2W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage 2.7Vto 5.25V

BLOCK DIAGRAM



Circuit Design Patented

3/97

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UNITRODE

Multimode SCSI 15 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra 2 (SPI-2 LVD) and Ultra 3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF.

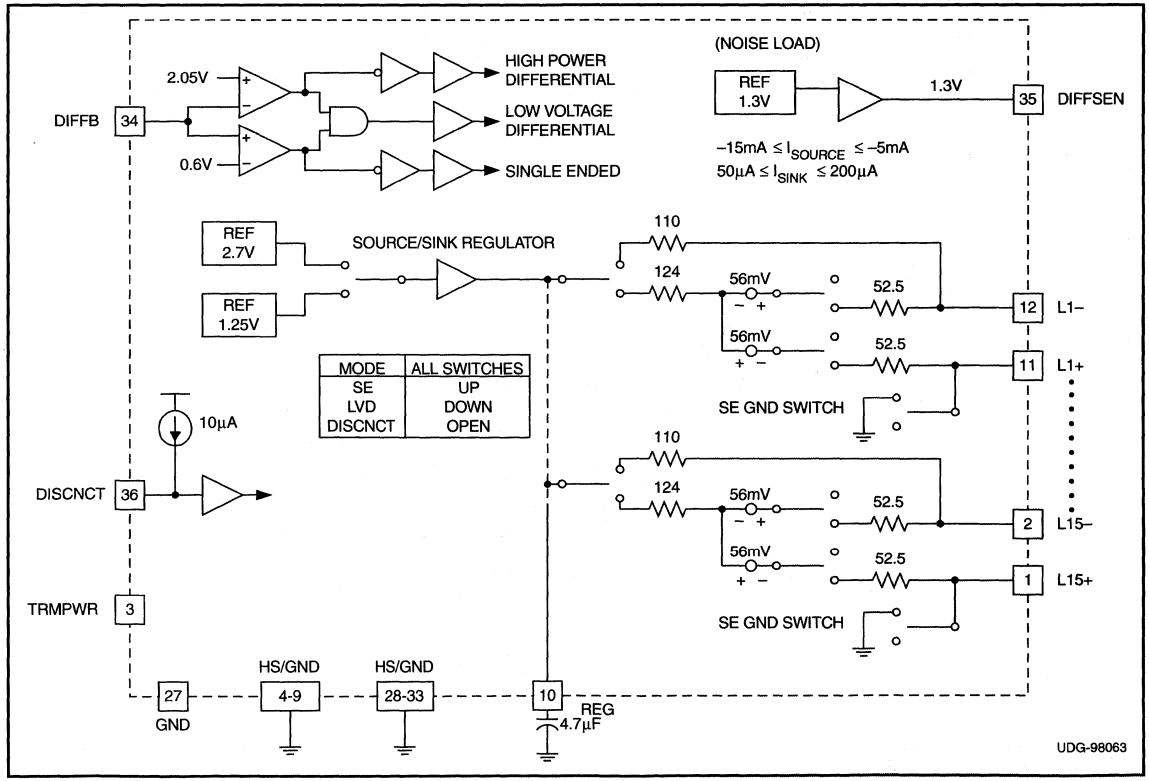
DESCRIPTION

The UCC5638 Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5638 can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5638 detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5638 is offered in a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Recommended Operating Conditions . . . . . 2.7V to 5.25V

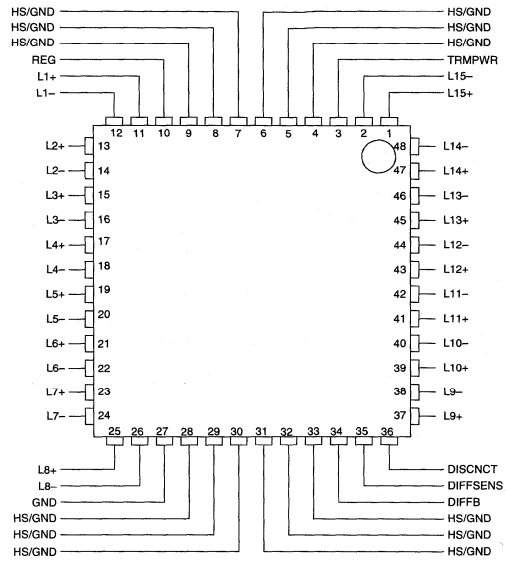
Currents are positive into negative out of the specified terminal.
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 2.7V to 5.25V
Temperature Ranges . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

(TOP VIEW)
FQP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode		20	25	mA
	SE Mode		1.6	10	mA
	Disabled Terminator		250	400	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
1.25V Regulator Sink Current	V_{REG}= 3.3V	170	300	700	mA
1.3V Regulator	Diff Sense	1.2	1.3	1.4	V
1.3V Regulator Source Current	V_{REG}= 0V	–15		–5	mA
1.3V Regulator Sink Current	V_{REG}= 3.3V	50		200	µA
2.7V Regulator	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
2.7V Regulator Sink Curren	V_{REG}= 3.3V	170	300	700	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedence	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Single Ended Termination Section					
Impedance	$Z = {(VL_X - 0.2V)}/{IL_X}$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–21	–24	–25.4	mA
	Signal Level 0.5V	–18		–22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I= 10mA		20	60	Ω
Disconnect and Diff Buffer Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			10	30	µA
Diff Buffer Single Ended to LVD Threshold		0.5		0.7	V
Diff Buffer LVD to HPD Threshold		1.9		2.2	V
DIFFB Input Current		–10		10	µA

Note 1: *Guaranteed by design. Not 100% tested in production.*

Note 2: *Line+ (positive) tied to Line– (negative);* $\frac{I_{(VCM\,max)} - I_{(VCM\,min)}}{1.2V}$

Note 3: *VL_X= Output voltage for each terminator minus output pin (L1– through L15–) with each pin unloaded.*
IL_X = Output current for each terminator minus output pin (L1– through L15–) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Diff sense filter pin should be connected at a 0.1µF capacitor.

DIFFSENS: The SCSI bus Diff Sense line to detect what types of devices are connected to the SCSI bus.

DISCNCT: Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.

LINE*n*–: Signal line active line for single ended or negative line in differential applications for the SCSI bus.

LINE*n*+: Ground line for single ended or positive line for differential applications for the SCSI bus.

REG: Regulator bypass pin, must be connected to a 4.7µF capacitor.

TRMPWR: V_{IN} 2.7V to 5.25V supply.

Note: *In Disconnect Mode, the comparitor set powers down for low idle current.*

APPLICATION INFORMATION

The UCC5638 is a Multi-mode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the "diff sense" signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. A LVD or multi-mode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If a HVD device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5V is single ended, between 0.7V and 1.9V is LVD and above 2.2V is HVD.

In the single ended mode, a multi-mode terminator has a 110Ω terminating resistor connected to a 2.7V termination voltage regulator. The 2.7V regulator is used on all Unitrode terminators designed for 3.3V systems. This requires the terminator to operate in specification down to 2.7V TRMPWR voltage to allow for the 3.3V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD or disconnect mode. The device requirements call for 0.5pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

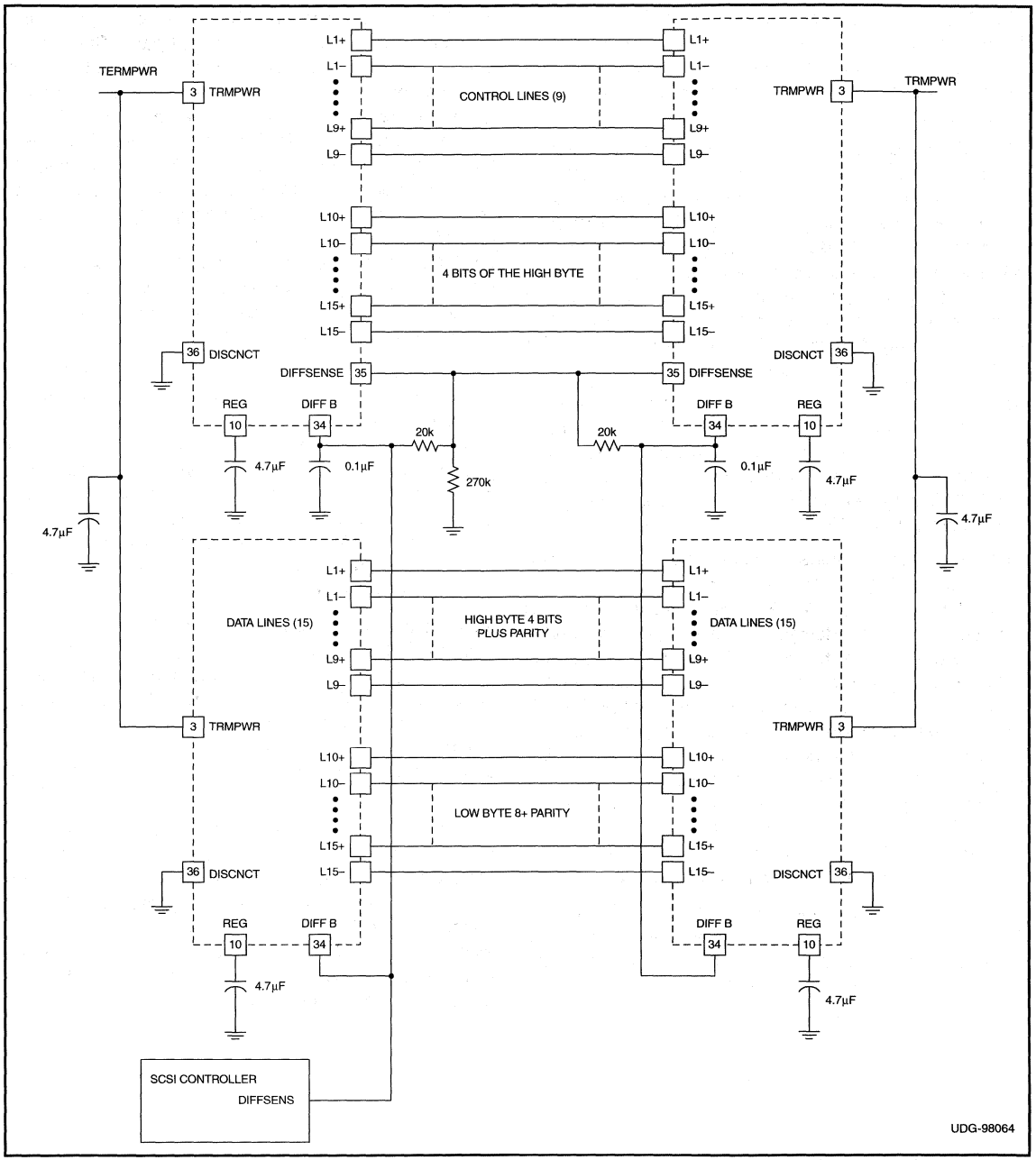
Layout is very critical for Ultra 2 and Ultra 3 systems. Multi-layer boards need to adhere to the 120Ω impedance standard, including connector and feed-through. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between the runs within a pair, and a minimum of 8 mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems.

Capacitance balance is critical for Ultra 2 and Ultra 3. The balance capacitance standard is 0.5pF per line with the balance between pairs of 2pF. The components are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multi-mode terminators need to consider power dissipation; the UCC5638 is offered in a power package with heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

In 3.3V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3V battery systems normally have a 10% tolerance. The UCC3912 is 150mV drop under LVD loads, allowing 150mV drop in the cable system. All Unitrode LVD and multi-mode terminators are designed for 3.3V systems, operating down to 2.7V.

TYPICAL APPLICATION



Note: *A 220k resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFFSENS ties to the DIFFB pin on the terminators, only one RC network should be on a device.*

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Multimode SCSI 15 Line Terminator with Reverse Disconnect

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3, SPI, Ultra (Fast-20), Ultra2 (SPI-2 LVD) and Ultra3 Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF.

DESCRIPTION

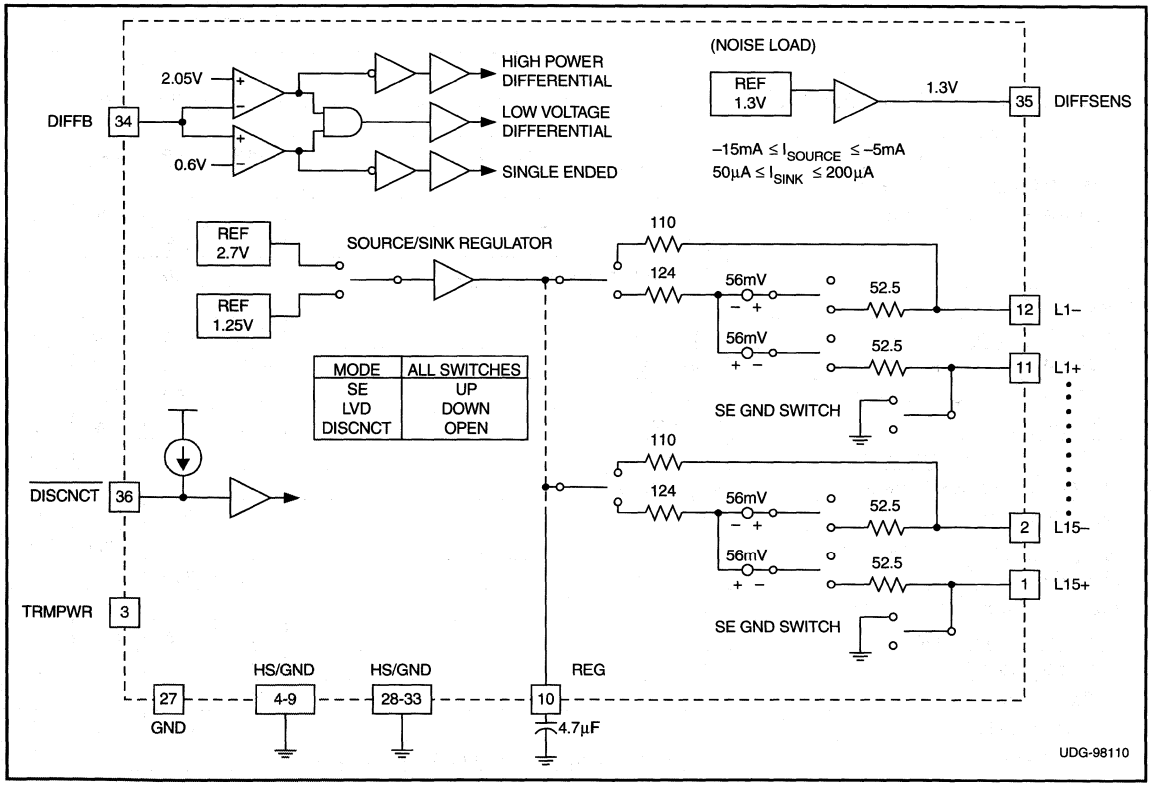
The UCC5639 Multimode SCSI Terminator provides a smooth transition into the next generation of the SCSI Parallel Interface (SPI-2). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5639 can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5639 detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5639 is offered in a 48 pin LQFP package for a temperature range of 0°C to 70°C.

3

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to TRMPWR
Package Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Recommended Operating Conditions . . . . . 2.7V to 5.25V

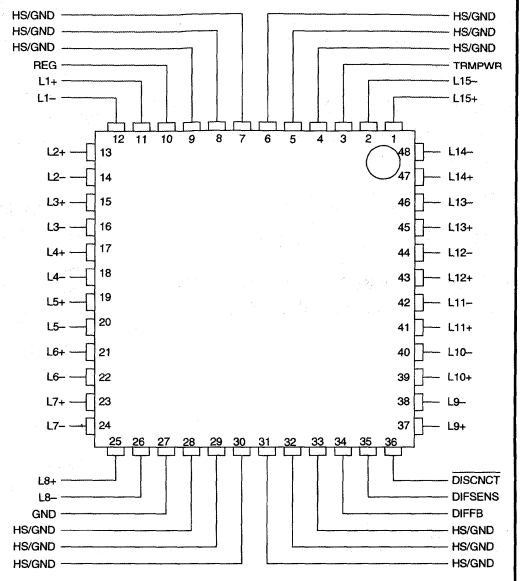
Currents are positive into negative out of the specified terminal.
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 2.7V to 5.25V
Temperature Ranges . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

(TOP VIEW)
FQP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode		20	25	mA
	SE Mode		1.6	10	mA
	Disabled Terminator		250	400	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
1.25V Regulator Sink Current	V_{REG}= 3.3V	170	300	700	mA
1.3V Regulator	DIFSENS	1.2	1.3	1.4	V
1.3V Regulator Source Current	V_{REG}= 0V	–15		–5	mA
1.3V Regulator Sink Current	V_{REG}= 3.3V	50		200	µA
2.7V Regulator	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG}= 0V	–375	–700	–1000	mA
2.7V Regulator Sink Curren	V_{REG}= 3.3V	170	300	700	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedence	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Single Ended Termination Section					
Impedance	$Z = {(VL_X - 0.2V)}/{IL_X}$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–21	–24	–25.4	mA
	Signal Level 0.5V	–18		–22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I= 10mA		20	60	Ω
Disconnect and Diff Buffer Input Section					
$\overline{\text{DISCNCT}}$ Threshold		0.8		2.0	V
$\overline{\text{DISCNCT}}$ Input Current			10	30	µA
Diff Buffer Single Ended to LVD Threshold		0.5		0.7	V
Diff Buffer LVD to HPD Threshold		1.9		2.2	V
DIFFB Input Current		–10		10	µA

Note 1: *Guaranteed by design. Not 100% tested in production.*

Note 2: $Z_{CM} = \dfrac{1.2V}{\left[I_{(VCM+0.6V)} - I_{(VCM-0.6V)}\right]}$ *where VCM=voltage measured with L+ tied to L– and zero current applied*

Note 3: *VL_X= Output voltage for each terminator minus output pin (L1– through L15–) with each pin unloaded.*
IL_X = Output current for each terminator minus output pin (L1– through L15–) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Diff sense filter pin should be connected at a 0.1µF capacitor.

DIFFSENS: The SCSI bus Diff Sense line to detect what types of devices are connected to the SCSI bus.

$\overline{\text{DISCNCT}}$: Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin high enables the terminator.

LINE*n*–: Signal line active line for single ended or negative line in differential applications for the SCSI bus.

LINE*n*+: Ground line for single ended or positive line for differential applications for the SCSI bus.

REG: Regulator bypass pin, must be connected to a 4.7µF capacitor.

TRMPWR: V_{IN} 2.7V to 5.25V supply.

APPLICATION INFORMATION

The UCC5639 is a Multi-mode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the "diff sense" signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. A LVD or multi-mode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If a HVD device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5V is single ended, between 0.7V and 1.9V is LVD and above 2.2V is HVD.

In the single ended mode, a multi-mode terminator has a 110Ω terminating resistor connected to a 2.7V termination voltage regulator. The 2.7V regulator is used on all Unitrode terminators designed for 3.3V systems. This requires the terminator to operate in specification down to 2.7V TRMPWR voltage to allow for the 3.3V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD or disconnect mode. The device requirements call for 0.5pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

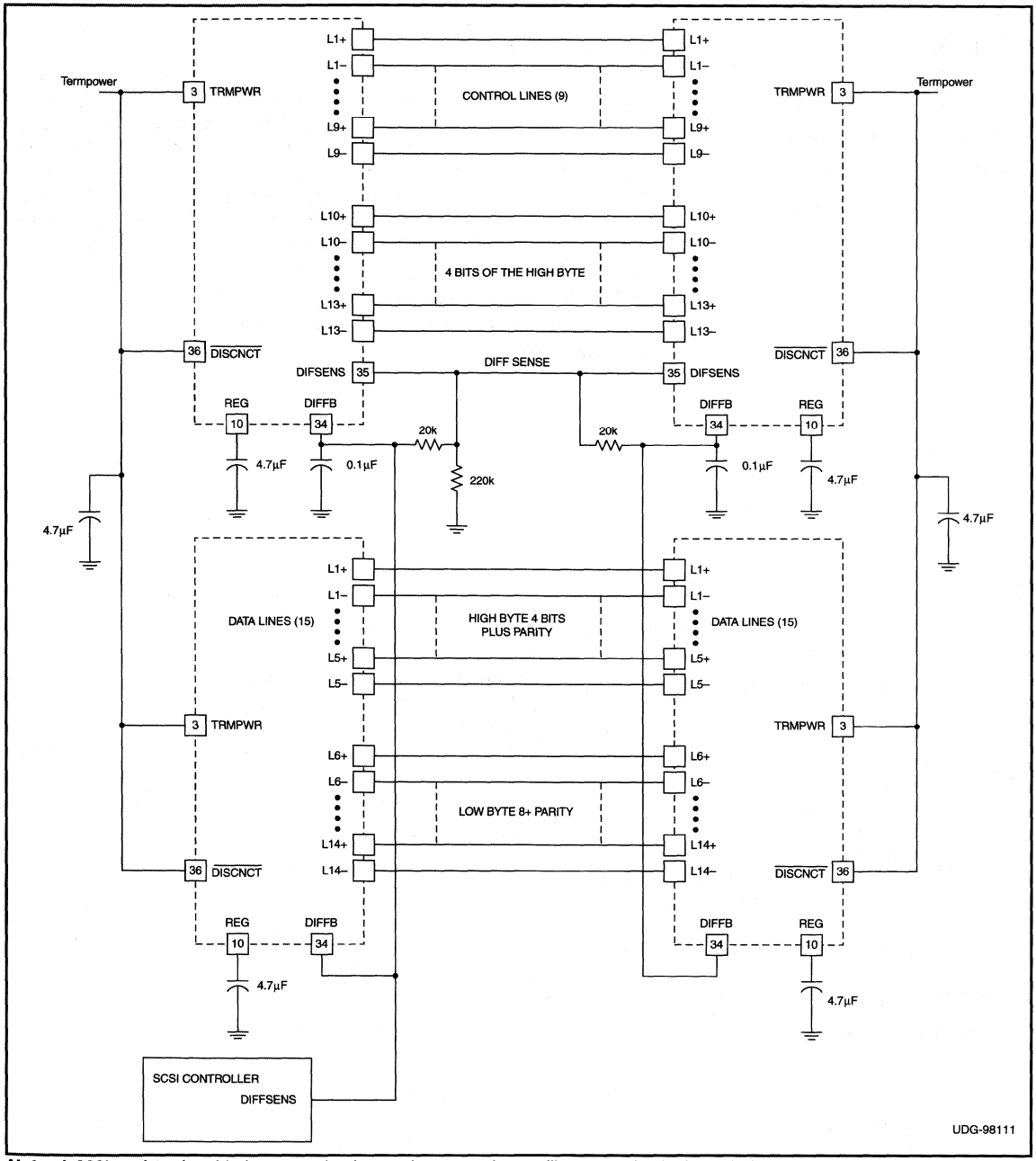
Layout is very critical for Ultra2 and Ultra3 systems. Multi-layer boards need to adhere to the 120Ω impedance standard, including connector and feed-through. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between the runs within a pair, and a minimum of 8 mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems.

Capacitance balance is critical for Ultra2 and Ultra3. The balance capacitance standard is 0.5pF per line with the balance between pairs of 2pF. The components are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multi-mode terminators need to consider power dissipation; the UCC5639 is offered in a power package with heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

In 3.3V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3V battery systems normally have a 10% tolerance. The UCC3912 is 150mV drop under LVD loads, allowing 150mV drop in the cable system. All Unitrode LVD and multi-mode terminators are designed for 3.3V systems, operating down to 2.7V.

TYPICAL APPLICATION



Note: *A 220k resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFFSENS ties to the DIFFB pin on the terminators, only one RC network should be on a device.*

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Low Voltage Differential (LVD) SCSI 9 Line Terminator

FEATURES

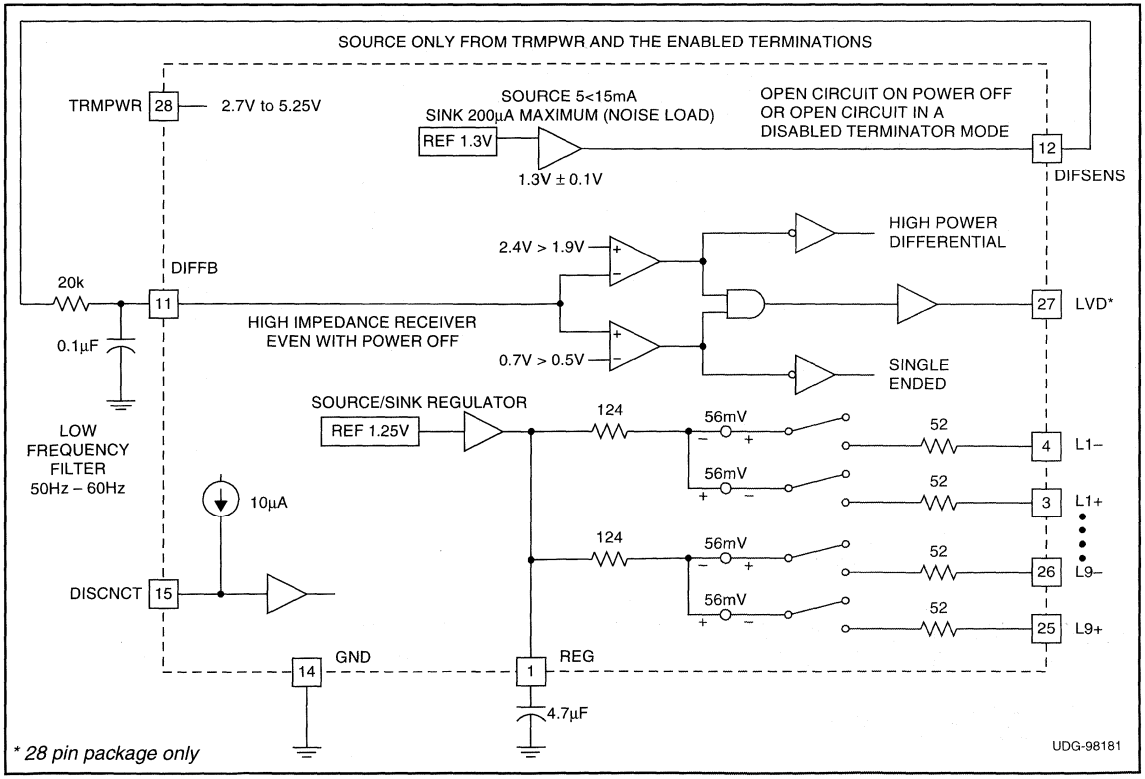
- First LVD only Active Terminator
- Meets SCSI SPI-2 Ultra2 (Fast-40) and Ultra3 (Fast-80) Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias

DESCRIPTION

The UCC5640 is an active terminator for Low Voltage Differential (LVD) SCSI networks. This LVD only design allows the user to reach peak bus performance while reducing system cost. The device is designed as an active Y-terminator to improve the frequency response of the LVD Bus. Designed with a 1.5pF channel capacitance, the UCC5640 allows for minimal bus loading for a maximum number of peripherals. With the UCC5640, the designer will be able to comply with the Fast-40 SPI-2 and Fast-80 SPI-3 specifications. The UCC5640 also provides a much-needed system migration path for ever improving SCSI system standards. This device is available in the 24 pin TSSOP and 28 pin TSSOP for ease of layout use.

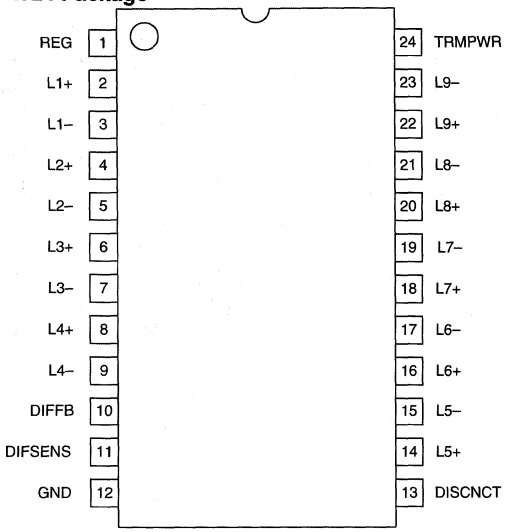
The UCC5640 is not designed for use in single ended or high voltage differential systems.

BLOCK DIAGRAM

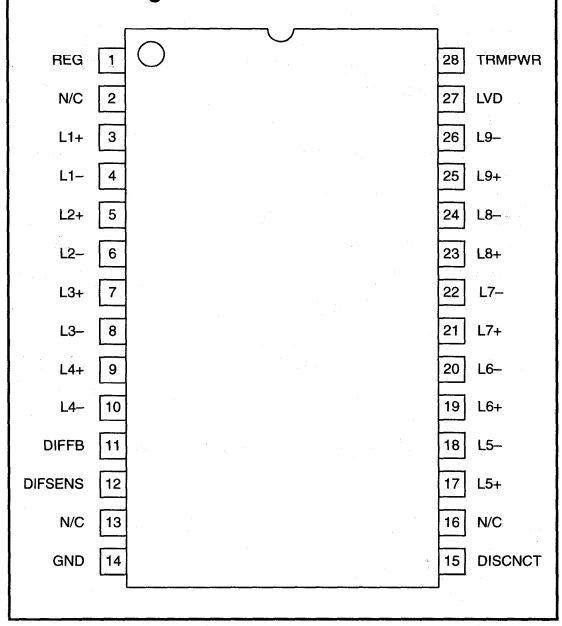


CONNECTION DIAGRAMS

TSSOP-24 (Top View)
PW24 Package



TSSOP-28 (Top View)
PW28 Package



ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to 3.6V
Package Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into negative out of the specified terminal. consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . . 2.7V to 5.25V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications apply for T_A = 0°C to 70°C, TRMPWR = 3.3V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	No Load			25	mA
	Disabled Terminator			400	µA
TRMPWR Voltage		2.7		5.25	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications apply for T_A = 0°C to 70°C, TRMPWR = 3.3V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
1.25V Regulator	DIFSENS connected to DIFFB	1.15	1.25	1.35	V
1.25V Regulator Source Current	DIFSENS connected to DIFFB		–100	–80	mA
1.25V Regulator Sink Current	DIFSENS connected to DIFFB	80	100		mA
1.3V Regulator	DIFFB connected to GND	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFSENS to GND	–15		–5	mA
1.3V Sink Current	DIFSENS to 3.3V	50		200	µA
Differential Termination Section					
Differential Impedance	–2.5mA to 4.5mA	100	105	110	Ω
Common Mode Impedance	L+ connected to L–	110	150	165	Ω
Differential Bias Voltage	No load, L+ or L–	100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Leakage, Disconnect	DISCNCT, TRMPWR = 0 to 5.25V, V_{LINE} = 0.2 to 5.25V		10	400	nA
Output Capacitance	Single ended measurement to ground (Note 1)			3	pF
Low Voltage Differential (LVD) Status Bit Section					
I_{SOURCE}	V_{LOAD} = 2.4V		–6	–4	mA
I_{SINK}	V_{LOAD} = 0.4V	2	5		mA
Disconnect & Differential Sense Input Section					
DISCNCT Threshold		0.8		2	V
Input Current	At 0V and 3.3V	–30	–10		µA
Differential Sense Signal Ended to LVD Threshold		0.5		0.7	V
Differential Sense LVD to HPD Threshold		1.9		2.4	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTION

DIFFB: Differential sense filter pin should be connected to a 0.1µF capacitor and 20kΩ resistor to Diff Sense.

DIFSENS: The SCSI bus differential sense line to detect what type of devices are connected to the SCSI Bus.

DISCNCT: Disconnect pin shuts down the terminator when it is not at the end of the bus.

GND: Ground.

L*n* –: Signal active line for single ended or negative line in differential applications for the SCSI Bus.

L*n* +: Ground line for single ended or positive line for differential applications for the SCSI Bus.

LVD: (28 pin package only) Indicates that the bus is in LVD mode.

REG: Regulator bypass; must be connected to a 4.7µF capacitor to ground.

TRMPWR: V_{IN} 2.7V to 5.25V supply.

APPLICATION INFORMATION

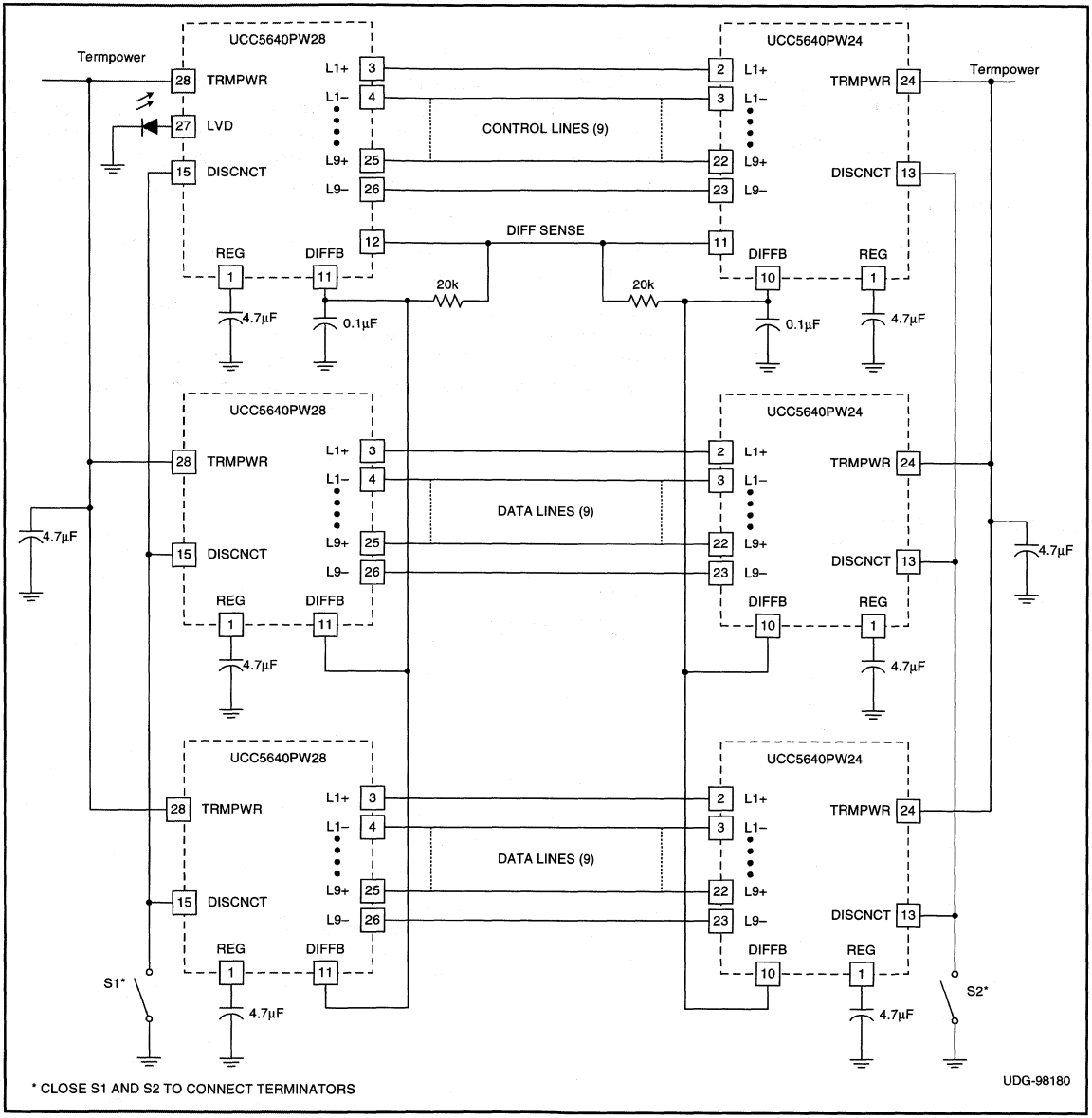


Figure 1. Application diagram.

UNITRODE CORPORATION
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Low Voltage Differential (LVD) SCSI 9 Line Terminator

FEATURES

- SCSI SPI-2 LVD SCSI 9 Line Low Voltage Differential Termination
- Meets SCSI SPI-2 Ultra2 (Fast-40) and Ultra3 (Fast-80) Standby
- 2.7V to 5.25V Operation
- Differential Failsafe Bias

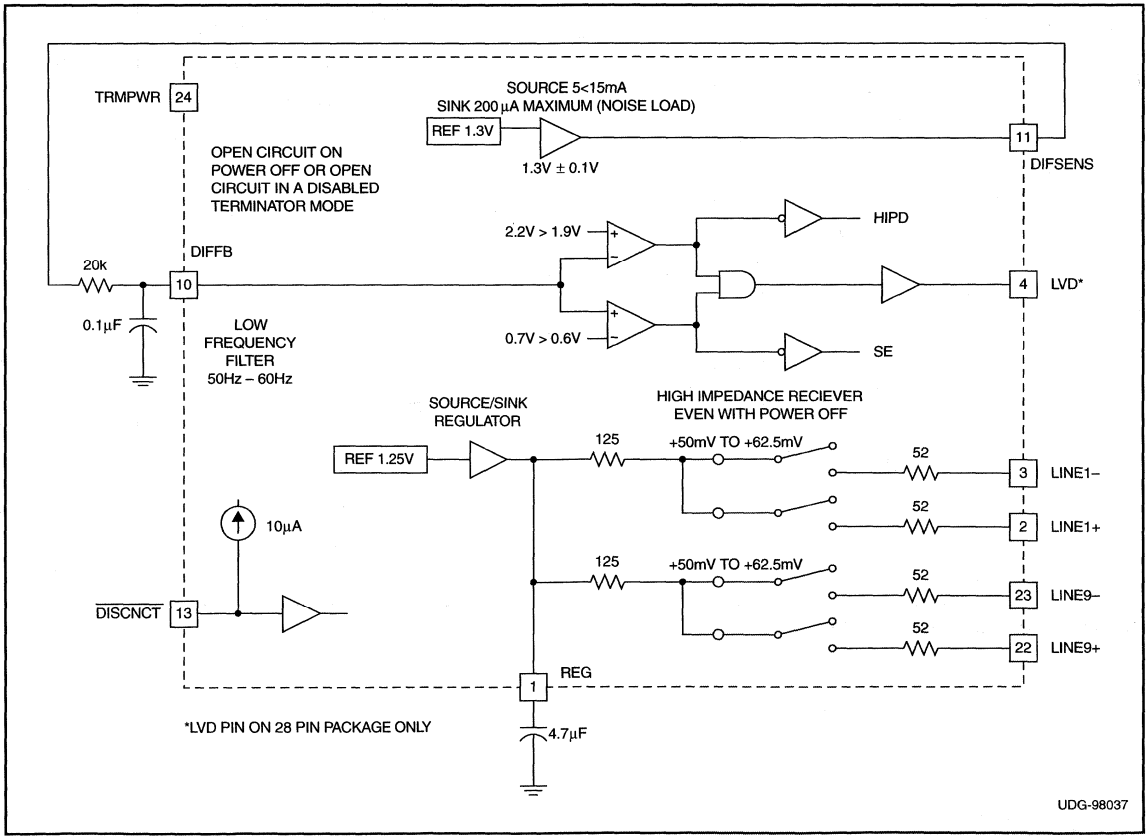
DESCRIPTION

The UCC5641 Low Voltage differential terminator is a low voltage differential terminator only for SCSI Parallel interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers.

Low Voltage differential is specified for FAST-40 and FAST-80, but has the potential of speeds up to FAST-320.

The UCC5641 can not be used with SCSI differential EIA485, it will shut down when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD SCSI or single-ended and the bias voltage, current and power are also different for EIA485 differential.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

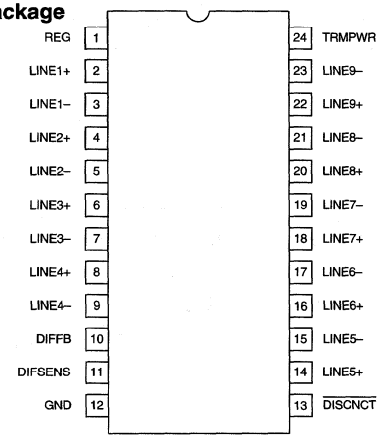
TRMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to TERMPWR
Package Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . . 2.7V to 5.25V

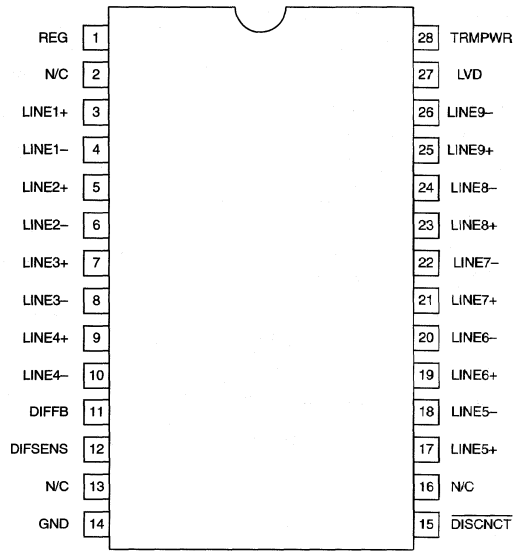
Currents are positive into negative out of the specified terminal. consult Packaging Section of Databook for thermal limitations and considerations of package.

TSSOP-24 (Top View)
PW Package



CONNECTION DIAGRAMS

TSSOP-28 (Top View)
PW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications apply for T_A = 0°C to 70°C, TRMPWR = 3.3V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	No Load			25	mA
	Disabled Terminator			200	µA
TRMPWR Voltage		2.7		5.25	V
Regulator Section					
1.25V Regulator	DIFSENS connected to DIFFB	1.15	1.25	1.35	V
1.25V Regulator Source Current	DIFSENS connected to DIFFB	–80	–100		mA
1.25V Regulator Sink Current	DIFSENS connected to DIFFB	80	100		mA
1.25V Current Limit	DIFSENS connected to DIFFB	300			mA
1.3V Regulator	DIFFB connected to GND	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFFB to GND	–5		–15	mA
1.3V Sink Current	DIFFB to GND	50		200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications apply for T_A = 0°C to 70°C, TRMPWR = 3.3V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Termination Section					
Differential Impedance	–2.5mA to 4.5mA	100	105	110	Ω
Common Mode Impedance	LINE+ connected to LINE–	110	150	165	Ω
Differential Bias Voltage	Drivers Tristated	100		125	mV
Common Mode Bias			1.25		V
Output Leakage, Disconnect	$\overline{\text{DISCNCT}}$, TRMPWR = 0 to 5.25V, V_{LINE} = 0.2 to 2.5V		10	400	nA
Output Capacitance	Single ended measurement to ground (Note 1)			3	pF
Disconnect & Differential Sense Input Section					
$\overline{\text{DISCNCT}}$ Threshold		0.8		2	V
Input Current	At 0V and 3.3V		10	30	µA
Differential Sense Signal Ended Threshold		0.6		0.7	V
Differential Sense LVD Threshold		1.9		2.2	V
Differential HP Differential Threshold		2.2			V

Note 1: Guaranteed by design. Not 100% tested in production.

TRMPWR: V_{IN} 2.7 to 5.25 Volts supply.

DIFSENS: The SCSI bus diff sense line to detect what type of devices are connected to the SCSI bus.

$\overline{\text{DISCNCT}}$: Disconnect pin shuts down the terminator when it is not at the end of the bus.

DIFFB: Diff Sense filter pin should be connected to a 0.1µF Capacitor.

REG: Regulator bypass pin, must be connected to a 4.7µF Capacitor.

LINE*n*–: Signal line Active line for single ended or negative line in differential applications for the SCSI Bus.

LINE*n*+: Ground line for single ended or positive line for differential applications for the SCSI Bus.

LVD: Indicates that the bus is in LVD mode regardless of the terminator's connection mode.

APPLICATION INFORMATION

Diff Sense is drivien by only one terminator at each end of the bus. All other terminators receive the mode signal by connecting the DIFFB pins together.

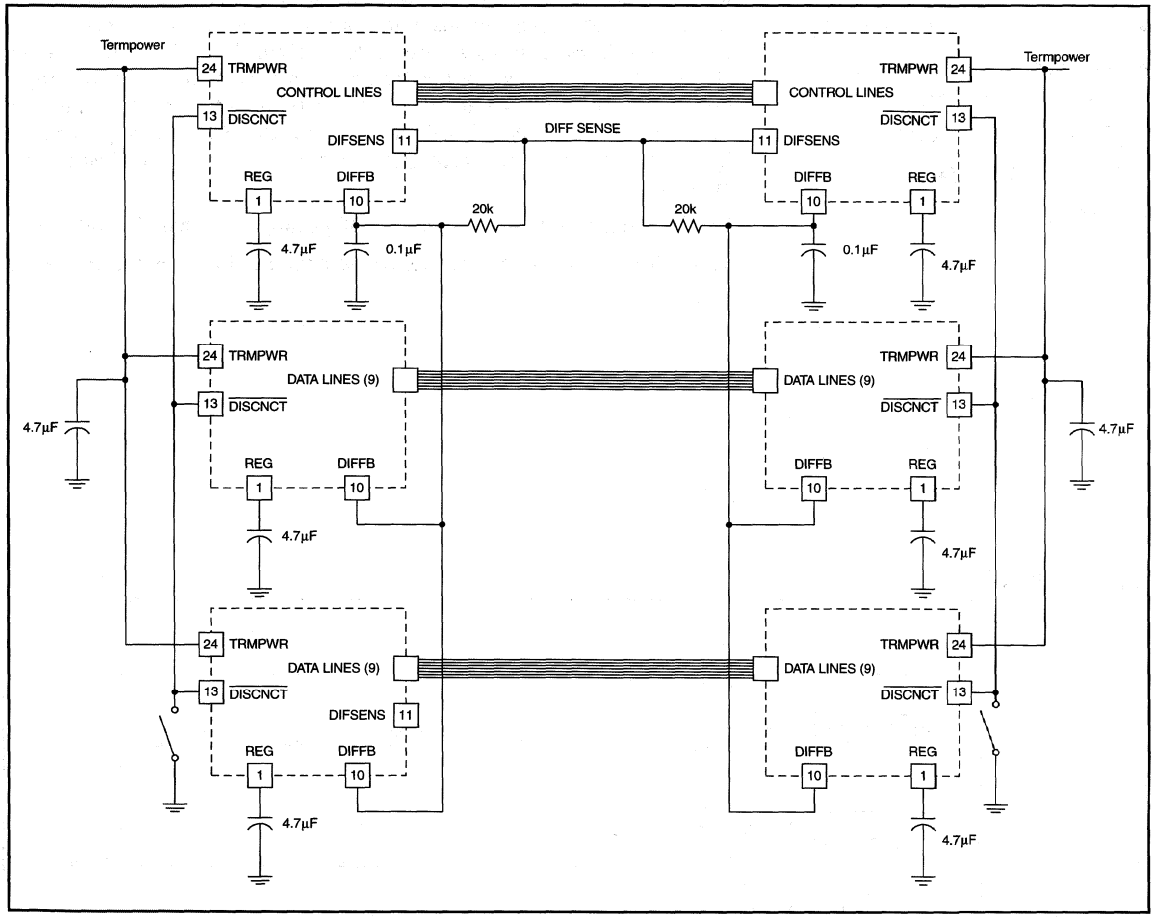


Figure 1. Application Diagram

UDG-97181

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

27 Line LVD SCSI Terminator

ADVANCE INFORMATION

FEATURES

- SCSI SPI-2, SPI-3, 160m Compliance
- Smallest Footprint
- Lowest Channel Capacitance, 2pF
- Less than 0.5pF Capacitance Differential Between Pairs
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- 64 Pin LQFP

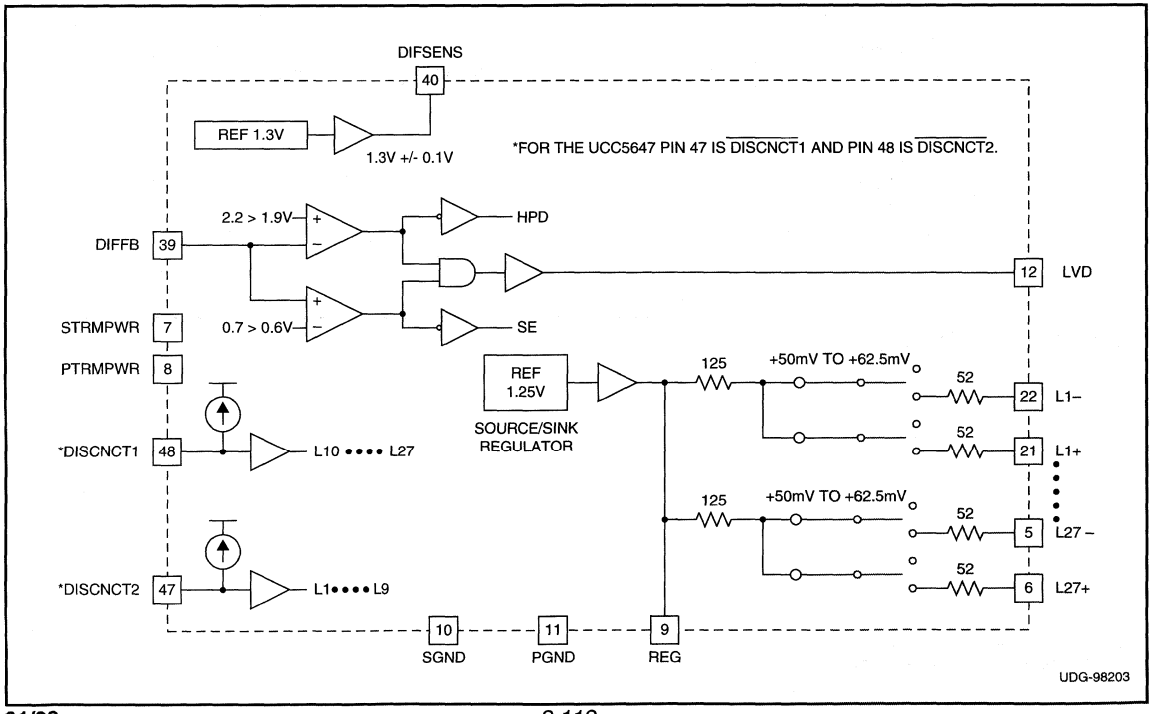
DESCRIPTION

The UCC5646 is a twenty-seven line active terminator for Low Voltage Differential (LVD) SCSI networks. This LVD SCSI only design allows the user to reach peak bus performance, while reducing system cost. The device is designed as an active Y-terminator to improve the frequency response of the LVD SCSI Bus. Designed with a 2pF typical channel capacitance, the UCC5646 allows for minimal bus loading for a maximum number of peripherals. With the UCC5646, the designer will be able to comply with the Ultra2 and Ultra3, 160m specifications. The UCC5646 also provides a much-needed system migration path for the ever improving SCSI system standards.

This device is available in the 64 pin LQF package for ease of layout use.

The UCC5646 is not designed for single ended or high volume differential systems.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR . . . . . -0.3V to 6V
Signal Line Voltage . . . . . –0.3V to TRMPWR
Package Dissipation 1W
Regulator Output Current 0.75A
Storage Temperature . . . . . –55°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10Sec.) . . . . . +300°C

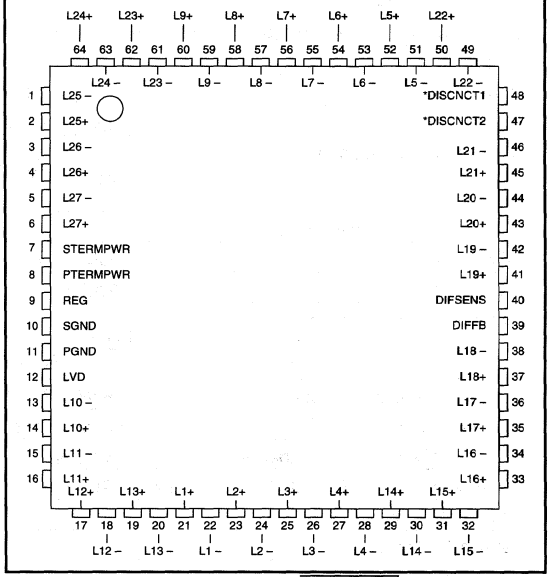
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

RECOMMENDED OPERATING CONDITIONS

TRMPWR . . . . . 2.7V to 5.25V

CONNECTION DIAGRAMS

LQFP-64 (TOP VIEW)
Q Packages



**For the UCC5647, Pin 47 Is $\overline{\text{DISCNCT1}}$ and Pin 48 is DISCNCT2.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications are for TRMPWR = 2.7V to 5.25V, T_A = 0°C to +70°C, DISCNCT1 = DISCNCT2 = 0V for UCC5646 DISCNCT1 = DISCNCT2 = open for UCC5647, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD Mode			65	mA
	Disabled Terminator			200	µA
TRMPWR Voltage		2.7		5.25	V
1.25V Regulator Section					
1.25V Regulator	$-240mA \le I_{REG} \le 240mA$	1.15	1.25	1.35	V
Regulator Source Current	V_{REG}= 0V	–240	–300		mA
Regulator Sink Current	V_{REG}= 3.3V	240	300		mA
1.3V (DIFSENS) Regulator Section					
1.3V Regulator	$-5mA \le I_{DIFSENS} \le 50\mu A$	1.2	1.3	1.4	V
Source Current	$V_{DIFSENS}$ = 0V	–5	–8	–15	mA
Sink Current	$V_{DIFSENS}$ = 3.3V	50		200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications are for TRMPWR = 2.7V to 5.25V, T_A = 0°C to +70°C, DISCNCT1 = DISCNCT2 = 0V for UCC5646 DISCNCT1 = DISCNCT2 = open for UCC5647, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Termination Section (Applies to each line pair 1-27)					
Differential Bias Voltage		100		125	V
$I_{DIFFB(max)}$	V_{DIFFB} = +1V; T_A = 25°C (Note1)	7.955		9	mA
$I_{DIFFB(min)}$	V_{DIFFB} = –1V; T_A = 25°C (Note1)	–10		–11.25	mA
Differential Impedance	$Z_{DIFF} = \left(\frac{V_{DIFF1} - V_{DIFF2}}{7mA}\right)$	100	105	110	Ω
Common Mode Bias Voltage	L+ and L– shorted together	1.15	1.25	1.35	V
ICM(max)	VCM = 2V (Note 3)	2.083		8.75	mA
ICM(min)	VCM = 0.5V (Note 3)	–2.083		–8.75	mA
Common Mode Impedance	$ICM = \frac{1.5V}{(ICM(\max) - ICM(\min))}$	110	140	165	Ω
Output Leakage in Disconnect	TRMPWR = 0V to 5.25V, V_{LINE} = 0.2V to 2.5V		10	400	nA
Output Capacitance	Single Ended measurement to GND (Note 1)			3	pF
Single Ended GND SE Impedance	I = 10mA		20	60	Ω
Disconnect Control (DISCNCT1) or (DISNCNT2) Section					
DISCNCT Threshold		0.8	1.5	2.0	V
DISCNCT Input Current		–10		–30	µA
DIFFB Input Section					
DIFFB SE to LVD Threshold		0.5	0.6	0.7	V
DIFFB LVD Range		0.7		1.9	V
DIFFB LVD to HPD Threshold		1.9	2.05	2.2	V
DIFFB Input Current		–10		10	µA

Note 1: I_{DIFF} = Current into L–, with V_{DIFF} applied to L–with respect to L+.
Note 2: V_{DIFF1} = (VL–) – (VL+) with 2.5mA current sourced applied across L– and L+ (current into L–.)
V_{DIFF2} = (VL–) – (VL+) with 4.5mA current sourced applied across L+ and L– (current into L+.)
Note 3: ICM = Sum of currents into L+ and L–, with VCM applied to both terminals with respect to ground.
Note 4: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

STRMPWR: 2.7 to 5.25 Volts power supply for all circuitry except the 1.25V regulator.

SGND: Ground reference for all circuitry except the 1.25V regulator.

PTRMPWR: 2.7 to 5.25 Volts power supply for the 1.25V regulator.

PGND: Ground reference for the 1.25V regulator.

REG: Output of the internal 1.25V regulator; must be connected to a 4.7µF bypass capacitor.

DIFSENS: Drives the SCSI bus DIFF SENSE line to 1.3V to detect what types of devices are tied to the bus.

DIFFB: DIFF SENSE filter pin. Should be connected to a 0.1uF capacitor to GND and to a 20k resistor to the SCSI bus DIFF SENSE line.

DISCNCT1: Disconnect one controls termination lines 10-27 (control and low byte.)

DISCNCT2: Disconnect two controls termination lines 1-9 (high byte.)

LVD: TTL compatible status bit indicating when Low Voltage Differential voltage is present on DIFFB.

L1– thru L27–: Negative lines for the SCSI bus.

L1+ thru L27+: Positive lines for the SCSI bus.

APPLICATION INFORMATION

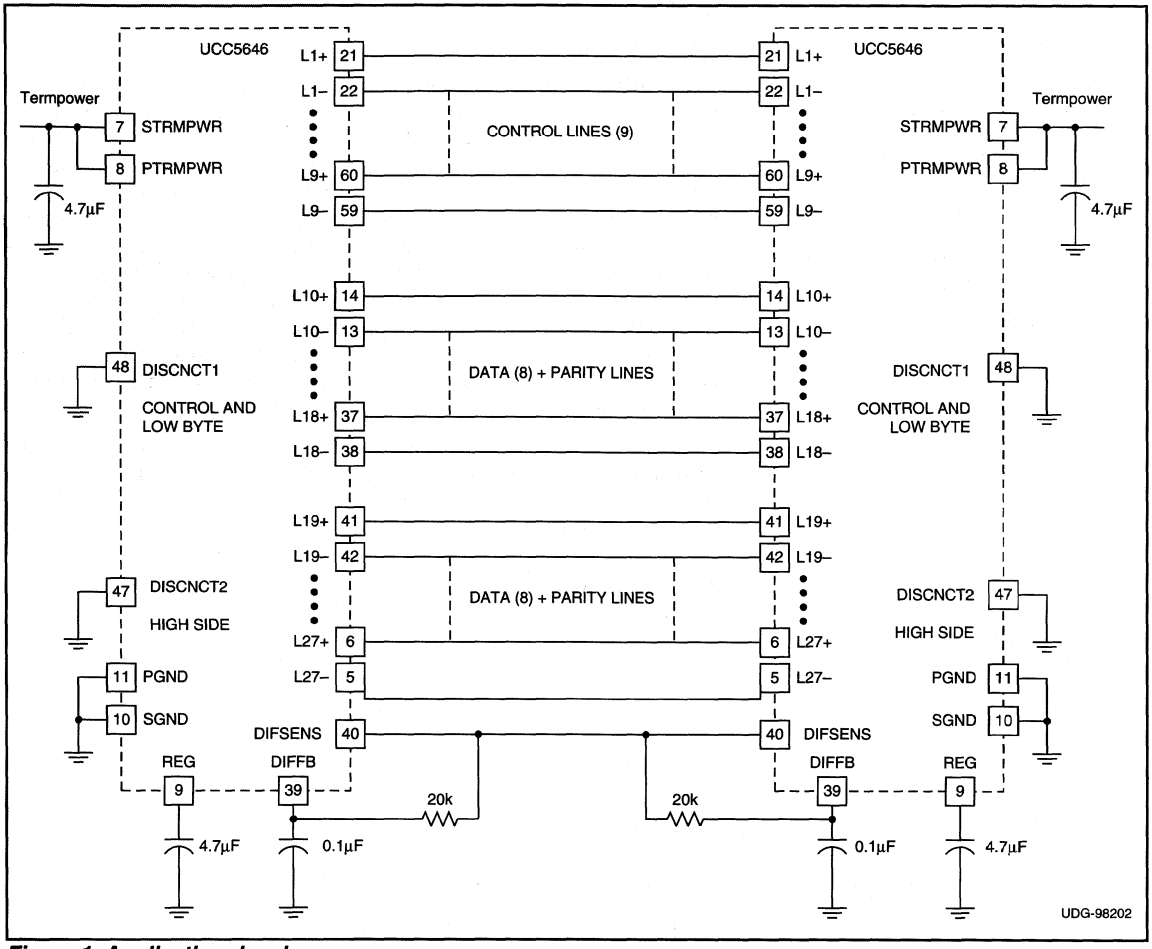


Figure 1. Application drawing.

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UNITRODE

Ethernet Coaxial Impedance Monitor

FEATURES

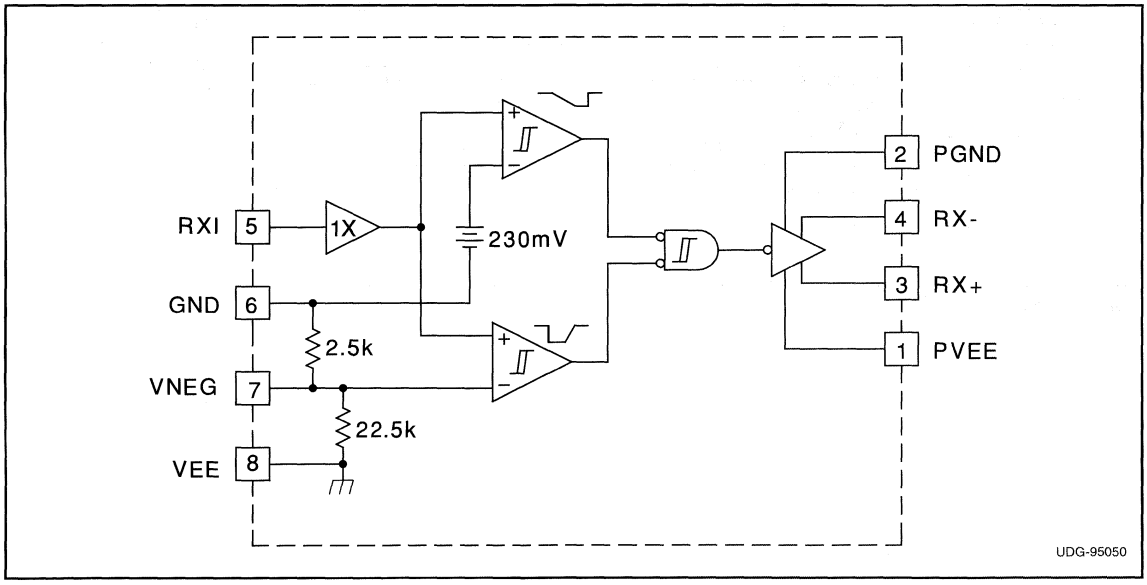
- Compatible with IEEE 802.3 10Base5, 10Base2, and 10BaseT
- Preset and Adjustable Data Thresholds
- Protects DTE from Spurious Data
- Prevents Erroneous Transmission Through Repeaters
- Detects Cable Termination Errors
- Detects Cable Impedance Errors

DESCRIPTION

The UC5661 is a monolithic integrated circuit which functions as an Ethernet Coaxial Impedance Monitor (CIM). This IC is intended to augment the receive (RX) function of IEEE 802.3 Coaxial Transceiver Interface (CTI) circuits. The UC5661 implements a hardware algorithm to detect reflections on the Ethernet coaxial cable or twisted pair which are caused by improper network termination or physical medium damage. If a physical problem is detected, the UC5661, whose receiver outputs operate in parallel with the CTI, immediately squelches the receive data, preventing the propagation of invalid network packets. During ordinary operation, the CIM RX outputs enable at the beginning of the data packet preamble, making it transparent to normal CTI functions. The valid data threshold, although preset for thick and thin-wire Ethernets, may be adjusted with the addition of one or two external resistors to meet 10BaseT requirements.

A secondary system design feature is provided by the UC5661. At the completion of a normal data transmission, the CIM Squelch activates much faster than typical transceiver ICs. The receiver outputs of the UC5661 have been designed to properly terminate the data packet, even with RX data transformers as small as 16µH, possibly allowing for smaller and less expensive system implementations. In these cases, end-of-packet squelch overshoot will be held to less than 100mV.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

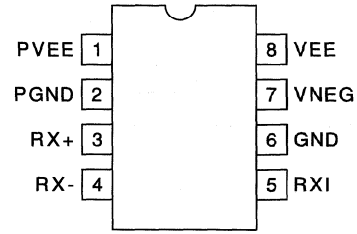
Supply Voltage (PVEE,VEE) . . . . . –15V
Input Voltage (RXI) . . . . . +2V to –10V
Operating Temperature Range . . . . . 0°C to +70°C
Junction Temperature (Note 1) . . . . . +125°C
Storage Temperature Range . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

Note 1: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

CONNECTION DIAGRAMS

DIL-8, (Top View)
J or N, Package



DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, VEE = PVEE = –9.0V, and R_L = 500 ohms, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Outputs Locked or Unlocked, Unloaded		10	20	mA
Input Bias Current	RXI = 0V		2	5	µA
Input Shunt Resistance	RXI = –2V to 0V	0.200	45		MΩ
Input Shunt Capacitance	(Note 1)		3	4	pF
VNEG (Valid Data Reference)	VNEG = open	–980	–900	–830	mV
RX Output Voltage High (Squelch)		–1.2	–0.9	0	V
RX Output Voltage Low (Enable)		–6	–3.7	–3.2	V
Output Short Circuit	RX+ = RX– = 9V	–150			mA
Valid Data Threshold		–980	–900	–830	mV
Data Reflection Threshold		200	230	300	mV

Note 1: Guaranteed by design. Not 100% tested in production.

AC ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, VEE = PVEE = –9.0V, and R_L = 500 ohms, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{EN} RX Enable Delay	See Figures 1, 2		100	400	ns
T_{DIS} RX Disable Delay	See Figures 1, 2	250	340	475	ns
T_{FS} RX+ to RX– Falling Edge Skew	See Figures 1, 2		5	20	ns
T_{FR} RX+ to RX– Rising Edge Skew	See Figures 1, 2		5	20	ns
T_{SQL} RX Squelch Delay	See Figures 1, 3		230	2000	ns
T_{REL} RX Release Delay	See Figures 1, 3	500	1150	1500	ns

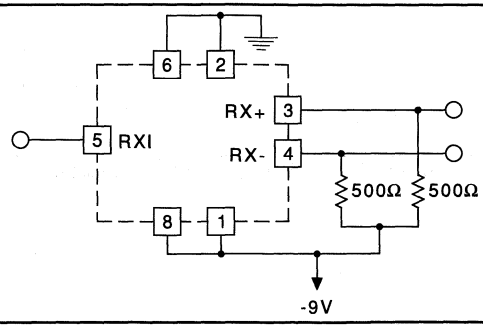


Figure 1. Switching Test Circuit

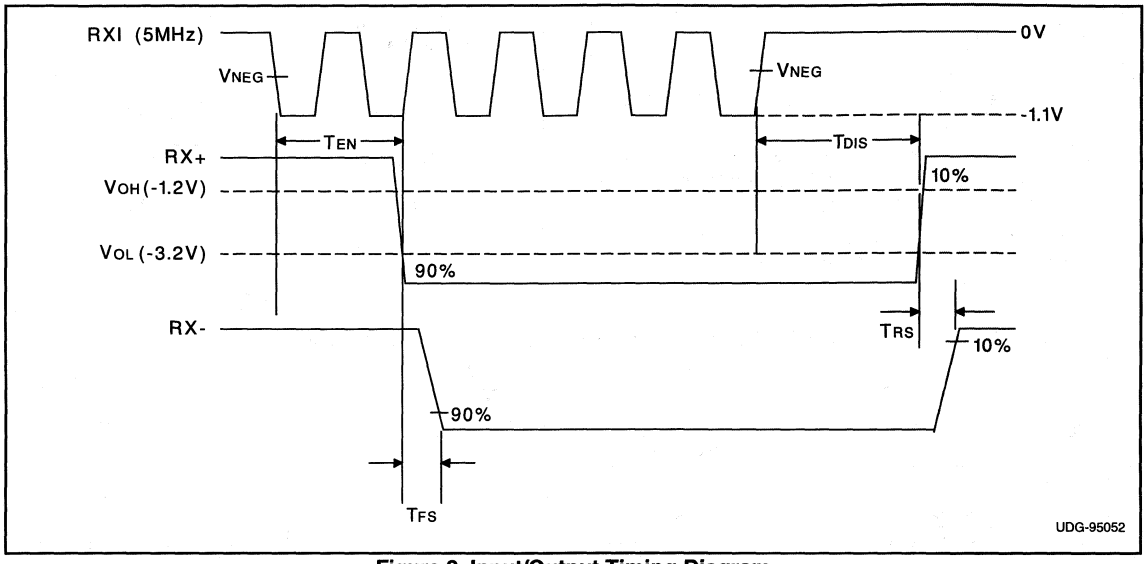


Figure 2. Input/Output Timing Diagram

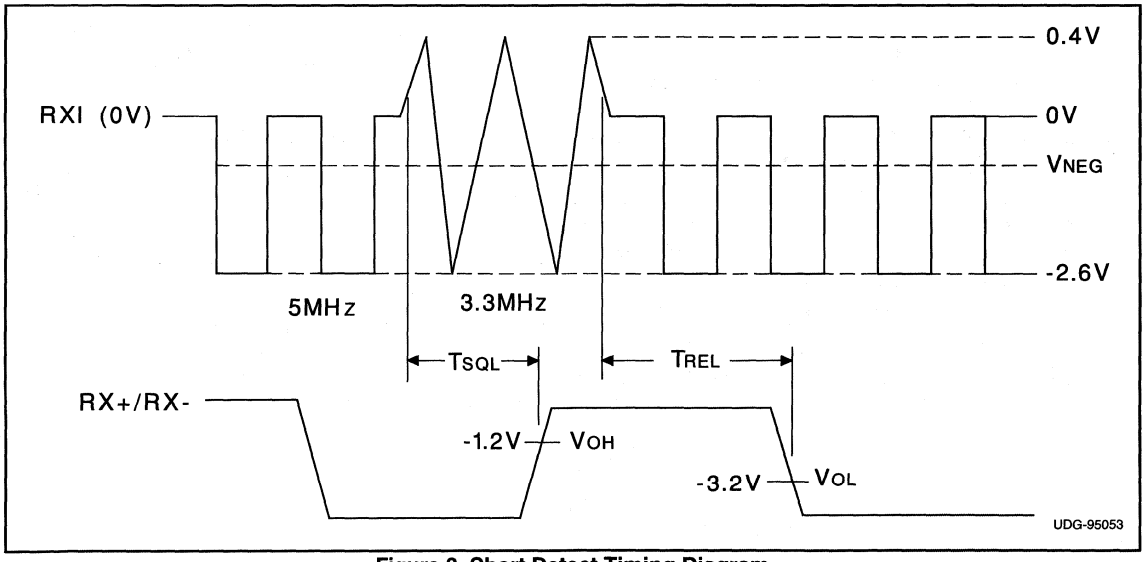


Figure 3. Short Detect Timing Diagram

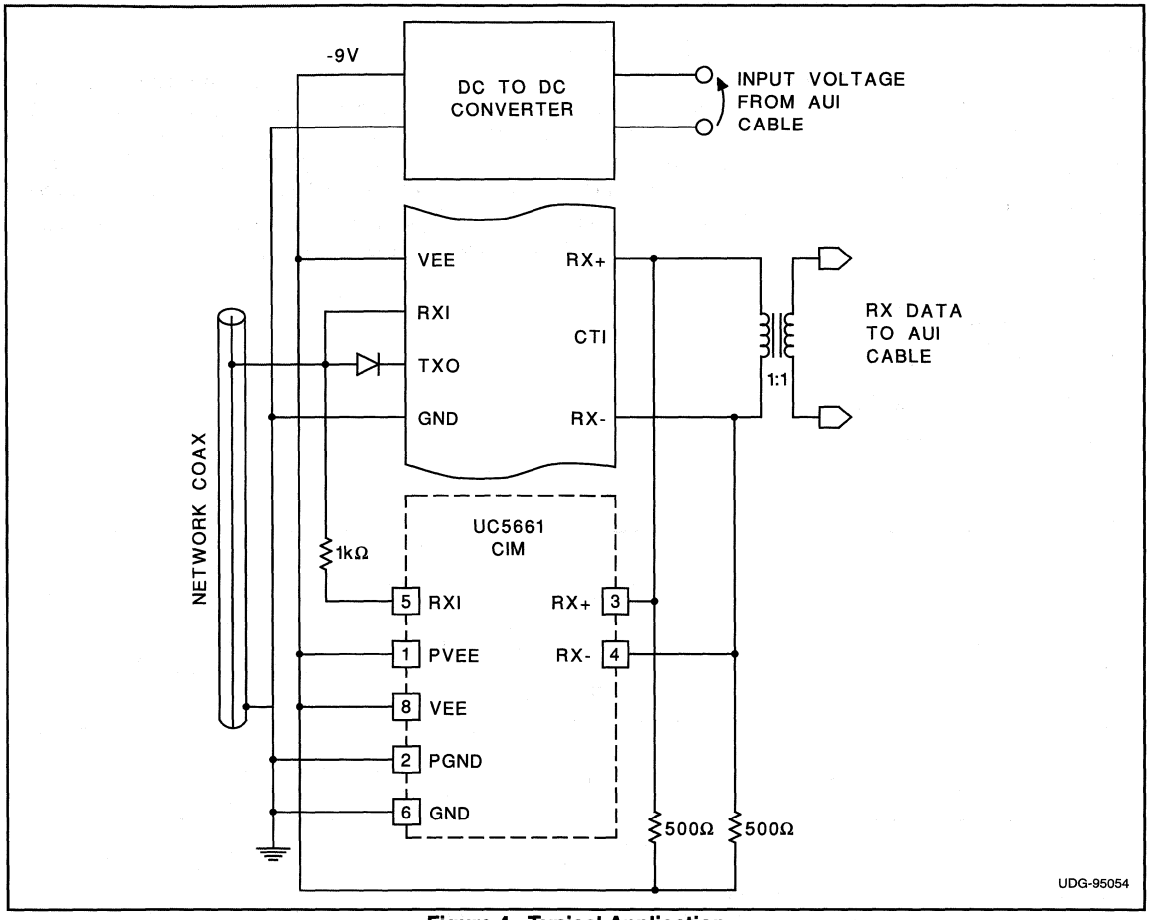


Figure 4. Typical Application

Figure 4 shows the UC5661 (SDI) being used with a Coaxial Transceiver Interface (CTI) device. The primary function of the SDI is to detect LAN cable shorts (or other impedance matching problems) and appropriately squelch the RX outputs of the CTI device to prevent the transmission of corrupted network data. The secondary function of the SDI is to provide improved RX squelching at the completion of a normal data transmission.

To perform the two functions, SDI uses two threshold voltages, Data Reflection Threshold (DRT), and the Valid Data Threshold (VDT). During transmission SDI looks for signal activity above ground and below ground. In the event that the magnitude of the input voltage exceeds DRT the outputs will be locked within 2µs and will remain locked for 0.5 to 1.5µs after the last edge below DRT (see Figure 3). During signal activity below ground when the signal goes below VDT the outputs will unlock within 400ns. While unlocked, if the input exceeds VDT the outputs will lock within 250 to 475ns relative to the last positive going edge (Figure 2).

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Multimode (LVD/SE) SCSI 9 Line Terminator

FEATURES

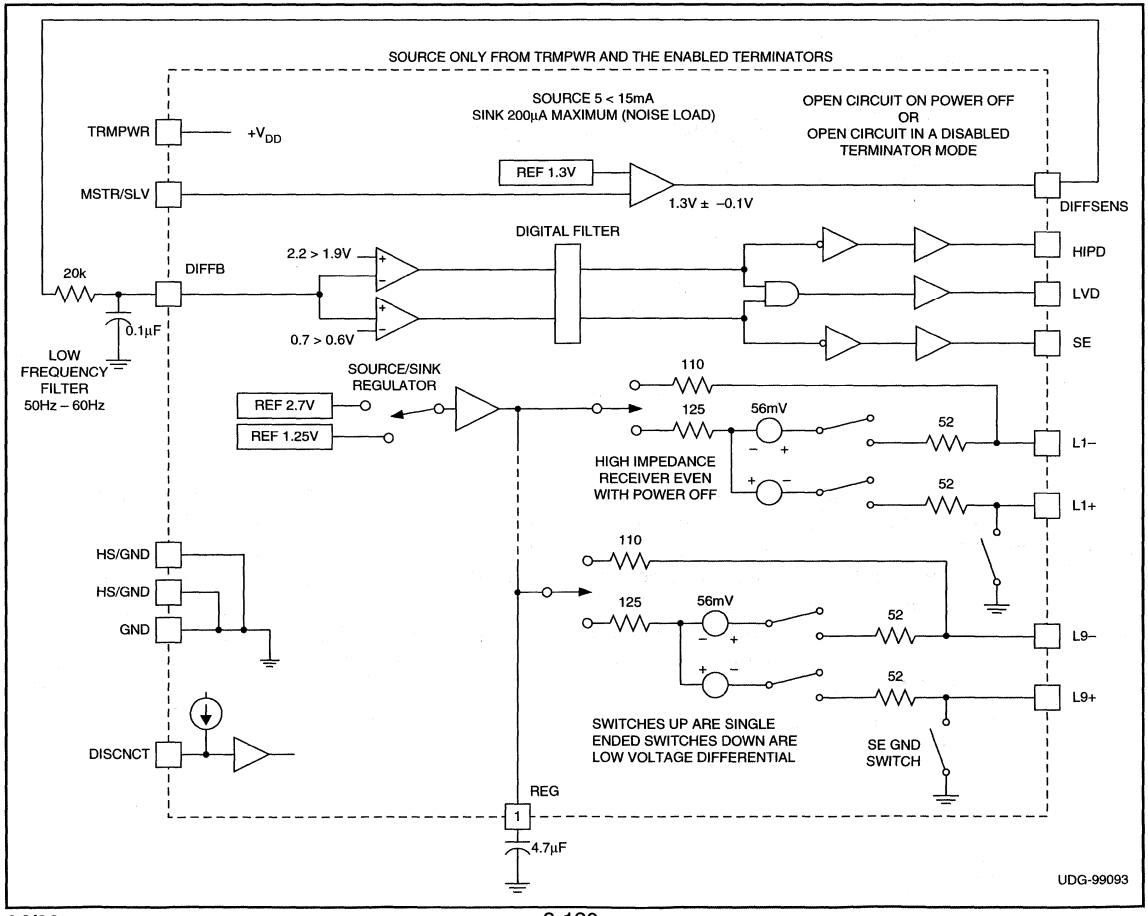
- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter Delay
- Master/Slave Inputs
- Supports Active Negation
- Standby (Disable Mode) 5µA
- 3pF Channel Capacitance

DESCRIPTION

The UCC5672 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets.

The UCC5672 is SPI-3, SPI-2, SPI and Fast-20 compliant. This device comes in a TSSOP package to minimize the footprint.

BLOCK DIAGRAM



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ADVANCE INFORMATION

Low Voltage Differential (LVD) SCSI 9 Line Terminator

FEATURES

- Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter Delay
- Supports Active Negation
- Standby (Disable Mode) 5µA
- 3pF Channel Capacitance

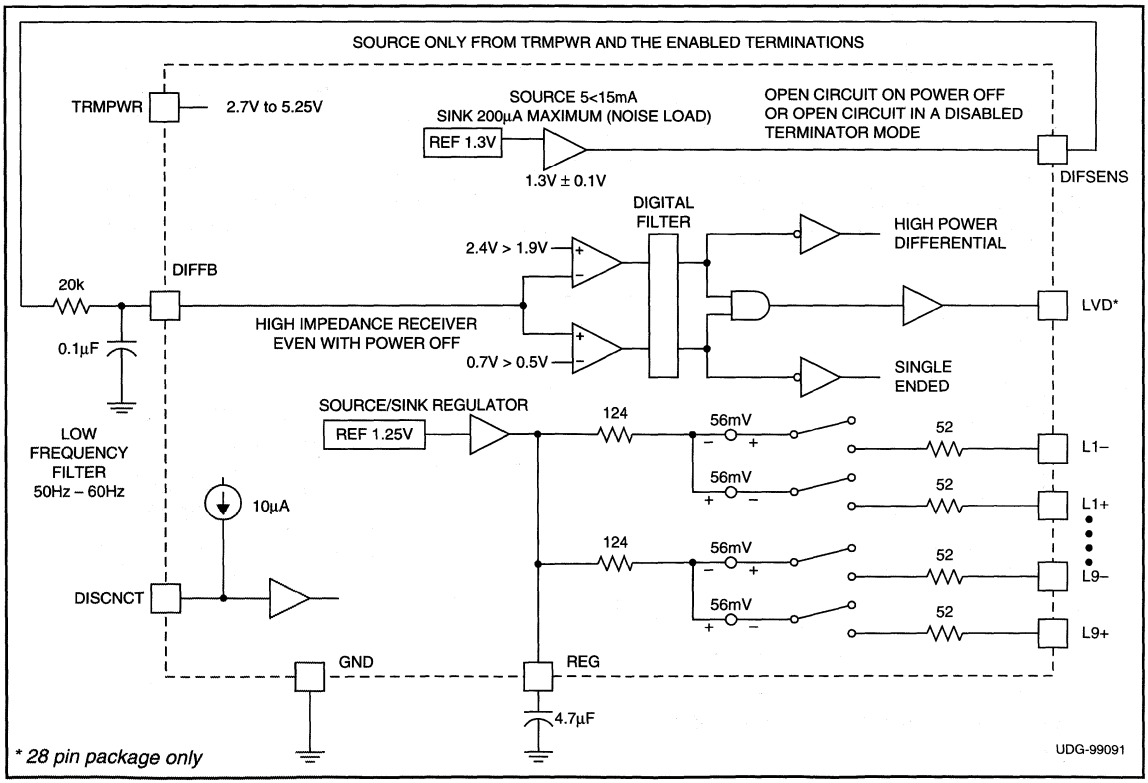
DESCRIPTION

The UCC5680 Low Voltage Differential Terminator is a low voltage differential terminator for the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The UCC5680 is backwards compliant with SPI-2 (Ultra2) and compliant with SPI-3 (Ultra3), (Ultra160/m).

This device comes in a TSSOP package to minimize the footprint and with a unique pin out that eliminate feed through requirements.

3

BLOCK DIAGRAM



UNITRODE

Design Note

UCC5630 SCSI Multimode (LVD/SE) Evaluation Board and List of Materials

By Paul Aloisi

The UCC5630 is a high performance 9 line Multimode terminator designed to provide the lowest capacitance and the lowest possible temperature drift. It is designed for 3.3V or 5V systems and will operate over the range of 2.7V to 5.25V.

The demo board should be used at the end of the bus, between the last device and the cable or as a plug terminator at the end of the cable. Active terminators should be used at both ends of the cable. Generally, they will be used between the controller and the cable and the last device and the cable. If they are used as a plug terminator, the second connector becomes a stub effecting the capacitance load on the bus. The termination can be disabled on the demo card allowing the demo board to be part of the bus path.

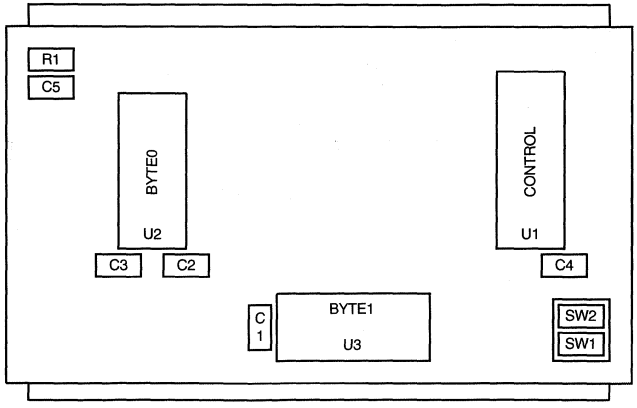
The demo board can be used to test the Unitrode terminator versus drive or controller termination. The demo board demonstrates how Unitrode termination can clean up problems on the bus.

The demo board layout below shows the UCC5630 9 line multimode SCSI termination with a separate disconnect for the high byte (Switch 2) and the control lines and the low byte (Switch 1). Termination should be disabled on all devices but the device at the ends of the cable.

The multimode terminators automatically detect the bus mode by placing 1.3V on the diff sense line, then monitoring the diff sense line through an R-C filter, (R1) 20k and (C5) 0.1µF, to filter out noise down to 50Hz on the bus. If the diff sense line is below 0.5V, the terminators are in single ended mode (SE). If the diff sense line is between 0.7V and 1.9V, the terminators are in Low voltage differential (LVD) mode. If the diff sense line is above 2.1V, the terminator is in high impedance mode. The demo board can not be used on a high voltage differential (HVD) system. The terminator mode can be monitored on pin 33 for single ended mode, pin 34 for low voltage differential mode, and pin 35 for when high impedance high voltage differential devices are detected. The outputs are not valid when the terminators are in disconnect mode.

The connector pinning is defined in **SCSI-3 SPI-2** P cable LVD.

The layout of the demo board is an attempt to match the length and loading of the lines. Every line has a feedthrough connection to the terminator, but the surface mount connector requires a feedthrough on one side of every line. This is not as critical on this 2 sided board since there is no inner layer capacitance on the feedthroughs. On a

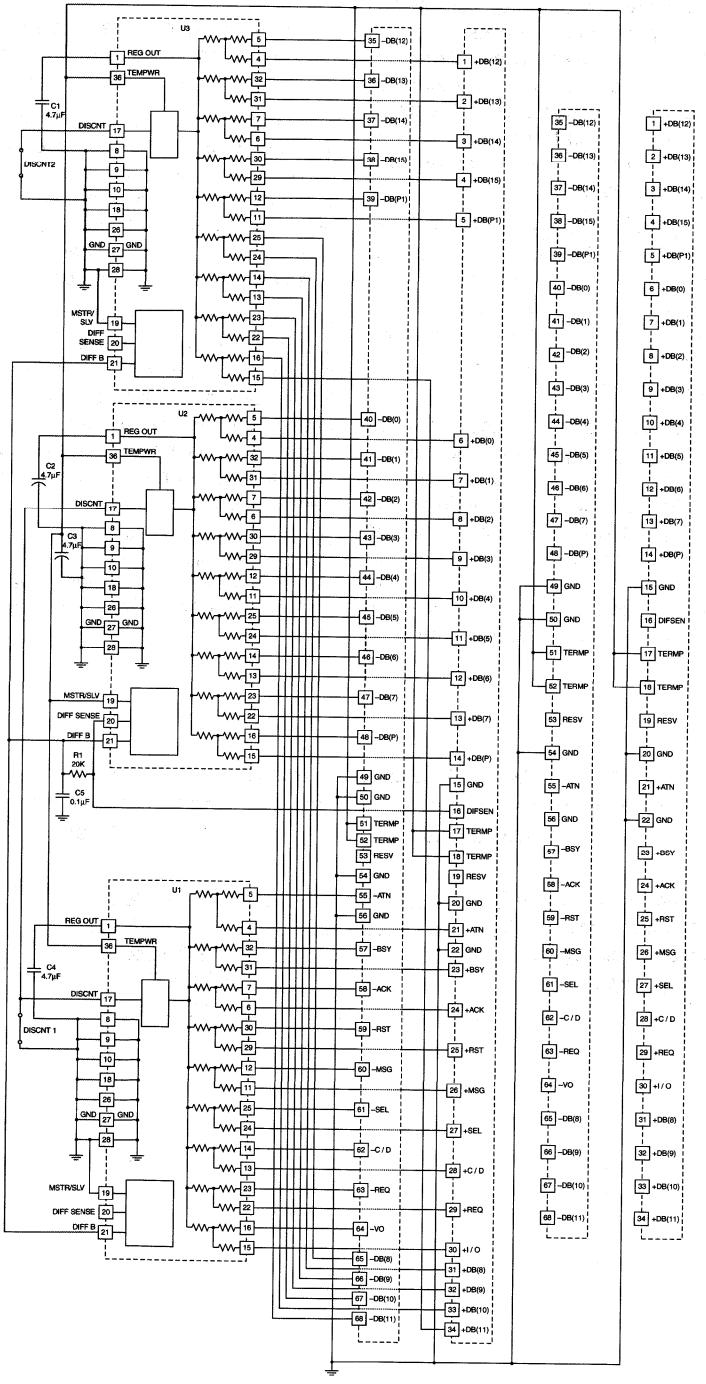


SWITCH 2	SWITCH 1
HIGH BYTE AND PARITY	LOW BYTE AND CONTROL
OFF DISCONNECT	OFF DISCONNECT
TERMINATION ENABLED	TERMINATION ENABLED

UDG-98167

Figure 1. Demonstration board layout

11/98



UDG-98166

Figure 1. UCC5630 Evaluation Board Schematic

multilayer board, one extra feedthrough is more capacitance imbalance than allowed unless the clearance holes on the inner layers are enlargered. Note the heat sink area for the UCC5630 terminators to dissipate heat. If a multilayer layout is used, one feedthrough from each heat sink pin should be connected to the ground plane instead of the heat sink area on the outside layer.

The key indicators of signal integrity are the rising and falling edges of the signals. The REQ and ACK signals are the highest speed signals until Fast-80DT. Reflections on lower speed signals up to Fast-40 normally occur within the bit time. LVD Fast-40 and beyond reflections can be 4 or more bit times from the switch point.

For single ended signals, the rising edge should be over 2.0V on the first step to guarantee data integrity and high speed operation or the bus should be shortened to allow the reflected wave within the set up time. If the falling edge of a signal overshoots and returns to a higher level this is normally a sign that the frequency response of the terminator is not fast enough. This is typical of a problem seen on current mode terminators or terminators with the disconnect switch in the wrong position. Some terminators look good when the signal is observed at the end of the cable, but in the center of the bus the signals can have serious problems.

LVD signals must transition at least 60mV beyond the zero crossing, some receivers will require at least ¼ the signal in the opposite polarity to switch at high speeds. If the signals do not reach the correct amplitude check the system impedance, it should be above 85Ω differential when all the devices are installed on the bus.

Reflections can be isolated by the reflection time. Signal round trip time is normally 10 nanoseconds per meter on cables with standard PVC insulation. Reflections from older devices or bad cables can cause major problems, older designs paid little attention to capacitance and balancing stub lengths. The long stubs and high capacitance will cause reflection problems.

For more information refer to the Unitrode LVD Design Guide or the Single Ended Active Termination Design Guide. Additional support help is available from Unitrode local applications or 408-246-3100 extension 41 or 603-429-8687.

Table 1. UCC5630 Evaluation Board List of Materials

Reference Designator	Description	Manufacturer	Part Number
C1, C2, C3, C4	Tantalum Capacitor 4.7μF	Panasonic	ECS-TICY4755
C5	Ceramic Capacitor 0.1μF	Panasonic	ECJ-3YFIA106Z
R1	20.0K small Resistor	Panasonic	ERJ-8ENF2002
SW1	2 position dip switch	C+K Comp.	SD02HOSK
U1, U2, U3	IC	Unitrode	UCC5630MWP

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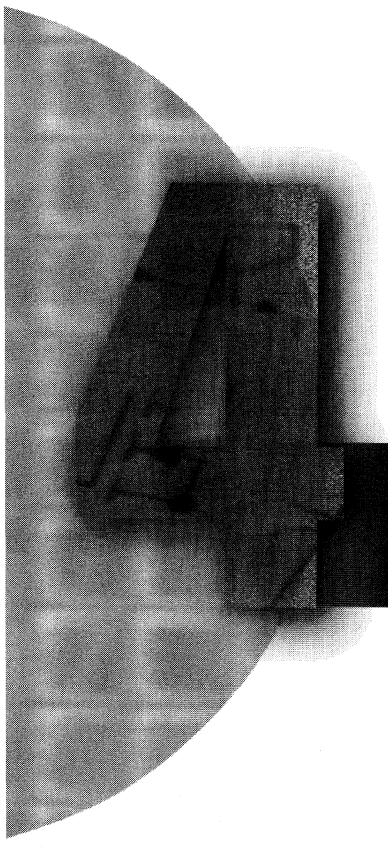


Bus Bias Generators

Bus Bias Generators

Special Functions	UNITRODE PART NUMBER				
	UC382	UC385	UC560	UCC561+	UC563+
Bus Standard	GTL / BTL	GTL / BTL	SCSI-1,2,3	SPI-2,3	VME / VME64
Sink / Source Current	Pgm / 3A	Pgm / 5A	300mA / –750mA	200mA / –200mA	475mA / –575mA
Page Number	PS/5-5	PS/5-35	IF/4-3	IF/4-7	IF/4-10

+ New Product


UNITRODE

27-Line SCSI Source/Sink Regulator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 SPI and Ultra SCSI (Fast-20)
- 2.85V Regulated Output Voltage With 1.4% Tolerance
- Provides Current for up to 27 Lines of Active Termination for SCSI Buses
- –750mA Sourcing Current for Termination
- +300mA Sinking Current for Active Negation Drivers
- 0.9V Dropout Voltage Regulator at 750mA and 2.75V Output
- 100µA Supply Current in Disconnect Mode
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

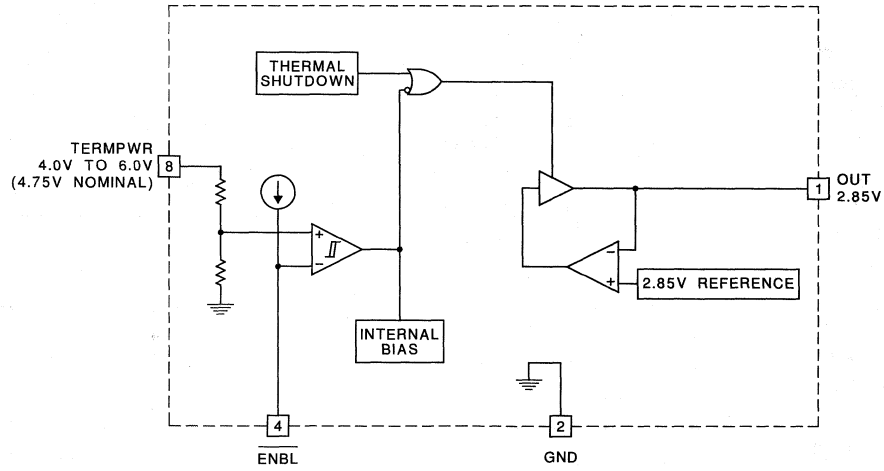
The UC560 provides current for up to 27 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard requires active termination at both ends of the cable. The UC560 is based on the UC5603 and UC5613 SCSI Active Terminators. It uses the voltage regulator and internal logic circuits of those parts, but has no termination circuits. The UC560 provides greater source current drive capability compared to the UC5603 and UC5613.

The UC560 sink current maintains regulation with all active-negation drivers negated. It provides a disconnect feature which disables the regulator to greatly reduce standby power. Internal circuit trimming is utilized for a 1.4% tolerance output voltage. Other features include thermal shutdown and current limit for short circuit conditions.

The UC560 is available in low thermal resistance versions of the industry standard 8-pin power SOIC, 5-pin TO-220 and 5-pin TO-263.

4

BLOCK DIAGRAM



Pin Numbers refer to 8-pin DP package.

UDG-95136-1

ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage 7V
ENBL Voltage . . . . . –0.3V to TERMPWR + 0.3V
Regulator Output Current 1.4A
Power Dissipation 2.5W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

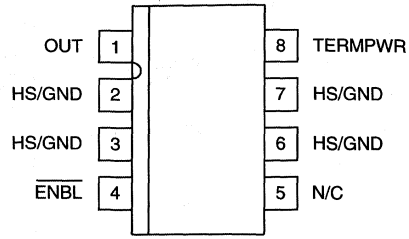
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . . 4.0V to 6.0V
ENBL Voltage . . . . . 0V to TERMPWR

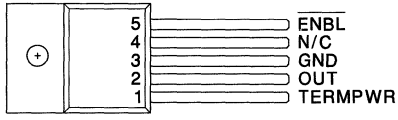
CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



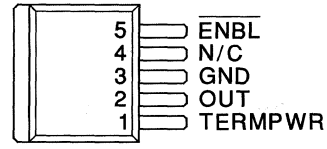
Note: *Pins 2,3,6, and 7 are heat sinking pins. Pin 2 is the connect point for electrical ground.*

5-Pin TO-220 (Top View)
T Package



Note: *TAB is ground.*

5-Pin TO-263 (Top View)
TD Package



Note: *TAB is ground.*

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C, TERMPWR = 4.75V, $\overline{ENBL}$ = 0V, C_{OUT} = 4.7µF, $C_{TERMPWR}$ = 4.7µF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TERMPWR Supply Current	No Load		16	22	mA
	I_{OUT} = –700mA		710	750	mA
Power Down Mode	$\overline{ENBL}$ = 2.0V		100	140	µA
Regulator Section					
Regulator Output Voltage	25°C, No Load	2.81	2.85	2.89	V
Load Regulation	I_{OUT} = 300mA to –750mA (Note 2)		25	30	mV
Line Regulation	TERMPWR = 4.0V to 6.0V, No Load (Note 2)		10	20	mV
Dropout Voltage	I_{OUT} = –750mA, V_{OUT} = 2.75V		0.9	1.2	V
Short Circuit Current	V_{OUT} = 0.0V	–0.85	–1.3		A
Sinking Current	V_{OUT} = 3.5V		500	600	mA
	$\overline{ENBL}$ = 2.0V, V_{OUT} = 3.0V		1	2	mA
Thermal Shutdown	(Note 1)		170		°C
Thermal Shutdown Hysteresis	(Note 1)		10		°C
Shutdown Section					
$\overline{ENBL}$ Threshold		1.1	1.4	1.7	V
Threshold Hysteresis			100		mV
$\overline{ENBL}$ Output Current			–10	–15	µA

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Tested at a constant junction temperature by low duty cycle pulse testing.

PIN DESCRIPTIONS

ENBL: Enable Bar pin. The $\overline{\text{ENBL}}$ function is active low, and the pin will source 10µA typically when at ground and TERMPWR is between 4V and 6V. The part will go into disable mode if $\overline{\text{ENBL}}$ is above 1.4V typical, and will turn back on when $\overline{\text{ENBL}}$ drops below 1.3V typical. The part also greatly reduces TERMPWR current when disabled (100µA typical).

GND: Ground pin.

OUT: 2.85V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. When the part is in disabled mode ($\overline{\text{ENBL}} \geq$ 1.4V typical), the output goes to 0V with no external supply source on OUT. The part will sink current, though, if there is an external supply voltage applied to OUT when in disabled mode. For best perfomance, a 4.7µF low ESR capacitor is recommended.

TERMPWR: Supply voltage pin. The pin should be decoupled with at least a 2.2µF low ESR output capacitor. For best perfomance, a 4.7µF low ESR capacitor is recommended. Lead lengths should be kept at a minimum.

APPLICATIONS INFORMATION

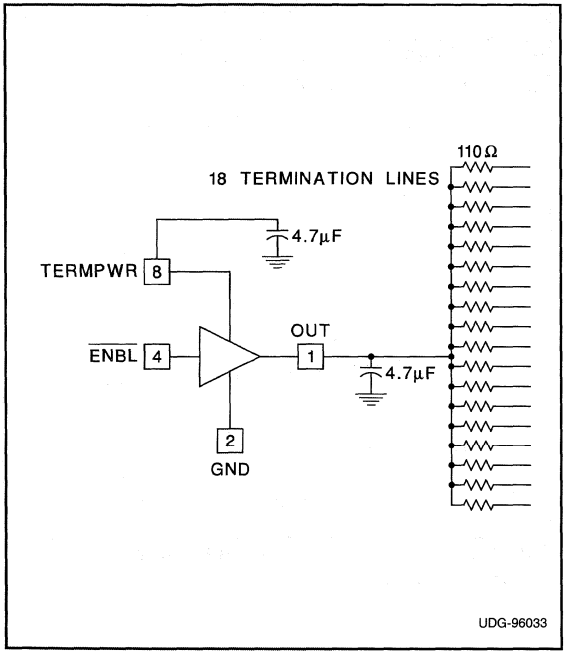


Figure 1. Typical SCSI Bus Configuration Utilizing UC560 Device

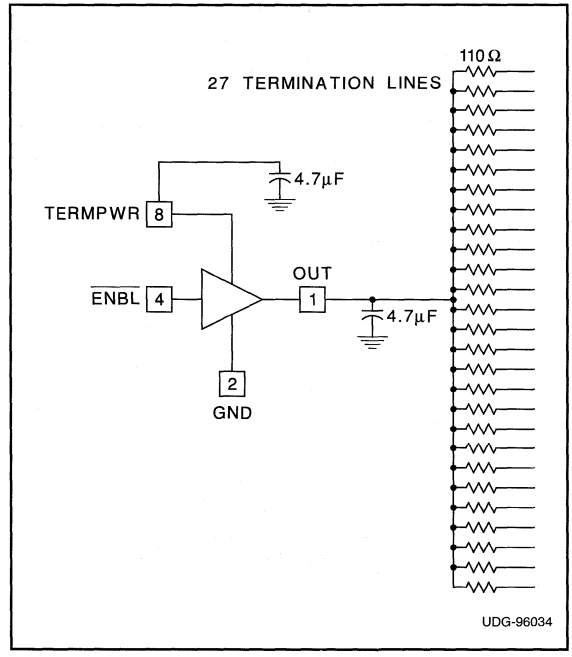


Figure 2. Typical Wide SCSI Bus Configuration Utilizing UC560 Device

TYPICAL CHARACTERISTICS

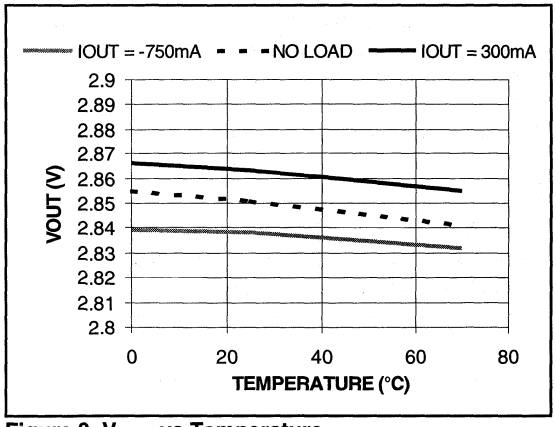


Figure 3. V_{OUT} vs Temperature

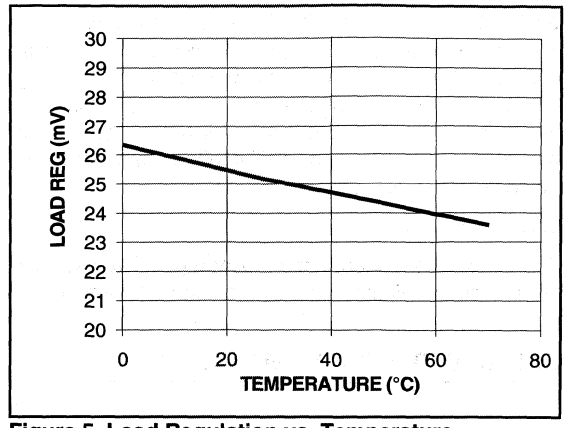


Figure 5. Load Regulation vs. Temperature (I_{OUT} = 300mA to –750mA)

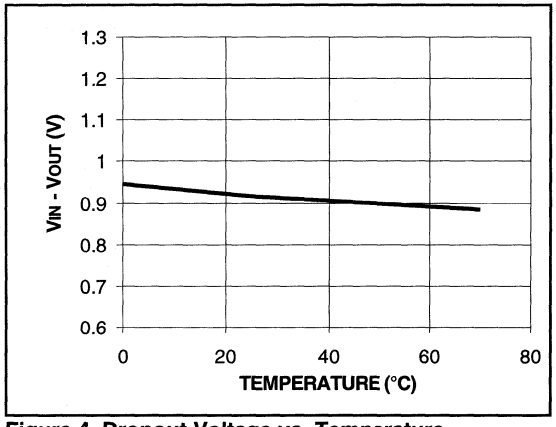


Figure 4. Dropout Voltage vs. Temperature (I_{OUT} = –750mA, V_{OUT} = 2.75V)

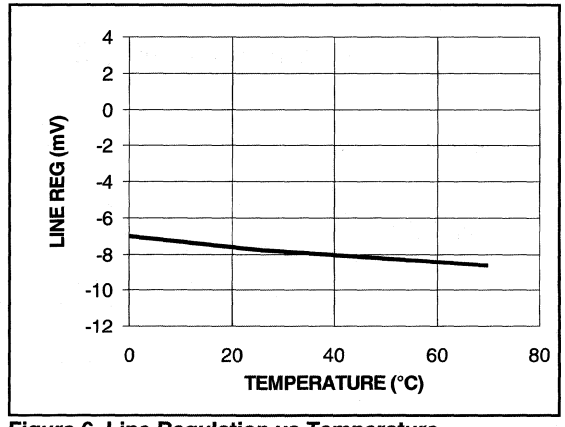


Figure 6. Line Regulation vs Temperature (TERMPWR = 4.0V to 6.0V)

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Low Voltage Differential SCSI (LVD) 27 Line Regulator Set

FEATURES

- SCSI SPI-2 LVD SCSI 27 Line Low Voltage Differential Regulator
- 2.7V to 5.25V Operation
- Integrated Regulator Set for LVD SCSI
- Differential Failsafe Bias

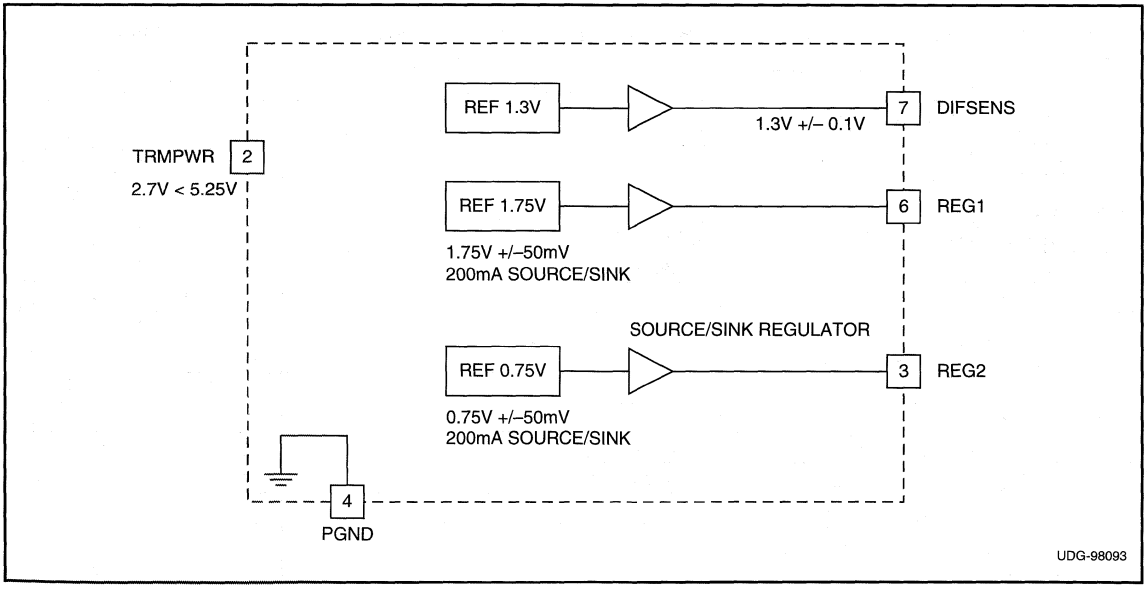
DESCRIPTION

The UCC561 LVD Regulator set is designed to provide the correct references voltages and bias currents for LVD termination resistor networks (475Ω, 121Ω, and 475Ω). The device also provides a 1.3V output for Diff Sense signaling. With the proper resistor network, the UCC561 solution will meet the common mode bias impedance, differential bias, and termination impedance requirements of SPI-2 (Ultra2) and SPI-3 (Ultra3).

This device incorporates into a single monolith, two sink/source reference voltage regulators, a 1.3V buffered output and protection features. The protection features include thermal shut down and active current limiting circuitry. The UCC561 is offered in 16-pin SOIC(DP) package.

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TERMPWR . . . . . +6V
Package Dissipation 1.2W
Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

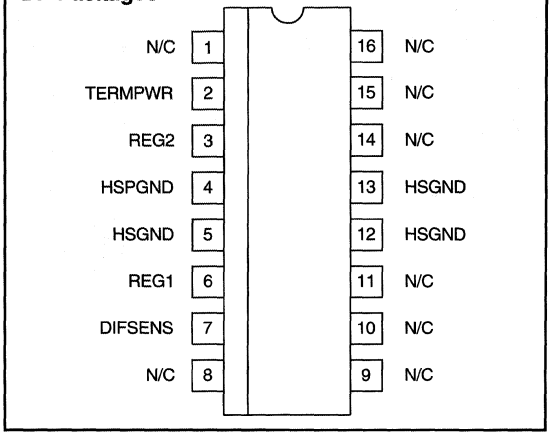
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . . 2.7V to 5.25V

CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications apply for TA = 0°C to 70°C, TERMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TERMPWR Supply Current Section					
TERMPWR Supply Current	No Load			40.0	mA
TERMPWR Voltage		2.7		5.25	V
Regulator Section					
1.75 Volt Regulator	REG1 (± 125mA)	1.7	1.75	1.8	V
1.3 Volt Regulator	DIFSENS , No Load	1.2	1.3	1.4	V
0.75 Volt Regulator	REG2 (± 125mA)	0.7	0.75	0.8	V
1.75 Volt Regulator Source Current	V_O = 1.25			–200	mA
1.75 Volt Regulator Sink Current	V_O = 2.25	200			mA
1.75 Volt Sink Current Limit				700	mA
1.75 Volt Source Current Limit		–700			mA
1.3 Volt Regulator Source Current	DIFSENS, GND	–5		–15	mA
1.3 Volt Regulator Sink Current	DIFSENS, 2.4V	50		200	µA
0.75 Volt Regulator Source Current	V_O = 0.25			–200	mA
0.75 Volt Regulator Sink Current	V_O = 1.25	200			mA
0.75 Source Current Limit				700	mA
0.75 Sink Current Limit		–700			mA

Note 1: Guaranted by design. Not 100% tested in production.

APPLICATION INFORMATION

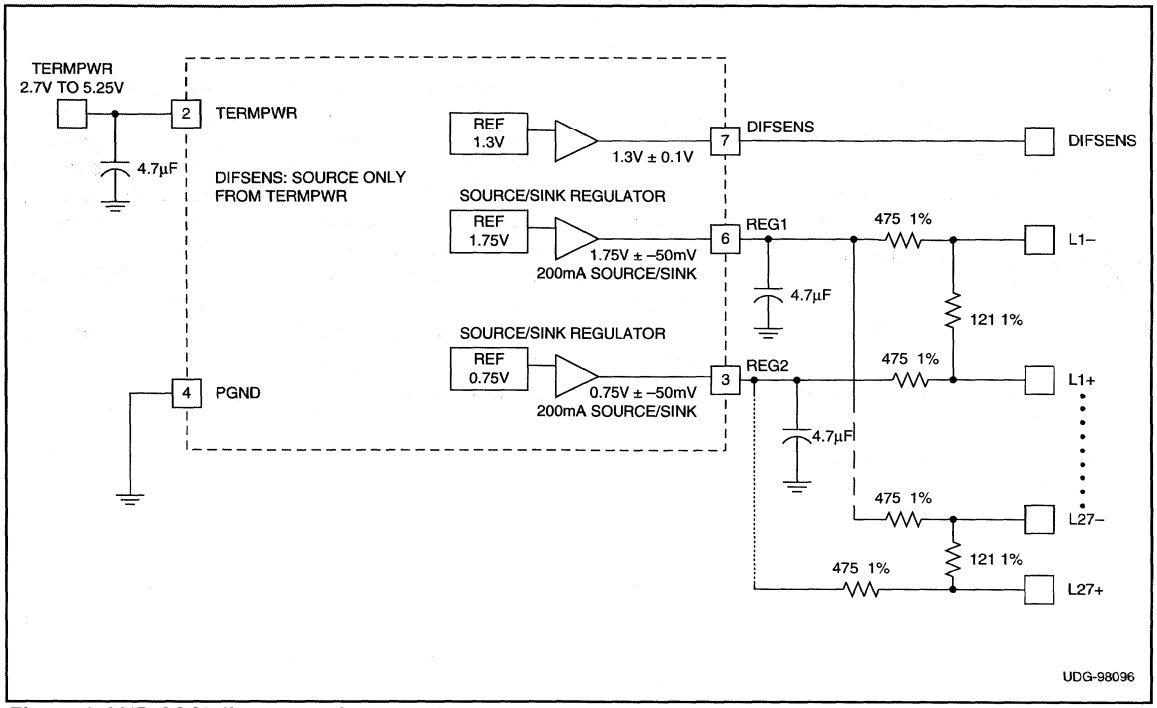


Figure 1. LVD SCSI discrete resistor stack.

Table I. Resistor stack vs. standard.

Outputs	Specification
107.3Ω Diff	100Ω to 110Ω
112.9mV Diff Bias	100mV to 125mV
237Ω Common Mode	100Ω to 300Ω
1.25V Common Mode	1.2V to 1.30V

Application Note: The resistor stack with the 1.75V and 0.75V reference will give the correct differential impedance, bias voltage, common mode differential impedance and common mode voltage as show in Table 1.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

32 Line VME Bus Bias Generator

FEATURES

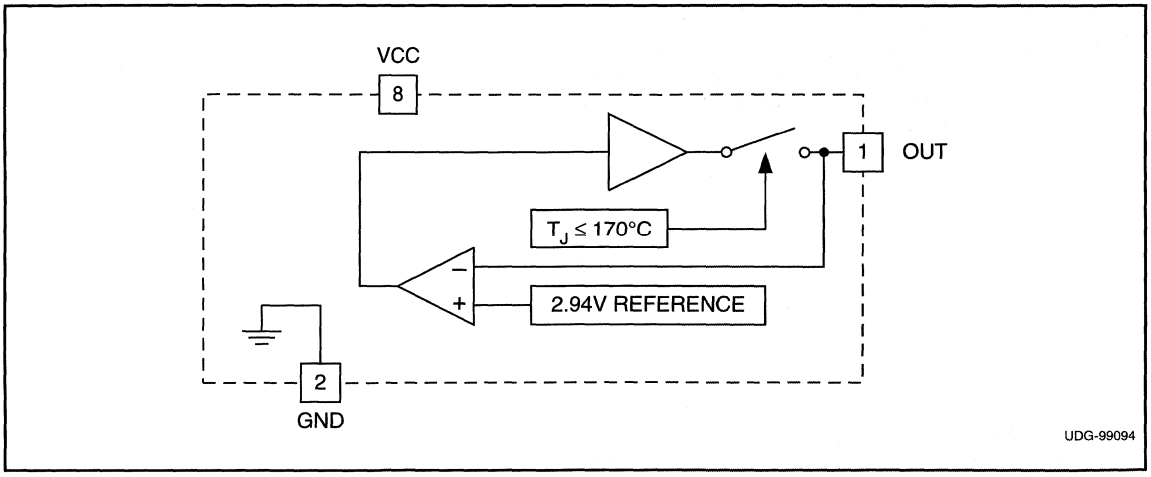
- Complies with VME64 Standard
- 2.94V Regulated Output Voltage With 1% Tolerance at 25°C
- Provides Bias for up to 32 Lines of Active Termination for VME busses
- –575mA Sourcing Current for Termination
- +475mA Sinking Current for Active Negation Drivers
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The VME bus bias generator provides current for up to 32 lines of active termination for a VME64 parallel bus. The VME standards require termination at both ends of the bus. The voltage regulator and internal logic circuits of these parts provide all the functionality and performance necessary to bias termination resistors for the VME Bus. The VME bus bias generator sink current maintains regulation with all active negation drivers negated. Internal circuit trimming is used to trim the output voltage to a 1% tolerance. Other features include thermal shutdown and current limit for short circuit conditions. This device is available in low thermal resistance versions of the industry standard 8-pin power SOIC, 3 pin TO-220 and 3 pin TO-263.

Termination is a VME requirement but passive is also an option.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

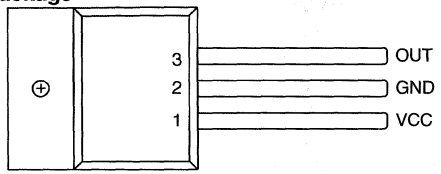
VCC ..... +7V
Regulator Output Current 600mA
Storage Temperature ..... -65°C to +150°C
Junction Temperature ..... -55°C to +150°C
Lead Temperature (Soldering, 10 secretary.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

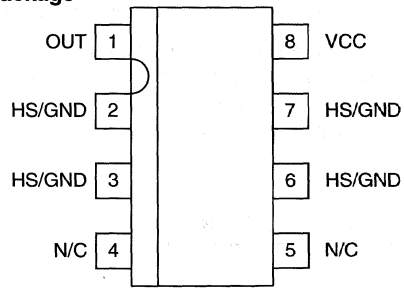
VCC Voltage ..... 4.875V to 5.25V

TO220-3 (Top View)
T Package

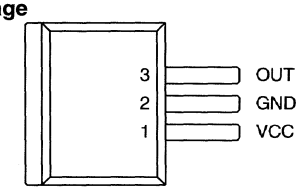


CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



TO263-3 (Top View)
TD Package



4

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, V_{CC} = 5.00V; C_{OUT} = 4.7µF; T_A = T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current	No load		25		mA
	I_{OUT} = –600mA		602	650	mA
Regulator Section					
Output Voltage	25°C, No load	2.793	2.94	3.087	V
Load Regulation	–575mA ≤ I_{OUT} ≤ 475mA (Note 1)		25	30	mV
Line Regulation	4.875V ≤ V_{CC} ≤ 5.25V, No load		10	20	mV
Short Circuit Current	V_{OUT} = 0V			–600	mA
	V_{OUT} = 3.5V	500			
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C

Note 1: Tested at a constant junction temperature by low duty cycle pulse testing.

Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

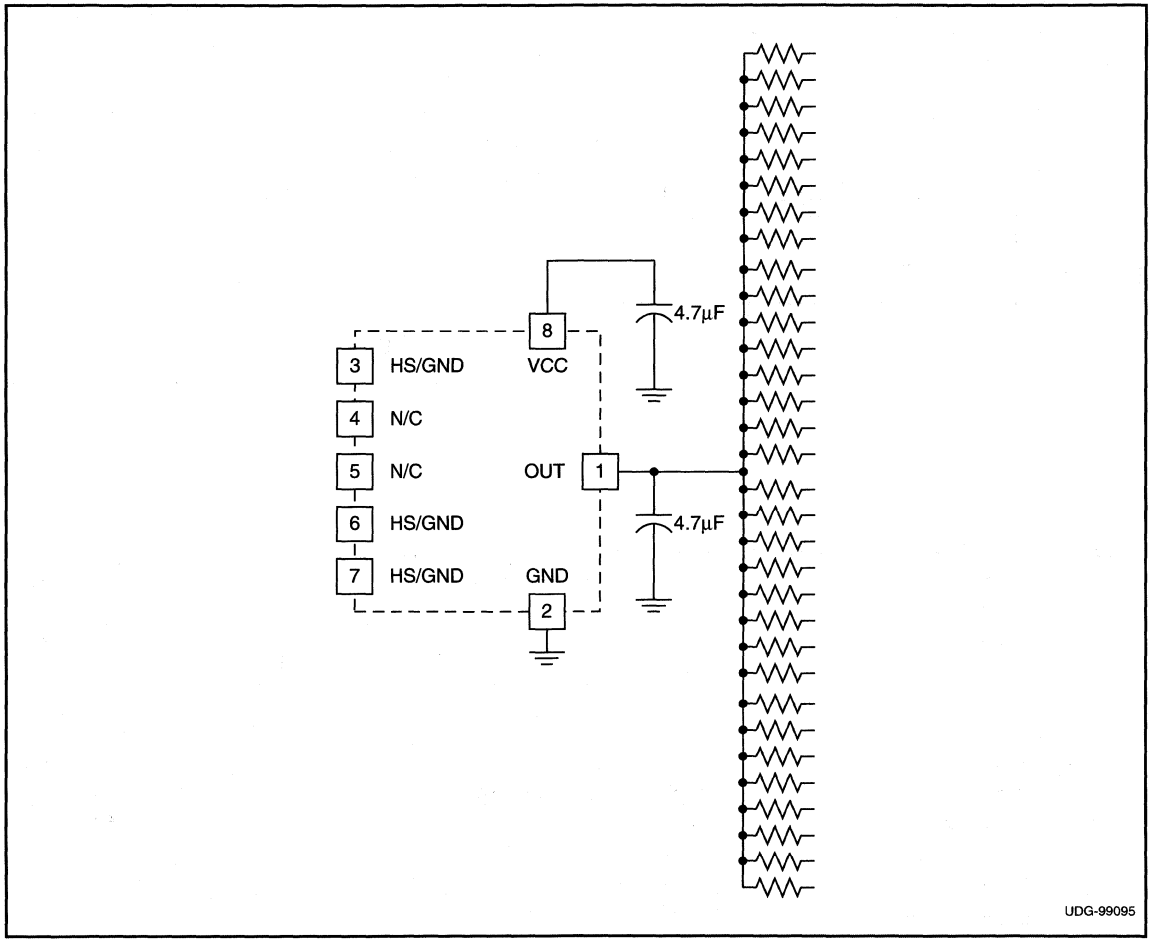
GND: Ground pin.

HS/GND: Heat sink GND. Connect to large area PC board traces to increase power dissipation capability.

OUT: 2.94V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. For best performance, a 4.7µF low ESR capacitor is recommended.

VCC: Supply voltage pin. The pin should be de-coupled with at least a 2.2µF low ESR capacitor. For best performance, a 4.7µF low ESR capacitor is recommended. Lead lengths should be kept at a minimum.

TYPICAL APPLICATION



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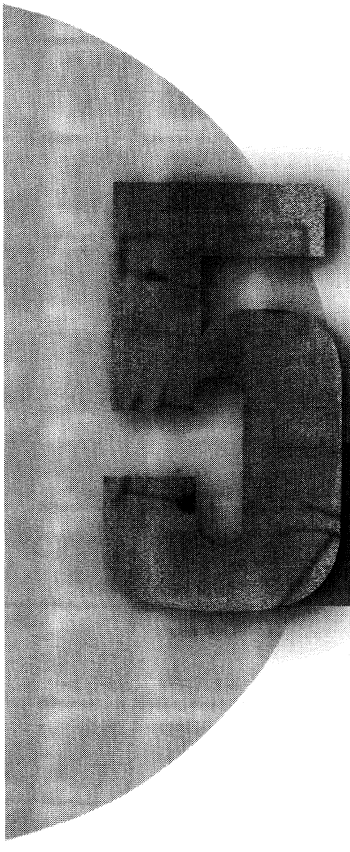


Hot Swap Power Manager™ ICs

Hot Swap Power Managers

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3912	UCC3913	UC3914	UCC3915	UCC39151
Voltage Range	3V to 8V	−10.5V to External Limitation	5V to 35V	7V to 15V	7V to 15V
Current Range	0A to 3A	Externally Limited	Externally Limited	0A to 3A	0A to 3A
Integrated Power FET	Y	N	N	Y	Y
RDSon	150mΩ	N/A	N/A	150mΩ	150mΩ
Programmable Fault Threshold	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	N	Y	Y	N	N
Average Power Limiting	N/A	Y	Y	N/A	N/A
Application / Design Note	DN-58, DN-68, U-151	DN-67		DN-58, DN-68, U-151	DN-58, DN-68, U-151
Available Package	TSSOP, SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-9	IF/5-15	IF/5-23	IF/5-37	IF/5-42

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3916	UCC39161	UCC3917+	UCC3918	UCC3919
Voltage Range	4V to 6V	4V to 6V	10V to External Limitation	3V to 6V	3V to 8V
Current Range	−1.8A to −1.5A	−1A to −0.7A	Externally Limited	0A to 4A	Externally Limited
Integrated Power FET	Y	Y	N	Y	N
RDSon	220mΩ	220mΩ	N/A	60mΩ	N/A
Programmable Fault Threshold	N	N	Y	Y	Y
Programmable Time Delays	Y	Y	Y	Y	Y
Latched Fault Mode	N	N	Y	N	Y
Average Power Limiting	N/A	N/A	Y	N/A	Y
Application / Design Note			DN-98	DN-87	DN-95
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP
Page Number	IF/5-47	IF/5-50	IF/5-53	IF/5-61	IF/5-68

+ New Product

Hot Swap Power Managers (cont.)

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3921	UCC3995+	UCC3996+		
Voltage Range	–10.5V to External Limitation	2.75V to 5.5V	2.75V to 13.6V Two Supplies Sequenced		
Current Range	Externally Limited	Externally Limited	Externally Limited		
Integrated Power FET	N	N	N		
RDSon	N/A	N/A	N/A		
Programmable Fault Threshold	Y	Y	Y		
Programmable Time Delay	Y	Y	Y		
Latched Fault Mode	Y	N	Y		
Average Power Limiting	Y	Y	Y		
Application / Design Note					
Available Package	SOIC or PDIP	TSSOP or SOIC	TSSOP, SOIC or PDIP		
Page Number	IF/5-78	IF/5-98	IF/5-100		

Special Functions	UNITRODE PART NUMBER				
	UCC3831	UCC38531	UCC3981+	UCC39811+	UCC3985+
Part Name	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	CompactPCI Hot Swap Power Manager
Description	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Fully CompactPCI Compliant. Four Channels for Individual Control of Four Supplies 12V, –12V, 5V, and 3.3V
Application / Design Note					
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-3	IF/5-6	IF/5-88	IF/5-91	IF/5-94

+ New Product

Universal Serial Bus Power Controller

FEATURES

- Fully USB Compliant
- Support Four 5V Peripherals and One USB 3.3V Controller
- Separate Power Enables
- 500mA Current Limiting per Channel
- Separate Open Drain Fault Indicator for Each Channel
- 3.3V Output for USB Controller
- Available in 28 Pin Wide Surface Mount and DIP

DESCRIPTION

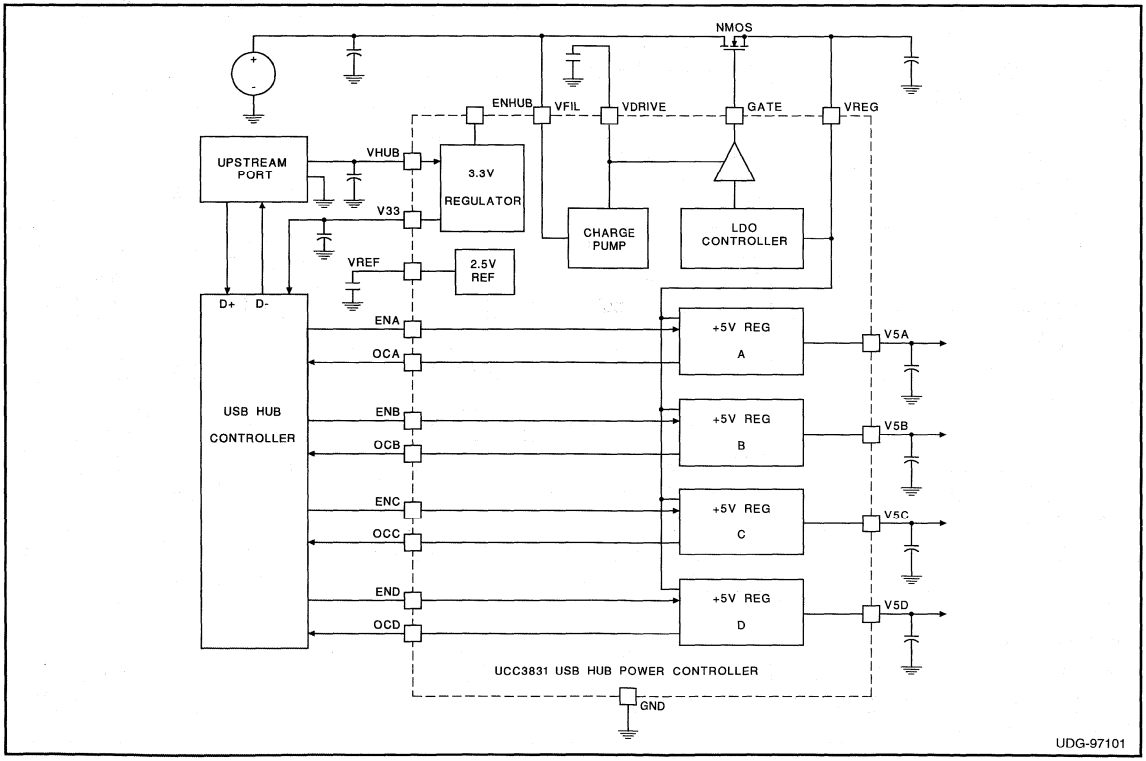
The UCC3831 Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage and four 5V regulated voltages for USB ports. Each of the 5V output ports is individually enabled for optimal port control. Each port also provides an overcurrent fault signal indicating that the port has exceeded a 500mA current limit. The 3.3V linear regulator is used to power the local USB microcontroller. This regulator is protected with a 100mA current limit and has a logic level enable input.

The UCC3831 can be configured to provide USB port power from a loosely regulated voltage such as a Filament voltage internal to a monitor. Pre-regulation is provided by an internal linear regulator controller and one external logic level N-channel MOSFET. The UCC3831 can also be configured without using the pre-regulator stage by connecting the VREG pins to a regulated 5.5V 2A source.

The UCC3831 comes in a 28-pin wide SOIC power package optimized for power dissipation, and is protected by internal over-temperature shutdown mechanism, which disables the outputs should the internal junction temperature exceed 150°C.

5

APPLICATION AND BLOCK DIAGRAM



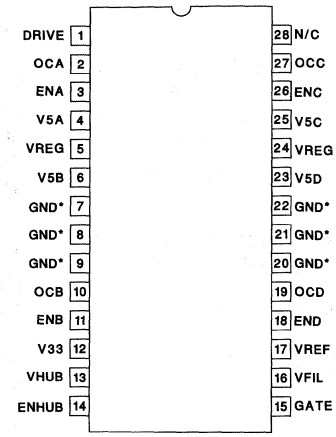
ABSOLUTE MAXIMUM RATINGS

VFIL 9V
VCON Supply Votage 9V
Logic Inputs (ENA-D, ENHUB)
  Maximum Forced Voltage . . . . . –0.3V to 7V
  Maximum Forced Current . . . . . ±1mA
V33
  Maximum Forced Voltage. 5V
  Maximum Current 200mA
V5A-D
  Maximum Voltage. 9V
  Maximum Current 750mA
Storage Temperature. . . . . -65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_J = 0°C to 125°C for the UCC3831. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Currents					
VHUB Supply Current	No External Load on V33		1	3	mA
VFIL Supply Current			1	3	mA
Reference					
VREF Voltage	Over Temperature	2.35	2.5	2.65	V
Line Regulation	VHUB = 4.5V to 9V		3	10	mV
3.3V Regulator					
V33 Voltage	T_J = 25°C, I_{LOAD} = 10mA	3.2	3.3	3.4	V
	0mA to 100mA, 0°C to 125°C, VHUB = 4.5V to 9V	3.165	3.3	3.435	V
Short Circuit Current Limit	VHUB = 6V, Output shorted to Ground	100	120	150	mA
Pre-Regulator					
VREG Voltage	0A to 2A, 0°C to 125°C, VFIL = 6V to 9V	5.25	5.5	5.7	V
5V Regulator					
V5A-D Voltage	T_J = 25°C, I_{LOAD} = 250mA, V_{REG} = 5.5V	4.85	5	5.15	V
	0mA to 500mA, 0°C to 125°C	4.8	5	5.2	V
Short Circuit Current Limit	VREG = 5.5V, Output Shorted to Ground	500	600	750	mA
Charge Pump					
Quiescent Output Voltage	T_J = 25°C, VFIL = 6V, ENA-D = 5V, ENHUB = 5V	11	11.45	12	V
	0°C to 125°C, VFIL = 6V	10.5	11.45	12	V
Output Impedance			9	15	kΩ
Enable Inputs					
ENA-D Inputs - Guaranteed Low				0.7	V
ENA-D Inputs - Guaranteed High		3			V
Enable Inputs (cont.)					
ENHUB Input - Guaranteed Low				0.7	V

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_J = 0°C to 125°C for the UCC3831. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENHUB Input - Guaranteed High		3			V
Overcurrent Signals					
Active Sink Current	Iocx =100µA		140	500	mV

PIN DESCRIPTIONS

ENA-D: Separate enables pins for each of the four 5V supplies.

ENHUB: Enables the 3.3V output V33. Pulling this pin low disables V33.

GATE: Gate drive for an external NMOS used to regulate the 5.5V VREG supply. Minimum available drive is 11V.

GND: All 6 GND pins must be tied to the system ground. In addition to serving as electrical conductors, these 6 pins are heat sinks. Refer to the Packaging Device Temperature Management guide in the Packaging section of the Unitrode Databook.

OCA-D: Open drain overcurrent indicator. OCA-D can be wire OR'ed by the user to create a single overcurrent indicator.

V5A-D: 5V regulated output with enable, 500mA (minimum) current limit, and overcurrent indicator.

V33: 3.3V regulator output. Enable when ENHUB is high. Current limit is 100mA minimum.

VDRIVE: Internal charge pump voltage is brought out for external decoupling. Nominal voltage is between 11V and 13V. No external loading permitting. Decouple with at least 0.001µF capacitor.

VFIL: Bias supply for all four of the 5V regulators. VFIL voltage must be between 6V and 9V.

VHUB: Supply for the 3.3V USB controller power supply and bandgap reference.

VREF: Internal 2.5V reference is brought out for external decoupling only. Decouple with 0.01µF capacitor.

VREG: Regulated to 5.5V by means of an external NMOS. 2 pins supply up to a total of 2.5A to the four 5V bus voltages (V5A, V5B, V5C, V5D).

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UNITRODE

application INFO available

UCC38531

PRELIMINARY

Universal Serial Bus Power Controller

FEATURES

- Fully USB Compliant
- Support Four 5V Peripherals and One USB 3.3V Controller
- Separate Power Enables
- 500mA Current Limiting per Channel
- Separate Open Drain Fault Indicator for Each Channel
- 3.3V Output for USB Controller
- Available in 20 Pin DIP

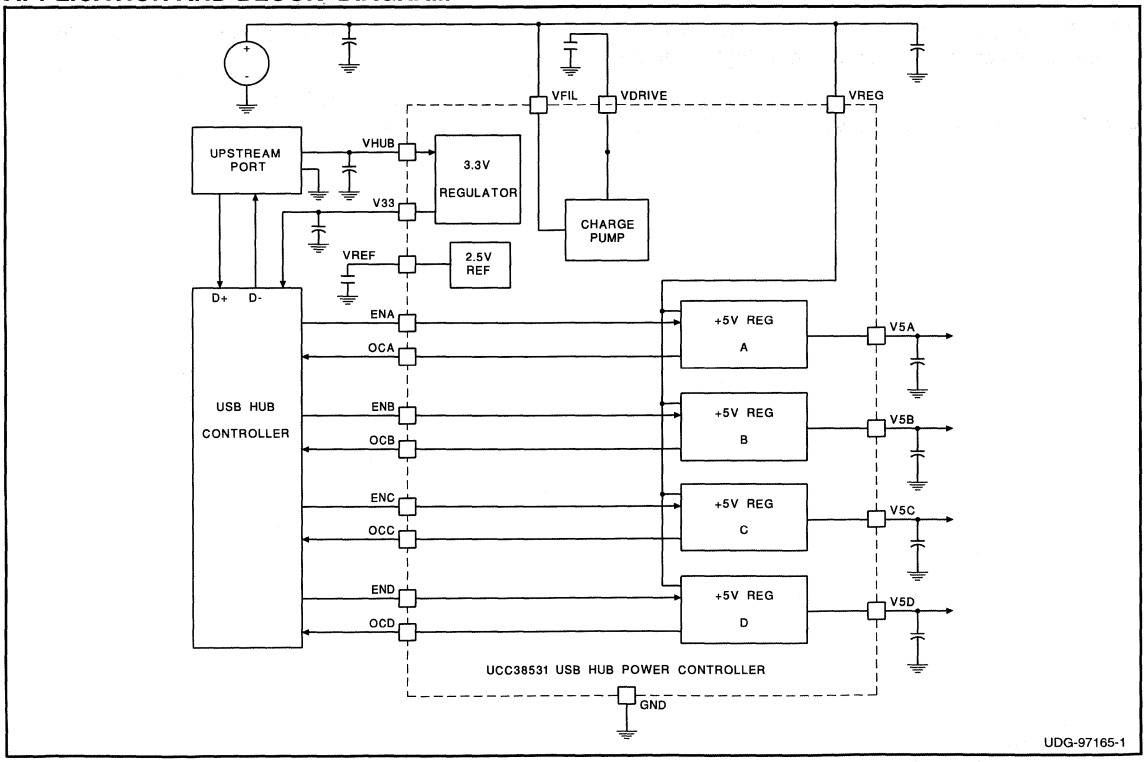
DESCRIPTION

The UCC38531 Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage and four 5V regulated voltages for USB ports. Each of the 5V output ports is individually enabled for optimal port control. Each port also provides an overcurrent fault signal indicating that the port has exceeded a 500mA current limit. The 3.3V linear regulator is used to power the local USB microcontroller. This regulator is protected with a 100mA current limit.

The UCC38531 is configured by connecting the VREG to a regulated 5.5V 2A source.

The 20-pin DIP package is protected by internal over-temperature shutdown mechanism, which disables the outputs should the internal junction temperature exceed 150°C.

APPLICATION AND BLOCK DIAGRAM



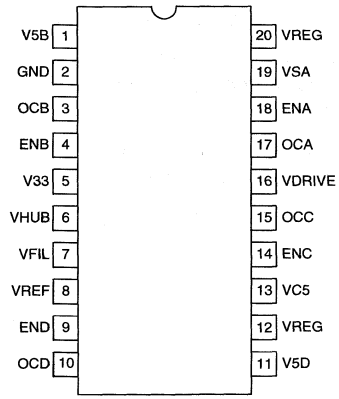
ABSOLUTE MAXIMUM RATINGS

VFIL 9V
VCON Supply Votage 9V
Logic Inputs (ENA-D)
  Maximum Forced Voltage . . . . . –0.3V to 7V
  Maximum Forced Current 1mA
V33
  Maximum Forced Voltage. 5V
  Maximum Current 200mA
V5A-D
  Maximum Voltage. 9V
  Maximum Current 750mA
Storage Temperature . . . . . 65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIP-20 (Top View)
N Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 0°C to 125°C for the UCC38531. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Currents					
VHUB Supply Current	No External Load on V33		1	3	mA
VFIL Supply Current			1	3	mA
Reference					
VREF Voltage	Over Temperature	2.35	2.5	2.65	V
Line Regulation	VHUB = 4.5V to 9V		3	10	mV
3.3V Regulator					
V33 Voltage	T_J = 25°C, I_{LOAD} = 10mA	3.2	3.3	3.4	V
	0mA to 100mA, 0°C to 125°C, VHUB = 4.5V to 9V	3.165	3.3	3.435	V
Short Circuit Current Limit	VHUB = 6V, Output shorted to Ground	100	120	150	mA
5V Regulator					
V5A-D Voltage	T_J = 25°C, I_{LOAD} = 250mA, V_{REG} = 5.5V	4.85	5	5.15	V
	0mA to 500mA, 0°C to 125°C	4.8	5	5.2	V
Short Circuit Current Limit	VREG = 5.5V, Output Shorted to Ground	500	600	750	mA
Charge Pump					
Quiescent Output Voltage	T_J = 25°C, VFIL = 6V, ENA-D = 5V, ENHUB = 5V	11	11.45	12	V
	0°C to 125°C, VFIL = 6V	10.5	11.45	12	V
Output Impedance			9	15	k
Enable Inputs					
ENA-D Inputs - Guaranteed Low				0.7	V
ENA-D Inputs - Guaranteed High		3			V
Overcurrent Signals					
Active Sink Current	I_{OCX} =100µA		140	500	mV

PIN DESCRIPTIONS

ENA-D: Separate enables pins for each of the four 5V supplies.

GND: All voltages are measured with respect to this pin. Bypass capacitors should be connected to GND as close to this pin as possible.

OCA-D: Open drain overcurrent indicator. OCA-D can be wire OR'ed by the user to create a single overcurrent indicator.

V5A-D: 5V regulated output with enable, 500mA (minimum) current limit, and overcurrent indicator.

V33: 3.3V regulator output. Current limit is 100mA minimum.

VDRIVE: Internal charge pump voltage is brought out for external decoupling. Nominal voltage is between 11V and 13V. No external loading permitting. Decouple with at least 0.001µF capacitor.

VFIL: Bias supply for all four of the 5V regulators. VFIL voltage must be between 6V and 9V.

VHUB: Supply for the 3.3V USB controller power supply and bandgap reference.

VREF: Internal 2.5V reference is brought out for external decoupling only. Decouple with 0.01µF capacitor.

VREG: Input supply for all four 5V regulators. 2 pins supply up to a total of 2.5A to the four 5V bus voltages (V5A, V5B, V5C, V5D). Can be tied directly to VFIL.

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Programmable Hot Swap Power Manager

FEATURES

- Integrated 0.15Ω Power MOSFET
- 3V to 8V Operation
- Digital Programmable Current Limit from 0 to 3A
- Electronic Circuit Breaker Function
- 1µA I_{CC} when Disabled
- Programmable on Time
- Programmable Start Delay
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC, Low Thermal Resistance Packaging

DESCRIPTION

The UCC3912 Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time,and start-up delay. In the event of a constant fault, the Internal fixed 3% duty cycle ratio limits average output power.

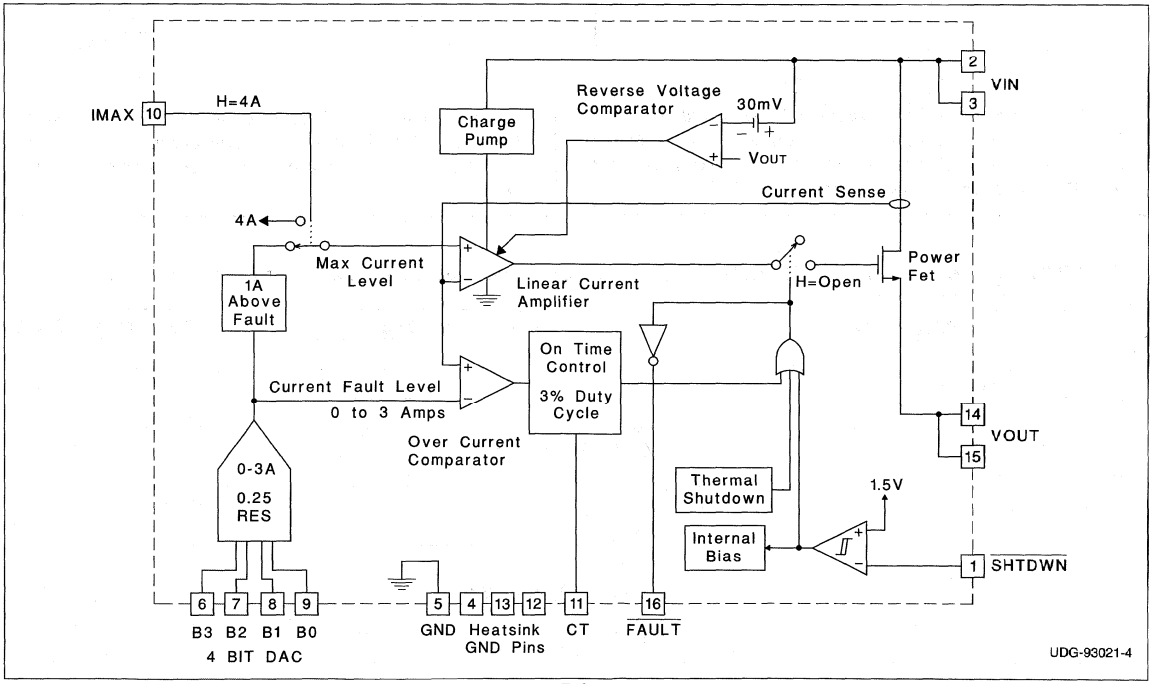
The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the fault level when driven low, and to a full 4A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging C_T. Once C_T charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

(continued)

5

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UCC3912 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr.

The UCC3912 can be put into sleep mode drawing only 1μA of supply current. The $\overline{\text{SHTDWN}}$ pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon start-up to achieve sequencing of power. Other features include an open drain Fault output indicator, Thermal Shutdown, Under Voltage Lockout, and a low thermal resistance Small outline package.

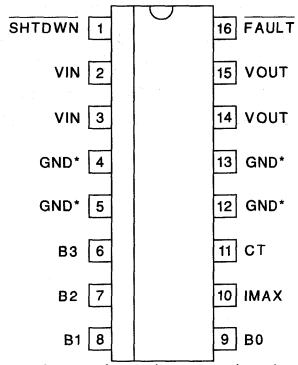
ABSOLUTE MAXIMUM RATINGS

$\overline{\text{VIN}}$ . . . . . +8 V
$\overline{\text{FAULT}}$ Sink Current 50mA
$\overline{\text{FAULT}}$ Voltage . . . . . –0.3 to V_{IN}
Output Current . . . . . Self Limiting
TTL Input Voltage . . . . . –0.3 to V_{IN}
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

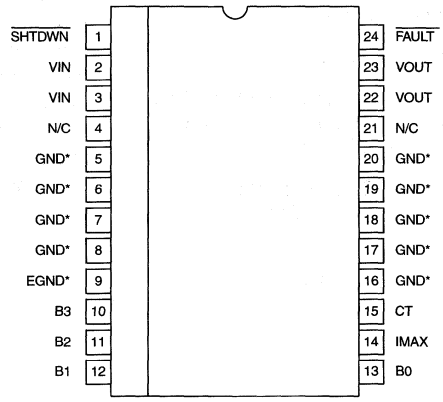
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
N, DP Package



**Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N package, pins 4, 12, and 13 are N/C.*

TSSOP-24 (Top View)
PWP Package



**Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_J = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{\text{SHTDWN}}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		3.0		8.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	$\overline{\text{SHTDWN}}$ = 0.2V		0.5	5.0	μA
Output Section					
Voltage Drop	I_{OUT} = 1A		0.15	0.22	V
	I_{OUT} = 2A		0.3	0.45	V
	I_{OUT} = 3A		0.45	0.68	V
	I_{OUT} = 1A, VIN = 3V		0.17	0.27	V
	I_{OUT} = 2A, VIN = 3V		0.35	0.56	V
	I_{OUT} = 3A, VIN = 3V		0.5	0.8	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_J = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{SHTDWN}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (cont.)					
Reverse Leakage	$V_{IN} < V_{OUT}$, V_{OUT} = 5V		5	20	µA
Initial Start-up Time	(Note 2)		100		µs
Short Circuit Response	(Note 2)		100		ns
Thermal Shutdown	(Note 2)		170		°C
Thermal Hysteresis	(Note 2)		10		°C
DAC Section					
Output Leakage	Code = 0000-0011		0	20	µA
Trip Current	Code = 0100	0.1	0.25	0.45	A
	Code = 0101	0.25	0.50	0.75	A
	Code = 0110	0.5	0.75	1.0	A
	Code = 0111	0.75	1.00	1.25	A
	Code = 1000	1.0	1.25	1.5	A
	Code = 1001	1.25	1.50	1.75	A
	Code = 1010	1.5	1.75	2.0	A
Trip Current	Code = 1011	1.7	2.00	2.3	A
	Code = 1100	1.9	2.25	2.58	A
	Code = 1101	2.1	2.50	2.9	A
	Code = 1110	2.3	2.75	3.2	A
	Code = 1111	2.5	3.0	3.5	A
Max Output Current	Code = 0000 to 0011			0.02	mA
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, IMAX = 0V	0.5	1.0	1.8	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, IMAX = 2.4V	3.0	4.0	5.2	A
Timer Section					
CT Charge Current	V_{CT} = 1.0V	-45.0	-36.0	-22.0	µA
CT Discharge Current	V_{CT} = 1.0V	0.72	1.2	1.5	µA
Output Duty Cycle	V_{OUT} = 0V	2.0	3.0	6.0	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			100		mV
Input Current	$\overline{SHTDWN}$ = 1V		100	500	nA
Fault Output Section					
Output Leakage Current				500	nA
Low Level Output Voltage	I_{OUT} = 10mA		0.4	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High	(can be connected to V_{IN})	2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	V_{IH} = 2.4V		3	10	µA
TTL Input Low Current	V_{IL} = 0.4V			1	µA

Note 1: *All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.*

Note 2: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

B0 - B3: These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as FAULT = $27.8 \bullet 10^3 \bullet$ CT. Once the fault time is reached the output will shutdown for a time given by: $T_{SD} = 833 \bullet 10^3 \bullet$ CT, this equates to a 3% duty cycle.

$\overline{\text{FAULT}}$: Open drain output which pulls low upon any condition which causes the output to open: Fault, Thermal Shutdown, or Shutdown.

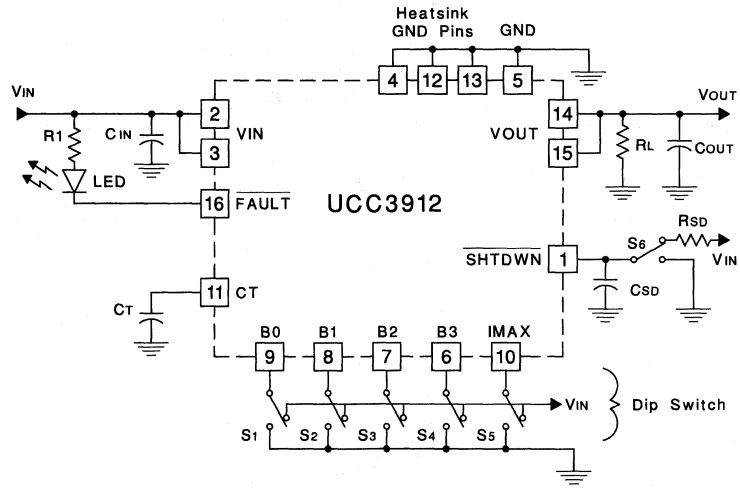
IMAX: When this pin is set to logic low the maximum sourcing current will always be 1A above the programmed fault level. When set to logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 1µA of Icc. The input threshold is hysteretic, allowing the user to program a start-up delay with an external RC circuit.

VIN: Input voltage to the UCC3912. The recommended voltage range is 3 to 8 volts. Both VIN pins should be connected together and to the power source.

VOUT: Output voltage from the UCC3912. When switched the output voltage will be approximately VIN - ($0.15\Omega \bullet I_{OUT}$). Both VOUT pins should be connected together and to the load.

APPLICATION INFORMATION



Note: For demonstration board schematic see Design Note DN-58.

UDG-93020-3

Figure 1. Evaluation circuit.

APPLICATION INFORMATION (cont.)

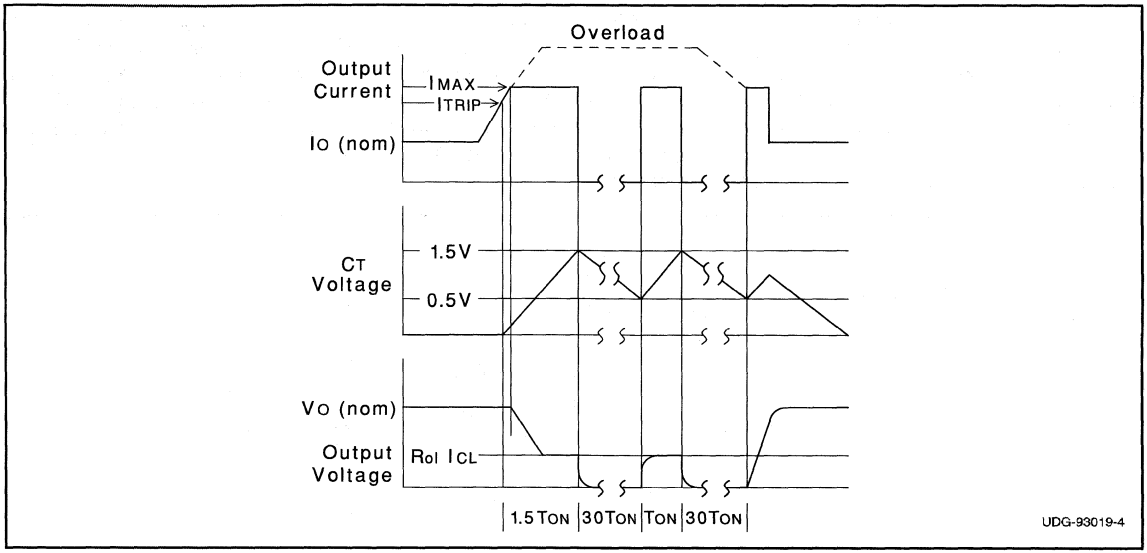


Figure 2. Load current, timing capacitor voltage, and output voltage of the UCC3912 under Fault conditions.

Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{28 \bullet 10^3 \bullet CT}{V_{OUT}} \right)$$

where V_{OUT} is the output voltage.

For a resistive load of value RL, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{28 \bullet 10^3 \bullet CT}{RL \bullet \ell n \left(\frac{1}{1 - \left(\frac{V_{OUT}}{I_{MAX} \bullet RL} \right)} \right)} \right)$$

APPLICATION INFORMATION (cont.)

The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor C_T charges with 36µA of current. If the fault occurs for the time it takes for C_T to charge up to 1.5V, the fault latch is set and the output switch is opened. The output remains opened until C_T discharges to 0.5V with a 1.2µA current source. Once the 0.5V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present then C_T will begin charging, starting the cycle over, resulting in approximately a 3% on time.

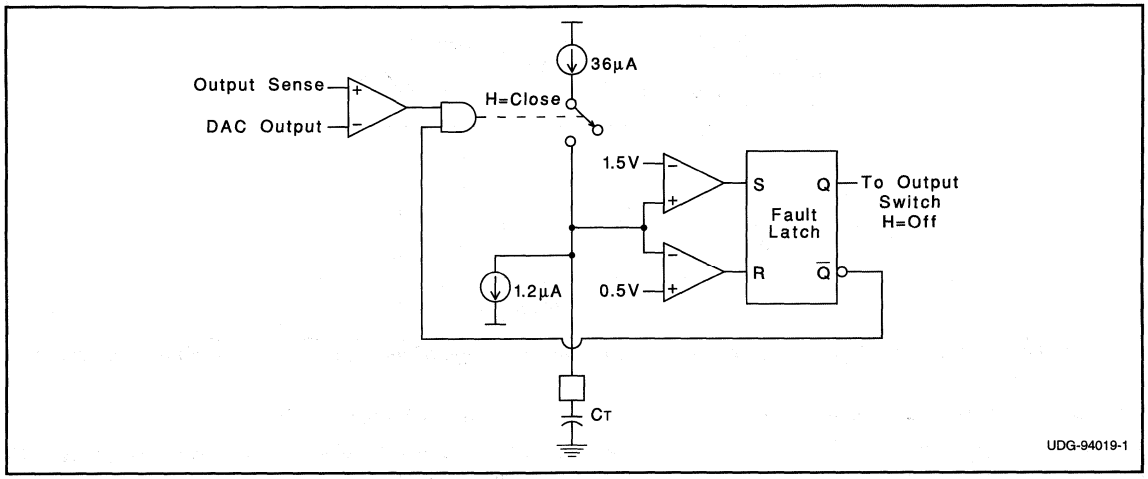


Figure 3. UCC3912 on time control circuitry.

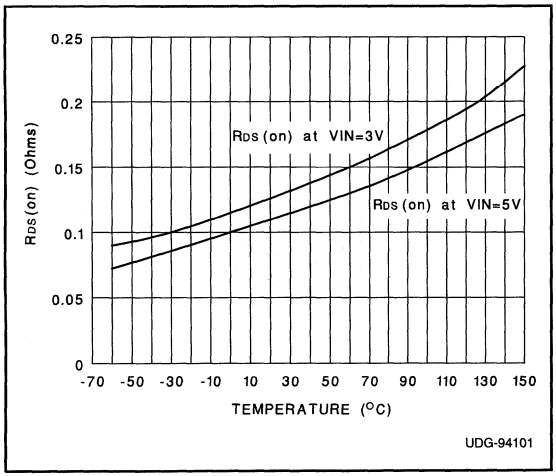


Figure 4. RDS(on) vs temperature at 2A load current.

SAFETY RECOMMENDATIONS

Although the UCC3912 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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UNITRODE

application INFO available

UCC1913
UCC2913
UCC3913

Negative Voltage Hot Swap Power Manager

FEATURES

- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable
- Overcurrent Limit
- Programmable Fault Time
- Fault Output Indication
- Shutdown Control
- Undervoltage Lockout
- 8-Pin SOIC

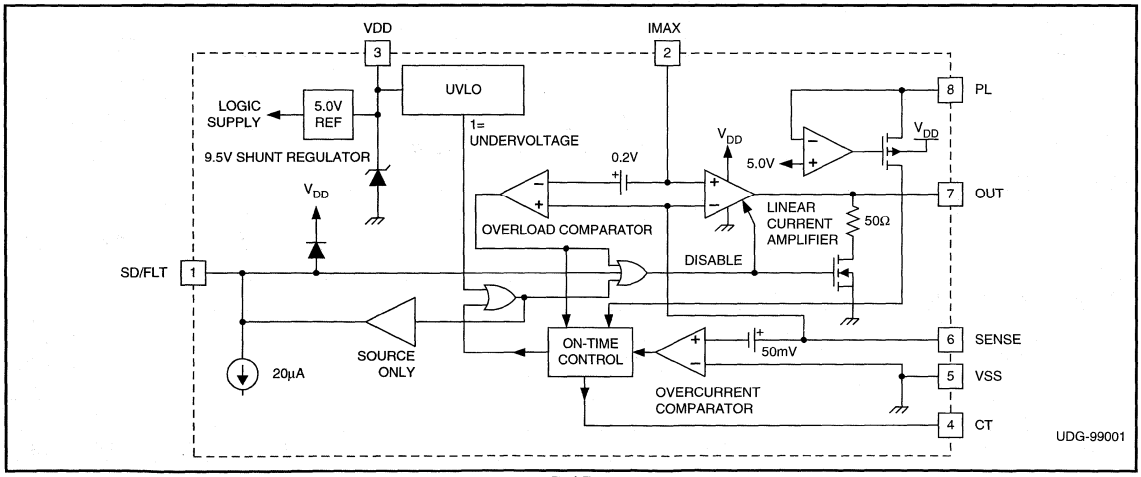
DESCRIPTION

The UCC1913 family of negative voltage circuit breakers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is driven through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The on-board 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on-time from less than 0.1% to a maximum of 3%. The duty cycle modulates depending on the current into the PL pin, which is a function of the voltage across the FET, and will limit average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on the IMAX pin. The current level, when the output appears as a current source, is equal to V_{IMAX}/R_{SENSE}. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by the IMAX pin, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later. When the output current reaches the maximum sourcing current level, the output appears as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC1913 family include undervoltage lockout, and 8-pin small outline (SOIC) and Dual-In-Line (DIL) packages.

BLOCK DIAGRAM



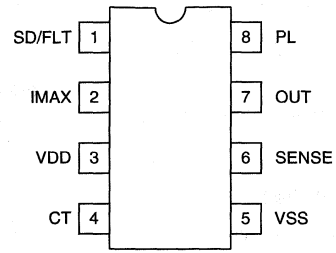
ABSOLUTE MAXIMUM RATINGS

I_{VCC} 50mA
SHUTDOWN Current 10mA
PL Current 10mA
IMAX Input Voltage VCC
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

All voltages are with respect to VSS (The most negative voltage). All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1913; –40°C to +85°C for UCC2913; 0°C to +70°C for UCC3913; I_{VDD} = 2mA, CT = 4.7pF, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1.0	2.0	mA
Regulator Voltage	I_{SOURCE} = 2mA to 10mA	8.5	9.5	10.5	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C	47.5	50	53	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1.0V, I_{PL} = 0	–50	–36	–22	µA
	Overload Condition, $V_{SENSE} - V_{IMAX}$ = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	V_{CT} = 1.0V, I_{PL} = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.4	2.6	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%
Output Section					
Output High Voltage	I_{OUT} = 0A	8.5	10		V
	I_{OUT} = –1mA	6	8		V
Outut Low Voltage	I_{OUT} = 0A; $V_{SENSE} - V_{IMAX}$ = 100mV		0	0.01	V
	I_{OUT} = 2mA; $V_{SENSE} - V_{IMAX}$ = 100mV		0.2	0.6	V
Linear Amplifier Section					
Sense Control Voltage	IMAX = 100mV	85	100	115	mV
	IMAX = 400mV	370	400	430	mV
Input Bias			50	500	nA
Shutdown/Fault Section					
Shutdown Threshold		1.4	1.7	2.0	V
Input Current	Shutdown = 5V	15	25	45	µA
Fault Output High		6	7.5	9	V
Fault Output Low			0	0.01	V
Delay to Output	(Note 1)		150	300	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1913; –40°C to +85°C for UCC2913; 0°C to +70°C for UCC3913; I_{VDD} = 2mA, CT = 4.7pF, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PL} = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	I_{PL} = 64µA	0.6	1.2	1.7	%
	I_{PL} = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	(Note 1)		300	500	ns
Output Sink Current	$V_{SENSE} = V_{IMAX}$ = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$T_{FAULT} = \frac{(2 \bullet CT)}{I_{CH}}$$

where

$$I_{CH} = 36\mu A + I_{PL},$$

and I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 2 \bullet 106 \bullet CT$$

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on the imax pin, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: Output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL}>>36µA then the average MOSFET power dissipation is given by:

$$P_{FET(avg)} = IMAX \bullet 1 \bullet 10^{-6} \bullet R_{PL}$$

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and CT starts to charge.

SD/FLT: This pin provides fault output indication and shutdown control. Interface into and out of this pin is usually performed through level shift transistors. When 20µA is sourced into this pin, shutdown drives high causing the output to disable the NMOS pass device. When opened, and under a non-fault condition, the SD/FLT pin will pull to a low state. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state, indicating the output FET is off.

VDD: Current driven with a resistor to a voltage at least 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD at 10V above the VSS pin, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

APPLICATION INFORMATION

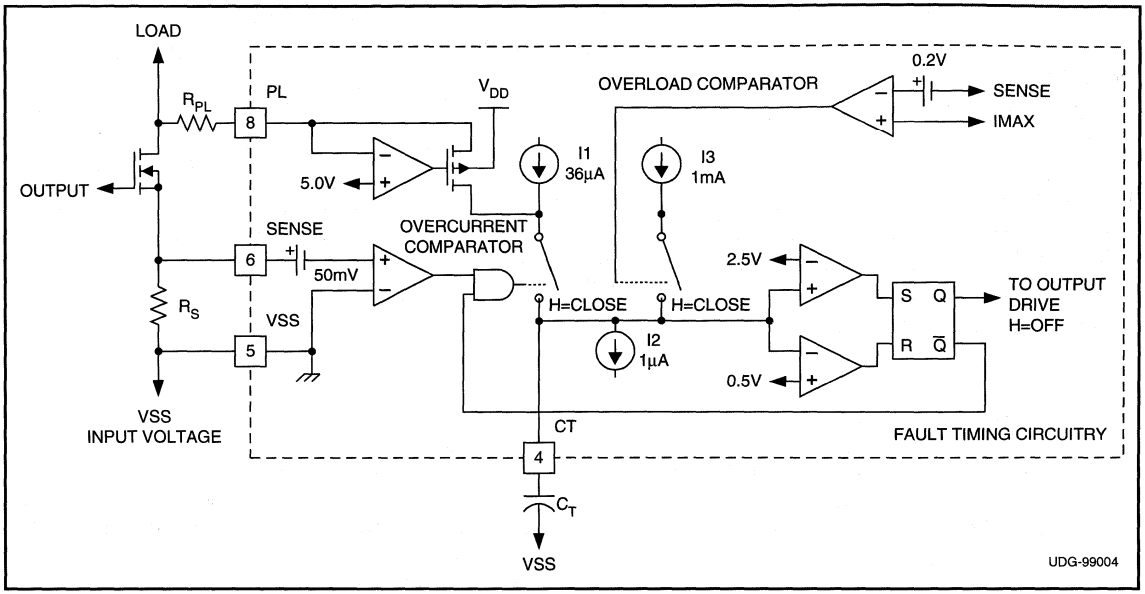


Figure 1. Fault timing circuitry for the UCC1913, including power limit overload.

Figure 1 shows the detailed circuitry for the fault timing function of the UCC1913. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, R_S, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36µA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

Where V_{FET} is the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, V_{OUT} ~ VSS (input voltage), I_{PL} = 0, the CT charging current is 36µA.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to begin. Under a constant fault, the duty cycle is given by:

$$Duty\ Cycle = \frac{1\mu A}{I_{PL} + 36\mu A}$$

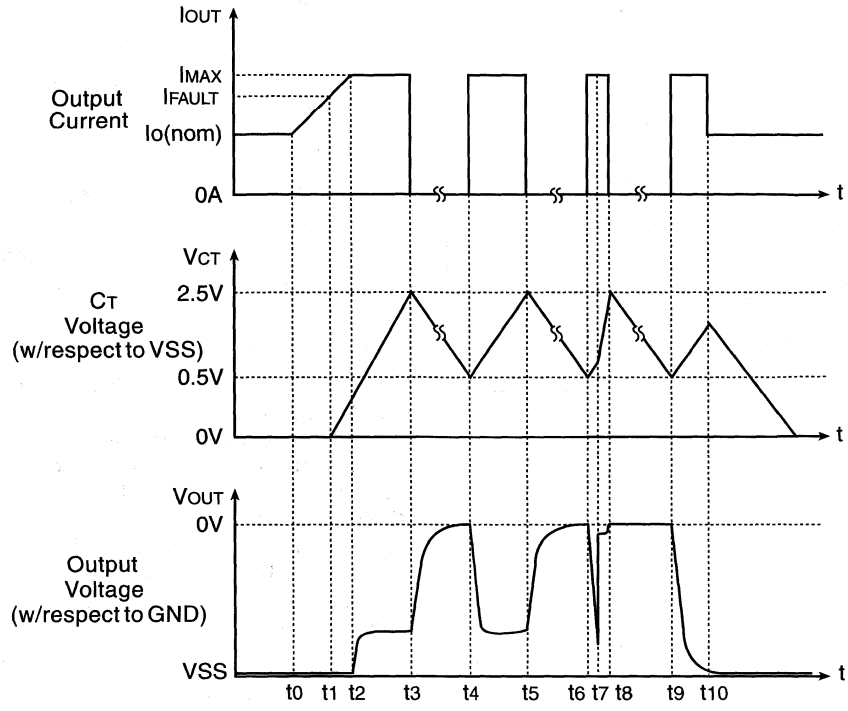
Average power dissipation in the pass element is given by:

$$P_{FET(avg)} = V_{FET} \bullet IMAX \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

where V_{FET} >> 5V I_{PL} can be approximated as : $\frac{V_{FET}}{R_{PL}}$

and where I_{PL}>>36µA, the duty cycle can be approximated as :

APPLICATION INFORMATION (cont.)



t0: safe condition – output current is nominal, output voltage is at the negative rail, VSS.

t1: fault control reached – output current rises above the programmed fault value, CT begins to charge at ≅ 36µA.

t2: max current reached – output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: fault occurs – CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground.

t4: retry – CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down to VSS.

t5: t5 = t3: illustrates 3%duty cycle.

t6: t6 = t4

t7: output short circuit - if V_{OUT} is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.

t8: fault occurs – output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9: t9 = t4; output short circuit released, still in fault mode.

t10: t10 = t0; fault released, safe condition – return to normal operaton of the circuit breaker.

Figure 2. Typical timing diagram.

APPLICATION INFORMATION (cont.)

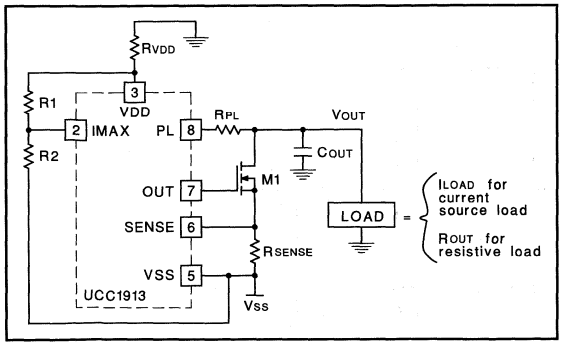


Figure 3.

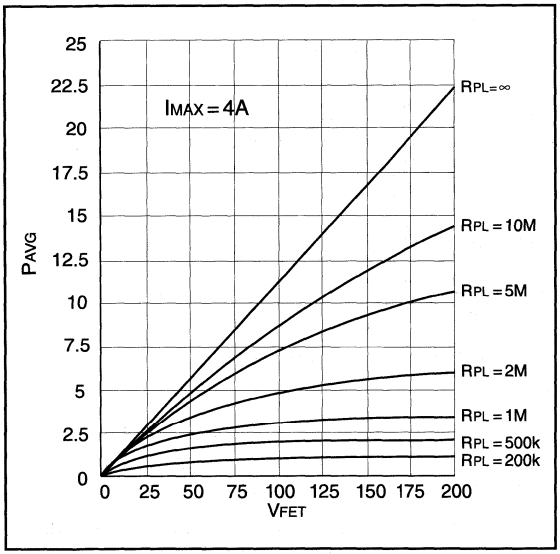


Figure 4. Plot average power vs. FET voltage for increasing values of R_{PL}.

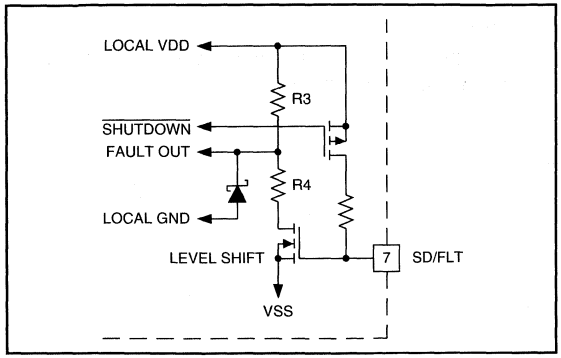


Figure 5. Possible level shift circuitry to interface to the UCC1913.

$$\frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET(avg)} =$$

$$V_{FET} \bullet IMAX \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}} = IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels. therefore, average power dissipation is limited in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC1913 ensures that the output NMOS does not pass more than I_{MAX} (which is V_{IMAX}/R_S). In the event the output current exceeds the programmed I_{MAX} by 0.2V/R_S, which can only occur if the output FET is not responding to a command from the IC, the CT pin will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SD/FLT pin, and also since the voltage on CT will only charge past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build in redundancy in the system.

Determining External Component Values

Referring now to Figure 3. To set R_{VDD} the following must be achieved:

$$\frac{V_{IN(\min)}}{R_{VDD}} > \frac{10V}{(R1+R2)} + 2mA$$

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic below as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate $C_{T(min)}$.

Now, given the values of C_{OUT}, Load, R_{SENSE}, VSS, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for CT to charge to 2.5V (relative to VSS), and is the basis for estimating the minimum value of CT. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

APPLICATION INFORMATION (cont.)

Next, the variable I_{MAX} must be calculated. I_{MAX} is the maximum current that the UCC1913 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value I_{MAX} where:

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}}$$

where V_{IMAX} = voltage on pin IMAX.

Given this information, calculation of the startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |VSS|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = C_{OUT} \bullet R_{OUT} \bullet \ell n\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |VSS|}\right)$$

Once T_{START} is calculated, the power limit feature of the UCC1913 must be addressed and component values derived. Assuming the user chooses to limit the maximum allowable average power that will be associated with the circuit breaker, the power limiting resistor, R_{PL}, can be easily determined by the following:

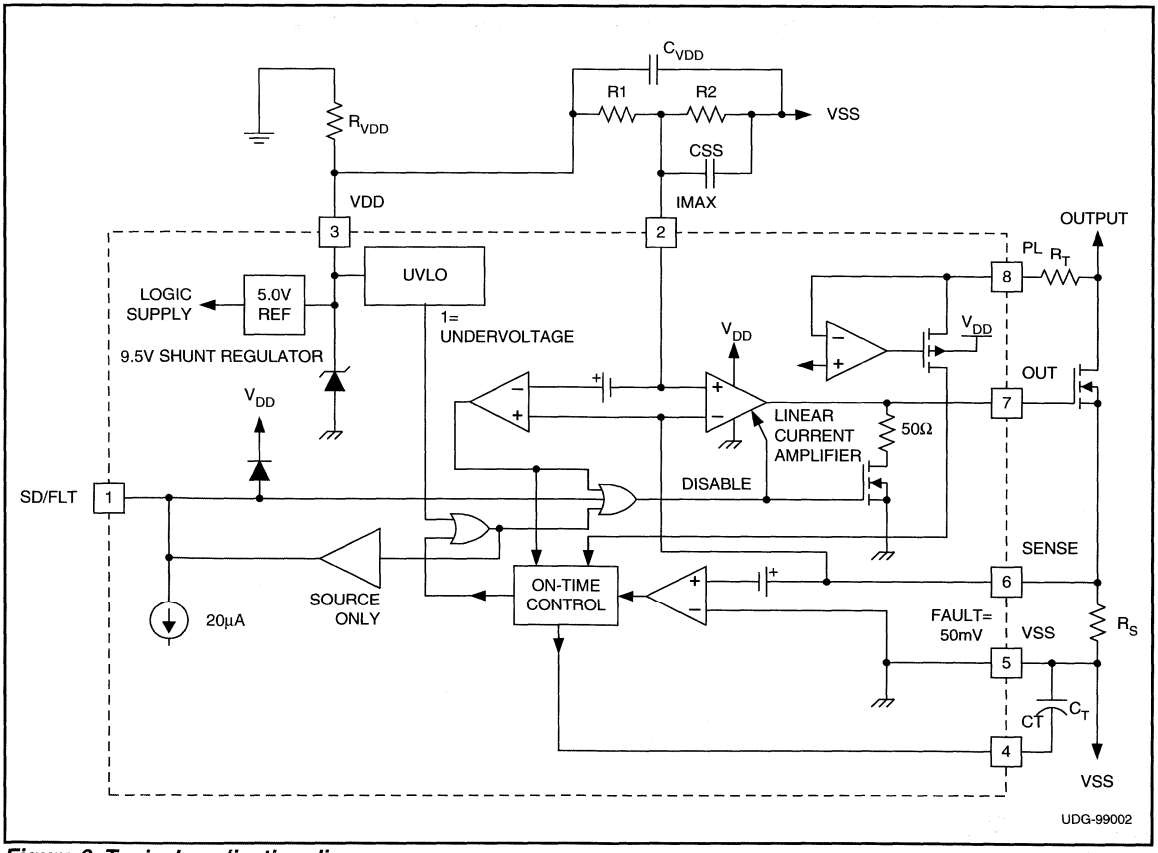


Figure 6. Typical application diagram.

APPLICATION INFORMATION (cont.)

$$R_{PL} = \frac{P_{FET(avg)}}{1\mu A \bullet I_{MAX}}$$

where a minimum R_{PL} exists defined by $R_{PL(min)} = \frac{|VSS|}{5mA}$

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_{T(min)} = \frac{(3 \bullet T_{START} \bullet 62\mu A \bullet R_{PL} + |VSS| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_{T(min)} = \frac{3 \bullet T_{START}(31\mu A \bullet R_{PL} + |VSS| - 5V - I_{MAX} \bullet R_{OUT})}{5 \bullet R_{PL}} + \frac{3 \bullet R_{OUT} \bullet |VSS| \bullet C_{OUT}}{5 \bullet R_{PL}}$$

SAFETY RECOMENDATION

Although the UCC3913 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3913 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3913 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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5V to 35V Hot Swap Power Manager

FEATURES

- 5V to 35V Operation
- Precision Maximum Current Control
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Overcurrent Limit
- Shutdown Control
- Charge Pump for Low RDSON High-Side Drive
- Latch Reset Function Available
- Output Drive VGS Clamping
- Fault Output Indication
- 18 Pin DIL and SOIC Packages

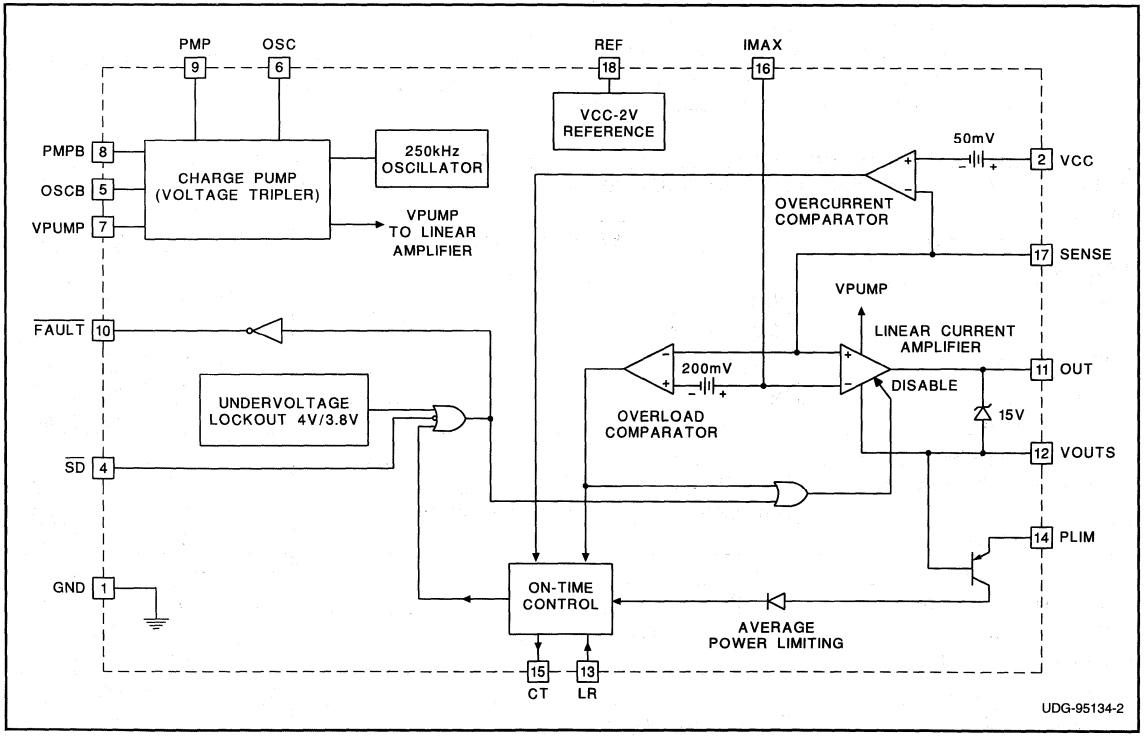
DESCRIPTION

The UC3914 family of Hot Swap Power Managers provides complete power management, hot swap and fault handling capability. Integrating this part and a few external components, allows a board to be swapped in or out upon failure or system modification without removing power to the hardware, while maintaining the integrity of the powered system. Complementary output drivers and diodes have been integrated for use with external capacitors as a charge pump to ensure sufficient gate drive to the external NMOS transistor for low RDS_{ON}. All control and housekeeping functions are integrated and externally programmable and include the fault current level, maximum output sourcing current, maximum fault time and average power limiting of the external FET. The UC3914 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The fault level is fixed at 50mV with respect to VCC to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed by using a resistor divider from VCC to REF to set the voltage on IMAX. The maximum current level, when the output appears as a current source is $(VCC - V_{IMAX})/R_{SENSE}$.

(continued)

5

BLOCK DIAGRAM



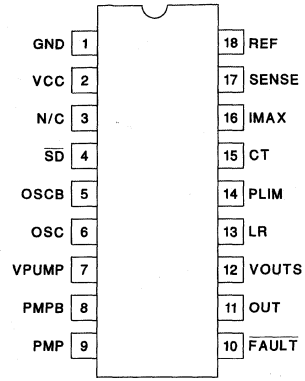
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, VCC 40V
Maximum Forced Voltage
  SD 12V
  IMAX VCC
  LR 12V
Maximum Current
  FAULT 20mA
  PLIM 10mA
Maximum Voltage, FAULT 40V
Reference Output Current . . . . . Internally Limited
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are referenced to ground. Currents are positive into, negative out of specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-18, SOIC-18 (Top View)
N or J Package, DW Package



DESCRIPTION (cont.)

When the output current is less than the fault level, the external output transistor remains switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts to charge C_T, a timing capacitor. Once C_T charges to 2.5V, the output device is turned off and C_T is slowly discharged. Once C_T is discharged to 0.5V, the IC performs a retry and the output transistor is switched on again. The UC3914 offers two distinct reset modes. In one mode with LR left floating or held low, the IC will repeatedly try to reset itself if a fault occurs as described above. In the second mode with LR held high, once a fault occurs, the output is latched off until either LR is toggled low, the part is shutdown then re-enabled using SD, or the power to the part is turned off and then on again.

This part is offered in both 18 pin DW Wide-Body (SOIC) and Dual-In-Line (DIL) packages.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, V_{PUMP} = V_{PUMP}(max), SD = 5V, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Section					
Icc	(Note 2)		8	15	mA
	VCC = 35V, (Note 2)		12	20	mA
Shutdown Icc	SD = 0V		500	900	µA
UVLO	Turn on threshold		4	4.4	V
UVLO Hysteresis		100	200	350	mV
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C, with respect to VCC	–55	–50	–45	mV
	Over operating temperature, with respect to VCC	–57	–50	–42	mV
IMAX Input Bias			1	3	µA
CT Charge Current	CT = 1V	–140	–100	–60	µA
CT Discharge Current	CT = 1V	2	3	4.5	µA
CT Charge Current	CT = 1V, Overload condition	–6	–3	–1.5	mA
CT Fault Threshold		2.25	2.5	2.75	V
CT Reset Threshold		0.45	0.5	0.55	V
Output Duty Cycle	Fault condition, I_{PL} = 0	1.5	3	4.5	%

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, V_{PUMP} = V_{PUMP}(max), $\overline{SD}$ = 5V, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max, with respect to VPUMP	–1.5	–1		V
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max, IOUT = –2mA, with respect to VPUMP	–2	–1.5		V
OUT Low Voltage	I_{OUT} = 0		0.8	1.3	V
	I_{OUT} = 5mA		1	2	V
	I_{OUT} = 25mA, Overload Condition, VOUTS = 0V		1.2	1.8	V
OUT Clamp Voltage	VOUTS = 0V	11.5	13	14.5	V
Rise Time	C_{OUT} = 1nF (Note 1)		750	1250	ns
Fall Time	C_{OUT} = 1nF (Note 1)		250	500	ns
Charge Pump Section					
OSC, OSCB Frequency		60	150	250	kHz
OSC, OSCB Output High	I_{OSC} = –5mA	10	11	11.6	V
OSC, OSCB Output Low	I_{OSC} = 5mA		0.2	0.5	V
OSC, OSCB Output Clamp Voltage	VCC = 25	18.5	20.5	22.5	V
OSC, OSCB Output Current Limit	High Side Only	–20	–10	–3	mA
Pump Diode Voltage Drop	I_{DIODE} = 10mA, Measured from PMP to PMPB, PMPB to VPUMP	0.5	0.9	1.3	V
PMP Clamp Voltage	VCC = 25	18.5	20.5	22.5	V
VPUMP Maximum Voltage	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Disabled	20	22	24	V
	VCC = 35V, VOUTS = VCC, Voltage Where Charge Pump Disabled	42	45	48	V
VPUMP Hysteresis	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Re-enabled	0.3	0.7	1.4	V
	VCC = 35V, VOUTS = VCC, Charge Pump Re-enabled	0.25	0.7	1.4	V
Linear Current Section					
Input Offset Voltage		–15	0	15	mV
Voltage Gain		60	80		dB
IMAX Control Voltage	IMAX = OUT, SENSE = VCC, with respect to VCC	–20	0	20	mV
	IMAX = OUT, SENSE = REF, with respect to REF	–20	0	20	mV
SENSE Input Bias			1.5	3.5	µA
Reference Section					
REF Output Voltage	With respect to VCC	–2.25	–2	–1.75	V
REF Current Limit		12.5	20	50	mA
Load Regulation	I_{VREF} = 1mA to 5mA		25	60	mV
Line Regulation	VCC = 5V to 35V		25	100	mV
Shutdown Section					
Shutdown Threshold		0.6	1.5	2	V
Input Current	$\overline{SD}$ = 5V		150	300	µA
Delay to Output	(Note 1)		0.5	2	µs
Fault Section					
Fault Output Low	I_{FAULT} = 1mA		100	200	mV
Fault Output Leakage	V_{FAULT} = 35V		10	500	nA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, V_{PUMP} = V_{PUMP}(max), $\overline{SD}$ = 5V, CP1 = CP2 = C_{PUMP} = 0.01µF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Latch Section					
LR Threshold	High to Low	0.6	1.4	2	V
Input Current	LR = 5V		500	750	µA
Power Limiting Section					
Duty Cycle Control	In Fault, I_{PLIM} = 200µA	0.6	1.3	2.0	%
	In Fault, I_{PLIM} = 3mA	0.05	0.12	0.2	%
Overload Section					
Delay to Output	(Note 1)		500	1250	ns
Threshold	Respect to IMAX	–250	–200	–150	mV

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: A mathematical averaging is used to determine this value. See Application Section for more information.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The minimum fault time must be more than the time to charge external load capacitance. The fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet CT}{I_{CH}}$$

where I_{CH} = 100µA + I_{PL}, where I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = \frac{2 \bullet CT}{I_{DIS}}$$

where I_{DIS} is nominally 3µA.

$\overline{FAULT}$: Open collector output which pulls low upon any of the following conditions: Timer fault, Shutdown, UVLO. This pin **MUST** be pulled up to VCC or another supply through a suitable impedance.

GND: Ground reference for the IC.

IMAX: This pin programs the maximum allowable sourcing current. Since REF is a –2V reference (with respect to VCC), a voltage divider can be derived from VCC to REF in order to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin, with respect to VCC, divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on IMAX to VCC.

LR: If this pin is held high and a fault occurs, the timer will be prevented from resetting the fault latch when CT is discharged below the reset comparator threshold. The part will not retry until this pin is brought to a logic low or a power-on-reset occurs. Pulling this pin low before the reset time is reached will not clear the fault until the reset time is reached. Floating or holding this pin low will result in the part repeatedly trying to reset itself if a fault occurs.

OUT: Output drive to the MOSFET pass element. Internal clamping ensures that the maximum V_{GS} drive is 15V.

OSC, OSCB: Complementary output drivers for intermediate charge pump stages. A 0.01µF capacitor should be placed between OSC and PMP, and OSCB and PMPB.

PLIM: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to VCC. Current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the typical 3% level. When I_{PL} >> 100µA then the average MOSFET power dissipation is given by: P_{FET_AVG} = IMAX • 3 • 10^{-6} • R_{PL}.

PMP, PMPB: Complementary pins which couple charge pump capacitors to internal diodes and are used to provide charge to the reservoir capacitor tied to VPUMP. Typical capacitor values used are 0.01µF.

REF: –2V reference with respect to VCC used to program the IMAX pin voltage. A 0.1µF ceramic or tantalum capacitor **MUST** be tied between this pin and VCC to ensure proper operation of the chip.

$\overline{SD}$: When this TTL compatible input is brought to a logic low, the output of the linear amplifier is driven low, $\overline{FAULT}$ is pulled low and the IC is put into a low power mode. The **ABSOLUTE** maximum voltage that can be placed on this pin is 12V.

PIN DESCRIPTIONS (cont.)

SENSE: Input voltage from current sense resistor. When there is greater than 50mV across this pin with respect to VCC, a fault is sensed and C_T begins to charge.

VCC: Input voltage to the IC. Typical voltages are 4.5V to 35V. The minimum input voltage required for operation is 4.5V.

VOUTS: Source connection of external N-channel MOSFET and sensed output voltage of load.

VPUMP: Charge pump output voltage. A capacitor should be tied between this pin and VOUTS with a typical value being 0.01µF.

TYPICAL CHARACTERISTIC CURVES

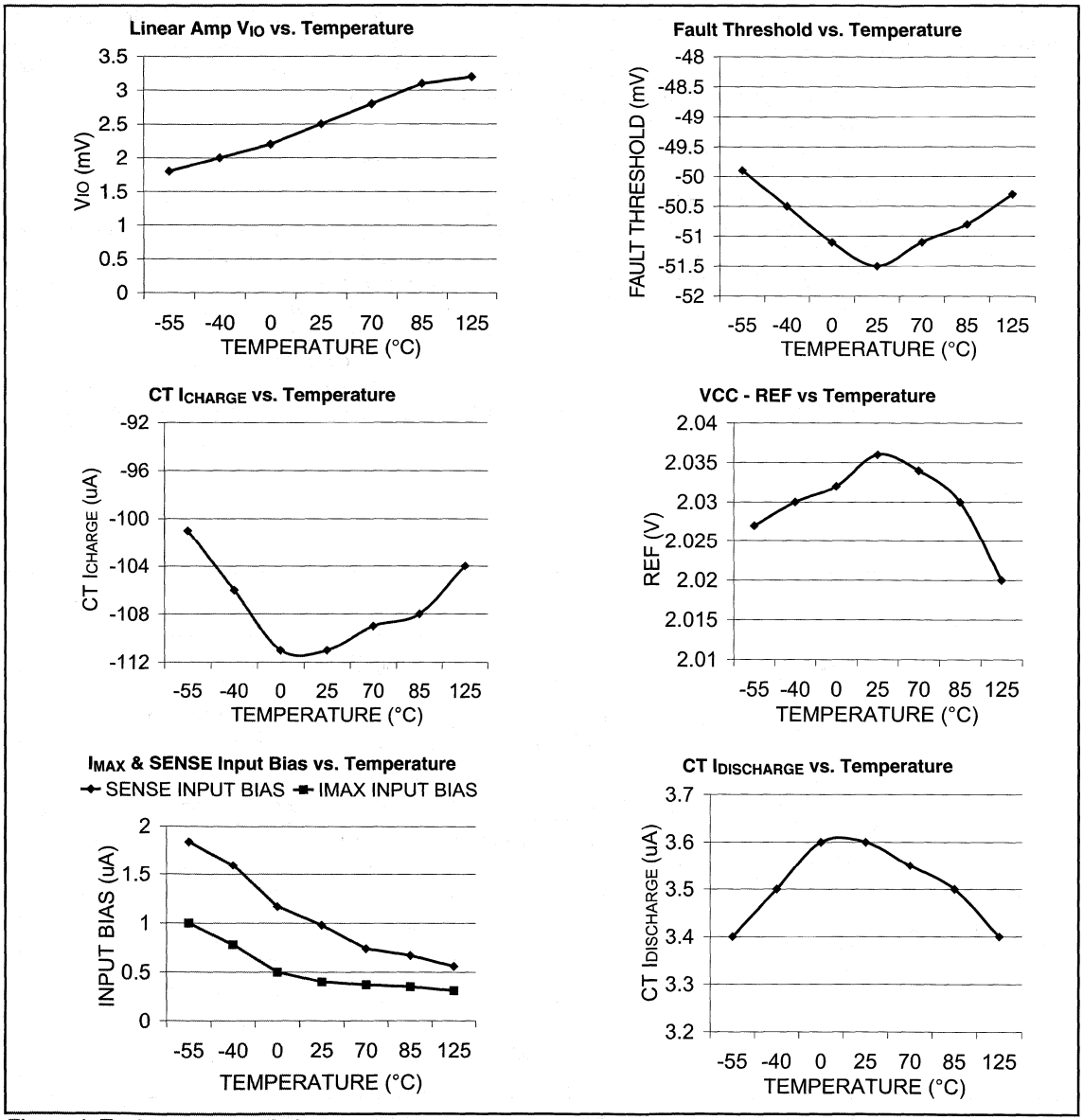


Figure 1. Typical characteristic curves.

APPLICATION INFORMATION

The UC3914 is to be used in conjunction with external passive components and an N-channel MOSFET (NMOS) to facilitate hot swap capability of application modules. A typical application set-up is given in Figure 9. The term hot swap refers to the system requirement that submodules be swapped in or out upon failure or system modification without removing power to the operating hardware. The integrity of the power bus must not be compromised due to the addition of an unpowered module. Significant power bus glitches can occur due to the substantial initial charging current of on-board module bypass capacitance and other load conditions (for more information on hot swapping and power management applications, see Application Note U-151). The UC3914 provides protection by monitoring and controlling the output current of an external NMOS to charge this capacitance and provide load current. The addition of the NMOS, a sense resistor, R_{SENSE}, and two other resistors, R1 and R2, sets the programmed maximum current level the NMOS can source to charge the load in a controlled manner. The equation for this current, I_{MAX}, is:

$$I_{MAX} = \frac{V_{CC} - V_{IMAX}}{R_{SENSE}}$$

where V_{IMAX} is the voltage generated at the IMAX pin. Analysis of the application circuit shows that V_{IMAX} (with respect to GND) can be defined as:

$$V_{IMAX} = V_{REF} + \frac{(V_{CC} - V_{REF}) \bullet R1}{R1 + R2} = \frac{2V \bullet R1}{R1 + R2} + V_{REF}$$

where V_{REF} is the voltage on the REF pin and whose internally generated potential is two volts below VCC. The UC3914 also has an internal overcurrent comparator which monitors the voltage between SENSE and VCC. If this voltage exceeds 50mV, the comparator determines that a fault has occurred, and a timing capacitor, C_T, will begin to charge. This can be rewritten as a current which causes a fault, I_{FAULT}:

$$I_{FAULT} = \frac{50mV}{R_{SENSE}}$$

Fault Timing

Figure 2 shows the circuitry associated with the fault timing function of the UC3914. A typical fault mode, where the overload comparator and current source I3 do not factor into operation (switch S2 is open), will first be considered. Once the voltage across R_{SENSE} exceeds 50mV, a fault has occurred. This causes the timing capacitor, C_T, to charge with a combination of 100µA (I1) plus the current from the power limiting circuitry (I_{PL}).

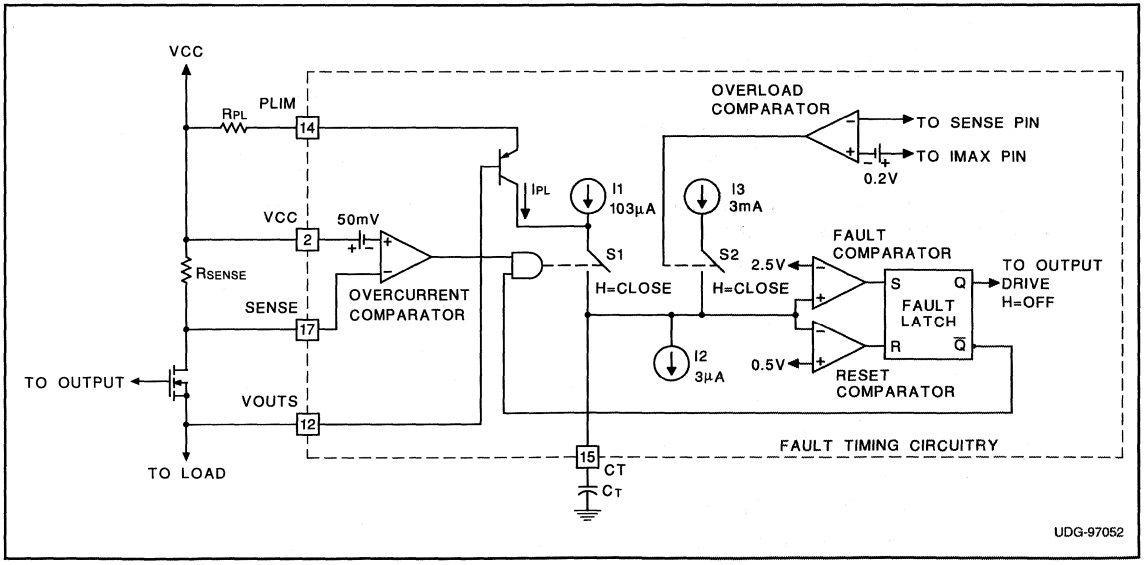
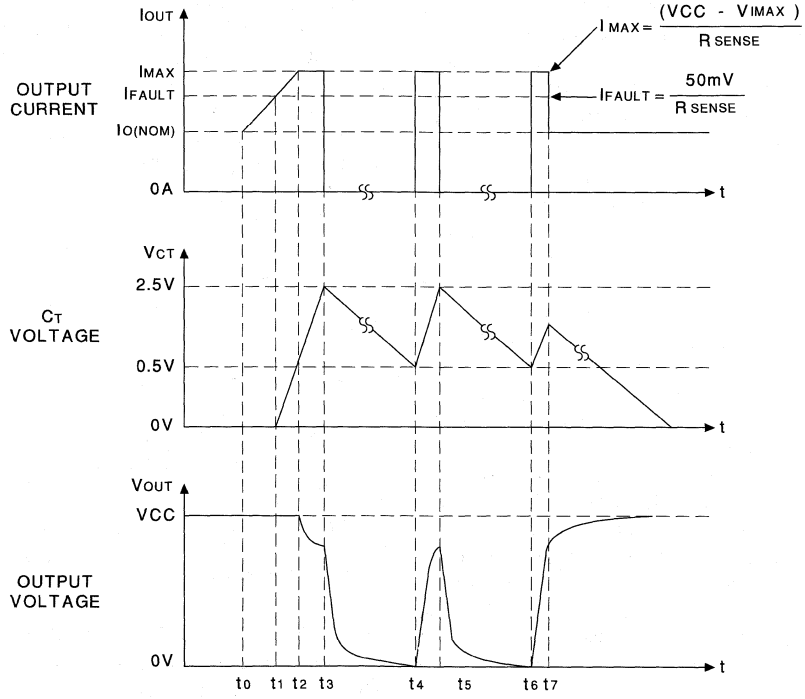


Figure 2. Fault timing circuitry for the UC3914, including power limit and overcurrent.

APPLICATION INFORMATION (cont.)

Figure 3a shows typical fault timing waveforms for the external NMOS output current, the voltage on the CT pin, and the output load voltage, V_{OUT}, with LR left floating or grounded. The output voltage waveforms have assumed an RC characteristic load and time constants will vary depending upon the component values. Prior to time to, the load is fully charged to almost VCC and the NMOS is supplying the current, I_O, to the load. At to, the current begins to ramp up due to a change in the load conditions until, at t1, the fault current level, I_{FAULT}, has been reached to cause switch S1 to close. This results in C_T being charged with the current sources I1 and I_{PL}. During this time, V_{OUT} is still almost equal to VCC except for small losses from voltage drops across the sense resistor and the NMOS. The output current reaches the programmed maximum level, I_{MAX}, at t2. The C_T voltage continues to rise since I_{MAX} is still greater than I_{FAULT}. The load output voltage drops because the current load requirements have become greater than the controlled maximum sourcing current. The C_T voltage reaches the upper comparator threshold (Figure 2) of 2.5V at t3, which promptly shuts off the gate drive to the NMOS (not



to: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, C_T begins to charge with ≅ 100µA + I_{PL}.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - C_T has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Retry - C_T has discharged to 0.5V, but fault current is still exceeded, C_T begins charging again, FET is on, VOUT increases.

t5 = t3: Illustrates <3% duty cycle depending upon R_{PL} selected.

t6 = t4

t7 = to: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 3a: Typical timing diagram.

APPLICATION INFORMATION (cont.)

shown but can be inferred from the fact that no output current is provided to the load), latches in the fault and opens switch S1 disconnecting the charging currents I1 and I_{PL} from C_T. Since no output current is supplied, the load voltage decays at a rate determined by the load characteristics and the capacitance. The 3µA current source, I2, discharges CT to the 0.5V reset comparator threshold. This time is significantly longer than the charging time and is the basis for the duty cycle current limiting technique. When the C_T voltage reaches 0.5V at t_4, the part performs a retry, allowing the NMOS to again source current to the load and cause V_{OUT} to rise. In this particular example, I_{MAX} is still sourced by the NMOS at each attempted retry and the fault timing sequence is repeated until time t_7 when the load requirements change to I_O. Since I_O is less than the fault current level at this time, switch S1 is opened, I2 discharges C_T and V_{OUT} rises to almost VCC.

Figure 3b shows fault timing waveforms similar to those depicted in Figure 3a except that the latch reset (LR) function is utilized. Operation is the same as described above until t_4 when the voltage on CT reaches the reset threshold. Holding LR high prevents the latch from being reset, preventing the IC from performing a retry (sourcing current to the load). The UC3914 is latched off until either LR is pulled to a logic low, or the chip is forced into an under voltage lockout (UVLO) condition and back out of UVLO causing the latch to automatically perform a power on reset. Figure 3b illustrates LR being toggled low at t_5, causing the part to perform a retry. Time t_6 again illustrates what happens when a fault is detected. The LR pin is toggled low and back high at time t_7, prior to the voltage on the CT pin hitting the reset threshold. This information tells the UC3914 to allow the part to perform a retry when the lower reset threshold is reached, which occurs at t_8. Time t_9 corresponds to when load conditions change to where a fault is not present as described for Figure 3a.

Power Limiting

The power limiting circuitry is designed to only source current into the CT pin. To implement this feature, a resistor, R_{PL}, should be placed between VCC and PLIM. The current, I_{PL} (show in Figure 2) is given by the following expression:

$$I_{PL} = \frac{V_{CC} - V_{OUTS}}{R_{PL}}, \text{ for } V_{OUTS} > 1V + V_{CT}$$

where V_{CT} is the voltage on the CT pin. For $V_{OUTS} < 1V + V_{CT}$ the common mode range of the power limiting circuitry causes $I_{PL} = 0$ leaving only the 100µA current source to charge C_T. $V_{CC} - V_{OUTS}$ represents the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a fault condition where the output current is just above the fault level, but less than the maximum level, $V_{OUTS} \sim$ VCC, $I_{PL} = 0$ and the C_T charging current is 100µA.

During a fault, the CT pin will charge at a rate determined by the internal charging current and the external timing capacitor, C_T. Once C_T charges to 2.5V, the fault comparator trips and sets the fault latch. When this occurs, OUT is pulled down to VOUTS, causing the external NMOS to shut off and the charging switch, S1, to open. C_T will be discharged with I2 until the C_T potential reaches 0.5V. Once this occurs, the fault latch will reset (unless LR is being held high, whereby a fault can only be cleared by pulling this pin low or going through a power-on-reset cycle), which re-enables the output of the linear amplifier and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$Duty\ Cycle = \frac{3\mu A}{I_{PL} + 100\mu A}$$

Average power dissipation can be limited using the PLIM pin. Average power dissipation in the pass element is given by:

$$PFETavg = (VCC - V_{OUTS}) \bullet I_{MAX} \bullet Duty\ Cycle$$

$$= (VCC - V_{OUTS}) \bullet I_{MAX} \bullet \frac{3\mu A}{I_{PL} + 100\mu A}$$

VCC – VOUTS is the drain to source voltage across the FET. When IPL >> 100µA, the duty cycle equation given above can be rewritten as:

$$Duty\ Cycle = \frac{RPL + 3\mu A}{(VCC - VOUTS)}$$

and the average power dissipation of the MOSFET is given by:

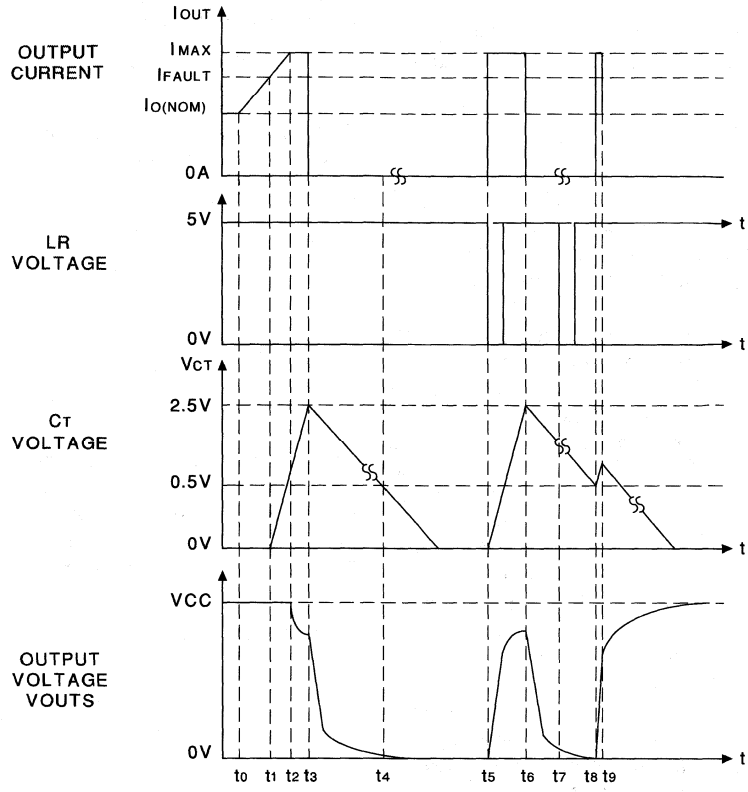
$$PFETavg$$

$$= (VCC - VOUTS) \bullet IMAX \bullet \frac{RPL + 3\mu A}{(VCC - VOUTS)}$$

$$= IMAX \bullet RPL \bullet 3\mu A$$

The average power is limited by the programmed IMAX current and the appropriate value for R_{PL}.

APPLICATION INFORMATION (cont.)



t0: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 100μA + IPL.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Reset comparator threshold reached but no retry since LR pin held high.

t5: LR toggled low, NMOS turned on and sources current to load.

t6 = t3

t7: LR toggled low before VCT reaches reset comparator threshold, causing retry.

t8: Since LR toggled low during present cycle, NMOS turned on and sources current to load.

t9 = t0: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 3b. Typical timing diagram utilizing LR (Latch Reset) function.

APPLICATION INFORMATION (cont.)

Overload Comparator

The linear amplifier in the UC3914 ensures that the external NMOS does not source more than the current IMAX, defined above as:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

In the event that output current exceeds the programmed IMAX by more than 200mV/R_{SENSE}, the output of the linear amplifier will immediately be pulled low (with respect to VOUTS) providing no gate drive to the NMOS, and preventing current from being delivered to the load. This situation could occur if the external NMOS is not responding to a command from the IC or output load conditions change quickly to cause an overload condition before the linear amplifier can respond. For example, if the NMOS is sourcing current into a load and the load suddenly becomes short circuited, an overload condition may occur. The short circuit will cause the V_{GS} of the NMOS to immediately increase, resulting in increased load current and voltage drop across R_{SENSE}. If this drop exceeds the overload comparator threshold, the amplifier output will be quickly pulled low. It will also cause the CT pin to begin charging with I3, a 3mA current source (refer to Figure 2) and continue to charge until approximately one volt below VCC, where it is clamped. This allows a constant fault to show up on $\overline{\text{FAULT}}$ and since the voltage on CT will only charge past 2.5V in an overload fault condition, it can be used for detection of output NMOS failure or to build redundancy into the system.

Estimating Minimum Timing Capacitance

The startup time of the IC may not exceed the fault time for the application. Since the timing capacitor, CT, determines the fault time, its minimum value can be determined by calculating the startup time of the IC. The startup time is dependent upon several external components. A load capacitor, C_{LOAD}, should be tied between VOUTS and GND. Its value should be greater than that of C_{PUMP}, the reservoir capacitor tied from V_{PUMP} to V_{OUTS} (see Figure 4). Given values of C_{LOAD}, Load, R_{SENSE}, VCC and the resistors determining the voltage on I_{MAX}, the user can calculate the approximate startup time of the node V_{OUT}. This time must be less than the time it takes for C_T to charge to 2.5V. Assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

I_{MAX} is the maximum current the UC3914 will allow through the transistor M1. During startup with an output capacitor, M1 can be modeled as a constant current source of value I_{MAX} where:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

Given this information, calculation of startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{LOAD} \bullet VCC}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = -R_{LOAD} \bullet C_{LOAD} \bullet \ell n \bullet \left(1 - \frac{VCC}{I_{MAX} \bullet R_{LOAD}}\right)$$

The only remaining external component which may affect the minimum timing capacitor is the optional power limiting resistor, R_{PL}. If the addition of R_{PL} is desirable, its value can be determined from the "Fault Timing" section above. The minimum timing capacitor values are now given by

Current Source Load:

$$CT\,\min = 2 \bullet T_{START} \bullet \left(\frac{10^{-4} \bullet R_{PL} + \frac{VCC}{2}}{2 \bullet R_{PL}}\right)$$

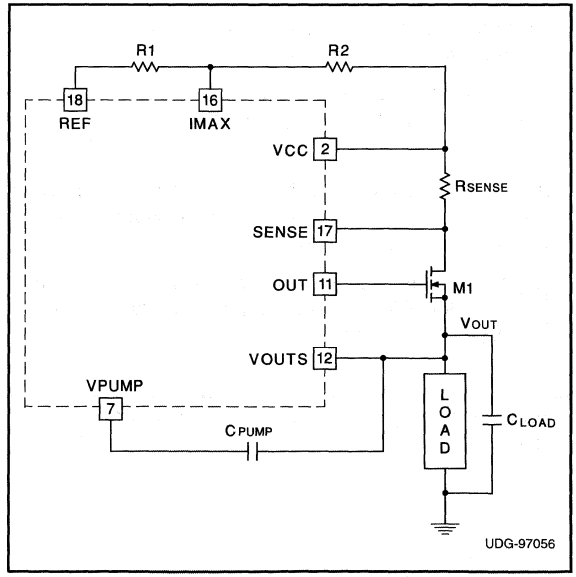


Figure 4. Estimating minimum timing capacitor.

APPLICATION INFORMATION (cont.)

Resistive Load:

$$CT\ \text{min} = \frac{\left(10^{-4} \bullet R_{PL} + V_{CC} - (I_{MAX} \bullet R_{LOAD})\right) \bullet T_{START}}{2 \bullet R_{PL}} + \frac{I_{MAX} \bullet (R_{LOAD})^2 \bullet C_{LOAD}}{2 \bullet R_{PL}} \bullet \left[1 - e^{\frac{-T_{START}}{R_{LOAD} \bullet C_{LOAD}}}\right]$$

Output Current Softstart

The external MOSFET output current can be increased at a user-defined rate to ensure that the output voltage comes up in a controlled fashion by adding capacitor Css, as shown in Figure 5. The chip does place one constraint on the soft start time and that is that the charge pump time constant has to be much less than the soft-start time constant to ensure proper soft start operation. The time constant determining the startup time of the charge pump is given by:

$$\tau_{CP} = R_{OUT} \bullet C_{PUMP}$$

R_{OUT} is the output impedance of the charge pump given by:

$$R_{OUT} = \frac{1}{f_{PUMP} \bullet CP}$$

where f_{PUMP} is the charge pump frequency (125kHz) and CP = CP1 = CP2 are the charge pump flying capacitors. For typical values of CP1, CP2 and C_{PUMP} (0.01µF) and a switching frequency of 125kHz, the output impedance is 800Ω and the charge pump time constant is 8µs. The charge pump should be close to being fully charged in 3 time constants or 24µs. By placing a capacitor from VCC to IMAX, the voltage at IMAX, which sets the maximum output current of the FET, will exponentially decay from VCC to the desired value set by R1 and R2. The output current of the MOSFET will be controlled via soft start as long as the soft start time constant (τ_{SS}) is much greater than the charge pump time constant τ_{CP}, given by

$$\tau_{SS} = (R1 \,||\, R2) \bullet C_{SS}$$

Minimizing Total Dropout Under Low Voltage Operation

In a typical application, the UC3914 will be used to control the output current of an external NMOS during hot swapping situations. Once the load has been fully charged, the desired output voltage on the load, V_{OUT}, will be required to be as close to VCC as possible to minimize total dropout. For a resistive load, R_{LOAD}, the output voltage is given by:

$$V_{OUT} = \frac{R_{LOAD}}{R_{LOAD} + R_{SENSE} + Rds_{ON}} \bullet VCC$$

R_{SENSE} was picked to set the fault current, I_{FAULT}. Rds_{ON}, the on-resistance of the NMOS, should be made as small as possible to ensure V_{OUT} is as close to VCC as possible. For a given NMOS, the manufacturer will specify the Rds_{ON} for a certain V_{GS} (maybe 7V to 10V). The source potential of the NMOS is V_{OUT}. In order to ensure sufficient VGS, this requires the gate of the NMOS, which is the output of the linear amplifier, to be many volts higher than VCC. The UC3914 provides the capability to generate this voltage through the addition of 3 capacitors, CP1, CP2 and C_{PUMP} as shown in Figure 6. These capacitors should be used in conjunction with the complementary output drivers and internal diodes included on-chip to create a charge pump or voltage

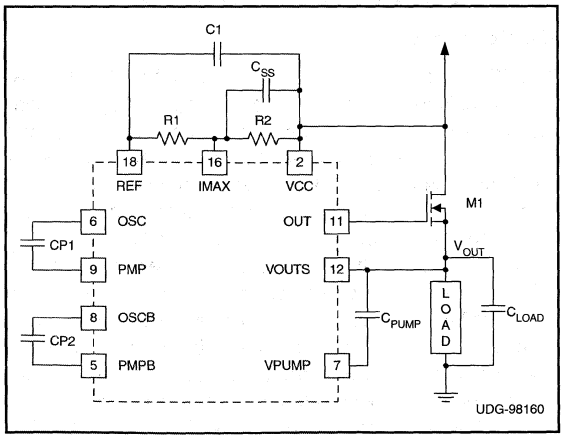


Figure 5. MOSFET soft start diagram.

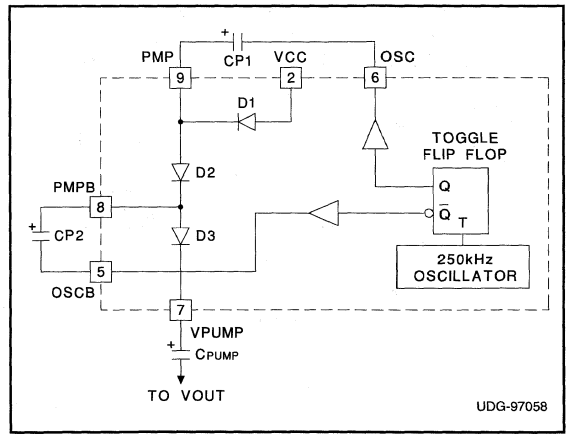


Figure 6. Charge pump block diagram.

APPLICATION INFORMATION (cont.)

tripler. The circuit boosts VCC by utilizing capacitors CP1, CP2 and C_{PUMP} in such a way that the voltage at V_{PUMP} approximately equals $(3 \bullet V_{CC}) - (5 \bullet V_{DIODE})$, almost tripling the input supply voltage to the chip.

On each complete cycle, CP1 is charged to approximately $V_{CC} - V_{DIODE}$ (unless V_{CC} is greater than 15V causing internal clamping to limit this charging voltage to about 13V) when the output Q of the toggle flip flop is low. When $\overline{Q}$ is transitioned low (and Q correspondingly is brought high), the negative side of CP2 is pulled to ground, and CP1 charges CP2 up to about $(2 \bullet V_{CC} - 3 \bullet V_{DIODE})$. When $\overline{Q}$ is toggled high, the negative side of CP2 is brought to $(V_{CC} - V_{DIODE})$. Since the voltage across a capacitor cannot change instantaneously with time, the positive side of the capacitor swings up to $(3 \bullet V_{CC} - 4 \bullet V_{DIODE})$. This charges C_{PUMP} up to $(3 \bullet V_{CC} - 5 \bullet V_{DIODE})$.

The maximum output voltage of the linear amplifier is actually less than this because of the ability of the amplifier to swing to within approximately 1V of V_{PUMP}. Due to inefficiencies of the charge pump, the UC3914 may not have sufficient gate drive to fully enhance a standard power MOSFET when operating at input voltages below 7V. Logic Level MOSFETs could be used depending on the application but are limited by their lower current capability. For applications requiring operation below 7V there are two ways to increase the charge pump output voltage. Figure 7 shows the typical tripler of figure 6 enhanced with three external schottky diodes. Placing the schottky diodes in parallel with the internal charge pump diodes decreases the voltage drop across each diode thereby increasing the overall efficiency and output voltage of the charge pump.

Figure 8 shows a way to use the existing drivers with external diodes (or Schottky diodes for even higher pump voltages but with additional cost) and capacitors to make a voltage quadrupler. The additional charge pump stage will provide a sufficient pump voltage $(V_{PUMP} = 4 \bullet V_{CC} - 7 \bullet V_{DIODE})$ to generate the maximum V_{GS}. Operation is similar to the case described above. This additional circuitry is not necessary for higher input voltages because the UC3914 has internal clamping which only allows V_{PUMP} to be 10V greater than V_{OUTS}.

Input Voltage (VCC)	Internal Diodes (V_{GS})	External Schottky Diodes (V_{GS})	Quadrupler (V_{GS})
4.5	4.57	6.8	8.7
5	5.8	7.9	8.8
5.5	6.6	8.6	8.9
6	7.6	8.8	9
6.5	8.7	8.8	9
7	8.8	9	9
9	9.2	9.4	9.1
10	9.3	9.4	9.3

Table 1. UC3914 charge pump characteristics.

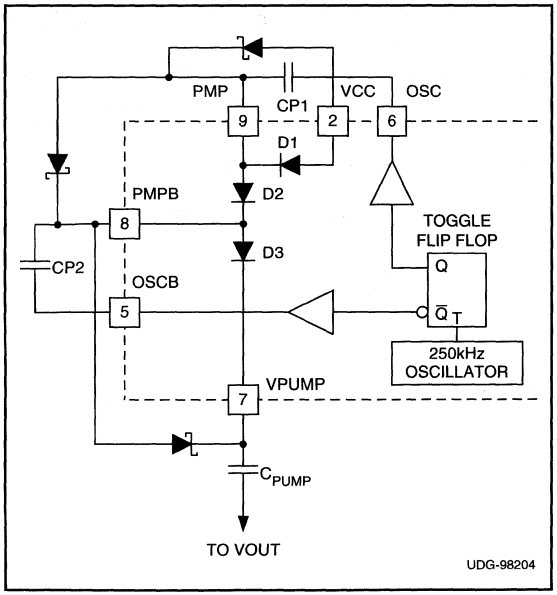


Figure 7. Charge pump block diagram.

Table 1 characterizes the UC3914 charge pump in its standard configuration, with external schottky diodes, and configured as a voltage quadrupler. Please note: The voltage quadrupler is unnecessary for input voltages above 7.0V due the internal clamping action.

ICC Specification

The ICC operating measurement is actually a mathematical calculation. The charge pump voltage is constantly being monitored with respect to both V_{CC} and V_{OUTS} to determine whether the pump requires servicing. If there is insufficient voltage on this pin, the charge pump drivers are alternately switched to raise the voltage of the pump (see Fig. 9). Once the voltage on the pump is high enough, the drivers and other charge pump related circuitry are shutdown to conserve current. The pump voltage will decay due to internal loading until it reaches a low enough level to turn the drivers back on. The chip requires significantly different amounts of current during these two modes of operation and the following mathematical calculation is used to figure out the average current:

APPLICATION INFORMATION (cont.)

$$ICC = \frac{ICC_{DRIVERS(on)} \bullet T_{ON} + ICC_{DRIVERS(off)} \bullet T_{OFF}}{T_{ON} + T_{OFF}}$$

Since the charge pump does not always require servicing, the user may think that the charge pump frequency is much less than the datasheet specification. This is not the case as the free-running frequency is guaranteed to be within the datasheet limits. The charge pump servicing frequency can make it appear as though the drivers are operating at a much lower frequency.

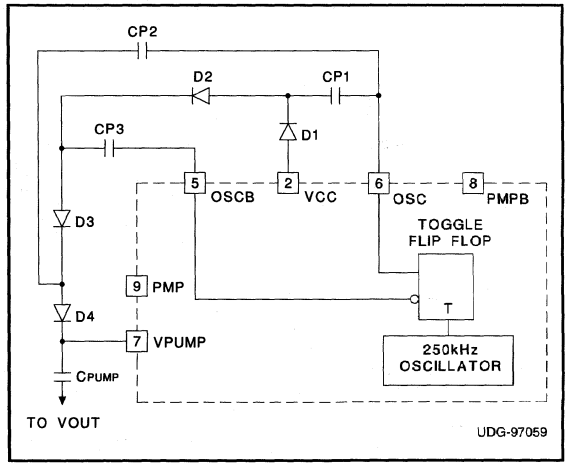


Figure 8. Low voltage operation to produce higher pump voltage

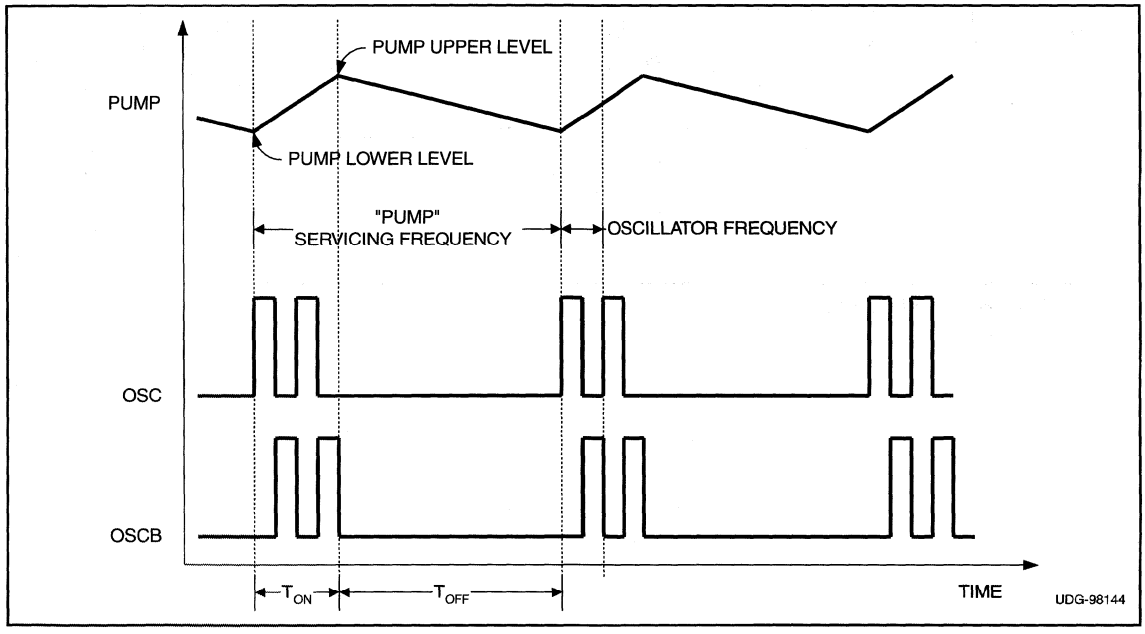


Figure 9. Charge pump waveforms.

SAFETY RECOMMENDATIONS

Although the UC3914 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UC3914 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UC3914 will prevent the fuse from blowing in virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

APPLICATION INFORMATION (cont.)

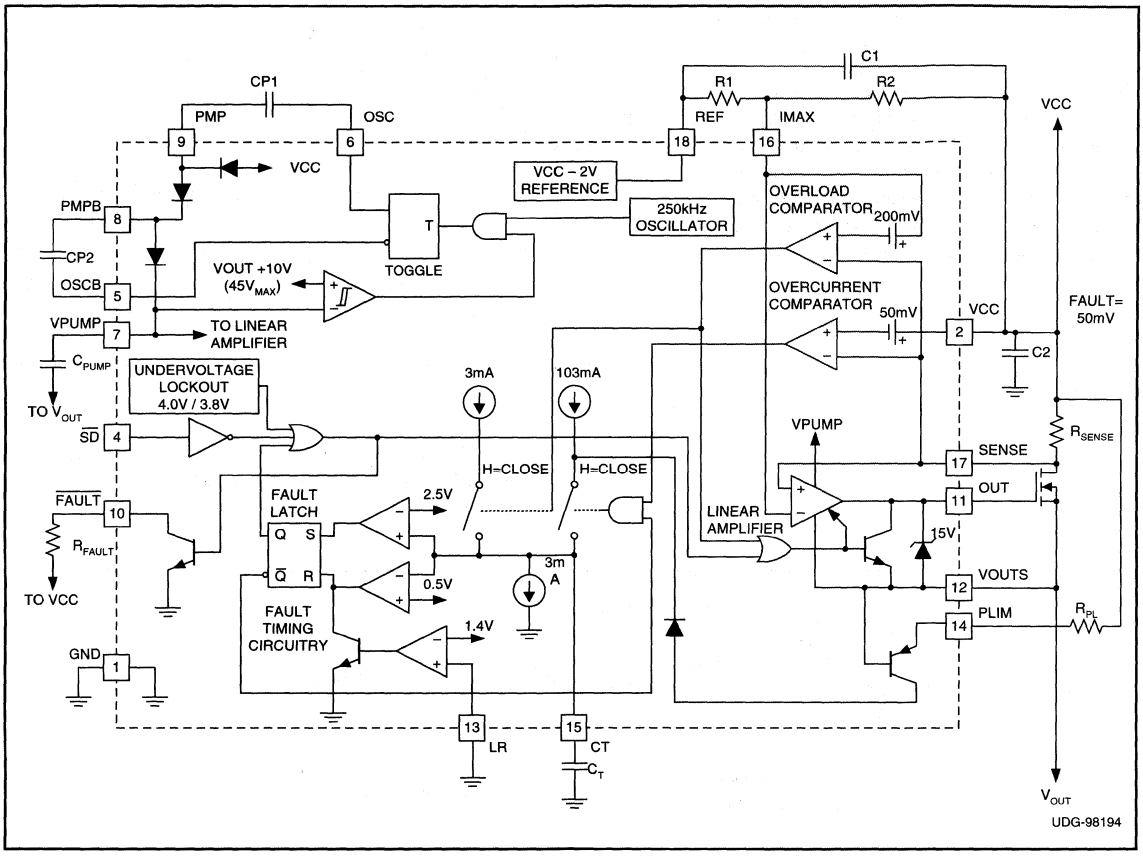


Figure 10. Typical application.

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15V Programmable Hot Swap Power Manager

PRELIMINARY

FEATURES

- Integrated 0.15 Ohm Power MOSFET
- 7V to 15V Operation
- Digital Programmable Current Limit from 0A to 3A
- 100µA I_{CC} when Disabled
- Programmable ON Time
- Programmable Start Delay
- Fixed 2% Duty Cycle
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC and TSSOP, Low Thermal Resistance Packaging

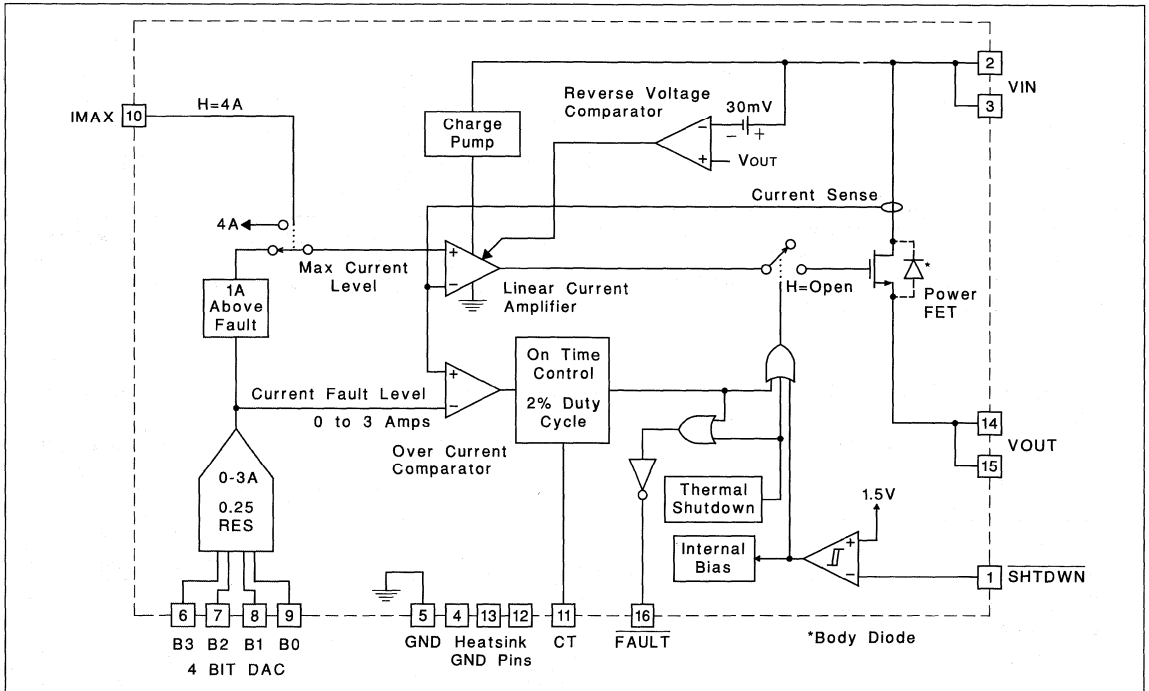
DESCRIPTION

The UCC3915 Programmable Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only external component required to operate the device, other than power supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the Internal fixed 2% duty cycle ratio limits average output power.

The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the trip level or to a full 4A of output current for fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched ON with a nominal ON resistance of 0.15Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched ON, but the fault timer starts, charging CT. Once CT charges to a preset threshold, the switch is turned OFF, and remains OFF for 50 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-16 and SOIC-16 packages.

UDG-94136-3

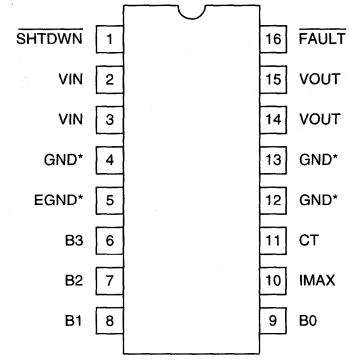
ABSOLUTE MAXIMUM RATINGS

VIN . . . . . +15.5 Volts
VOUT – VIN 0.3V
FAULT Sink Current 50mA
FAULT Voltage . . . . . –0.3 to 8V
Output Current . . . . . Self Limiting
TTL Input Voltage . . . . . –0.3 to V_{IN}
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

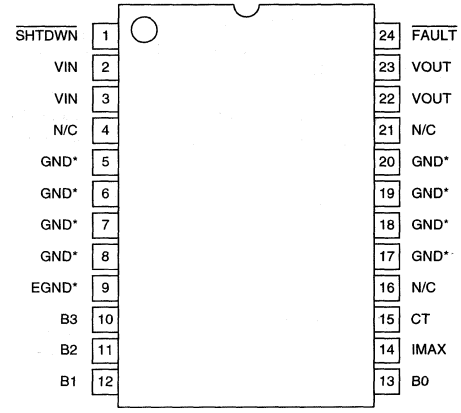
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
N, DP Package



**Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.*

PWP-24 (Top View)
TSSOP Package



**Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.*

DESCRIPTION (cont.)

(continued)

The UCC3915 can be put into sleep mode, drawing only 100µA of supply current. Other features include an open drain Fault Output Indicator, Thermal Shutdown, Under-

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –40°C to +85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12V, IMAX = 0.4V, SHTDWN = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		7.0		15.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	SHTDWN = 0.2V, No load		100	150	µA
Output Leakage	SHTDWN = 0.2V			20	µA
Output Section					
Voltage Drop	I_{OUT} = 1A (10V to 12V)		0.15	0.3	V
	I_{OUT} = 2A (10V to 12V)		0.3	0.6	V
	I_{OUT} = 3A (10V to 12V)		0.45	0.9	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –40°C to +85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12V, IMAX = 0.4V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (cont.)					
Voltage Drop (cont).	I_{OUT} = 1A, VIN = 7V and 15V		0.2	0.4	V
	I_{OUT} = 2A, VIN = 7V and 15V		0.4	0.8	V
	I_{OUT} = 3A, VIN = 7V, 12V Max.		0.6	1.2	V
Initial Startup Time	Note 2		100		µs
Short Circuit Response	Note 2		100		ns
Thermal Shutdown	Note 2		165		°C
Thermal Hysteresis	Note 2		10		°C
DAC Section					
Trip Current	Code = 0000-0011 (Device Off)				
	Code = 0100	0.07	0.25	0.45	A
	Code = 0101	0.32	0.50	0.70	A
	Code = 0110	0.50	0.75	0.98	A
	Code = 0111	0.75	1.00	1.3	A
	Code = 1000	1.0	1.25	1.6	A
	Code = 1001	1.25	1.50	1.85	A
	Code = 1010	1.5	1.75	2.15	A
	Code = 1011	1.70	2.00	2.4	A
	Code = 1100	1.90	2.25	2.7	A
	Code = 1101	2.1	2.50	2.95	A
	Code = 1110	2.30	2.75	3.25	A
	Code = 1111	2.50	3.0	3.50	A
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 0V	0.35	1.0	1.65	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 2.4V	3.0	4.0	5.2	A
Fault Output Section					
CT Charge Current	V_{CT} = 1.0V	–83	–62	–47	µA
CT Discharge Current	V_{CT} = 1.0V	0.8	1.2	1.8	µA
Output Duty Cycle	V_{OUT} = 0V	1.0	1.9	3.3	%
CT Fault Threshold		1.2	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			150		mV
Input Current			100	500	nA
Open Drain Output Section					
High Level Output Current	$\overline{FAULT}$ = 5V			250	µA
Low Level Output Voltage	I_{OUT} = 5mA		0.2	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High		2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	V_{IH} = 2.4V		3	10	µA
TTL Input Low Current	V_{IL} = 0.4V			1	µA

Note 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

SB0 - B3: These pins provide digital input to the DAC, which sets the fault current threshold. They can be used to provide a digital soft-start and adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time required to charge the external capacitance in one cycle. The maximum fault time is defined as $T_{FAULT} = 16.1 \bullet 10^3 \bullet CT$. Once the fault time is reached the output will shutdown for a time given by $T_{SD} = 833 \bullet 10^3 \bullet CT$, this equates to a 1.9% duty cycle.

$\overline{\text{FAULT}}$: Open drain output, which pulls low upon any fault or interrupt condition, Fault, or Thermal Shutdown.

IMAX: When this pin is set to a logic low, the maximum sourcing current will always be 1A above the programmed fault level. When set to a logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 100µA of I_{CC}.The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: Input voltage to the UCC3915. The recommended voltage range is 7 to 15 volts. Both VIN pins should be connected together and connected to power source.

VOUT: Output voltage from the UCC3915. Both VOUT pins should be connected together and connected to the load. When switched the output voltage will be approximately $V_{IN} - (0.15\Omega \bullet I_{OUT})$. VOUT must not exceed VIN by greater than 0.3V.

APPLICATIONS INFORMATION

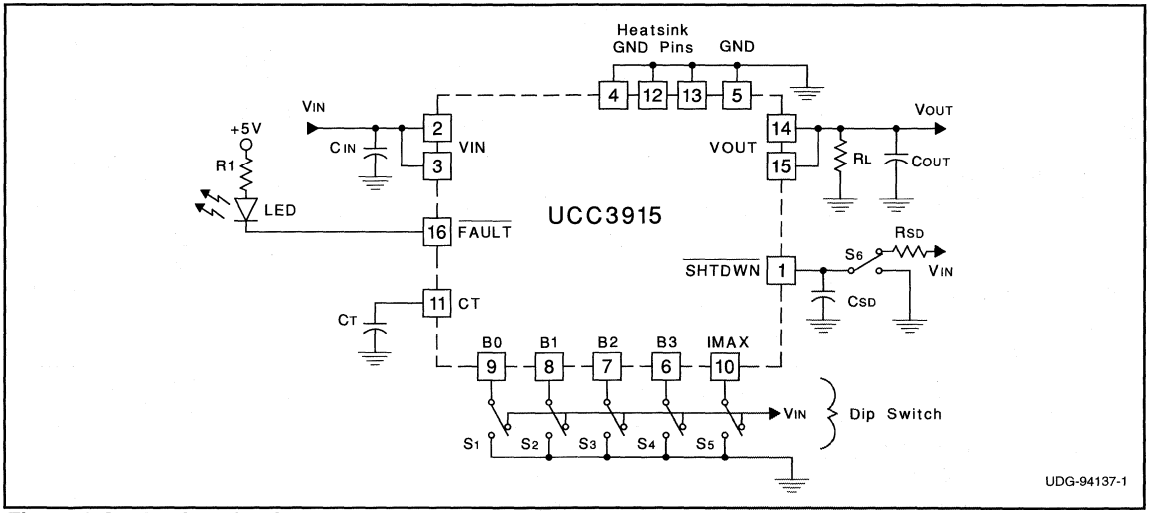
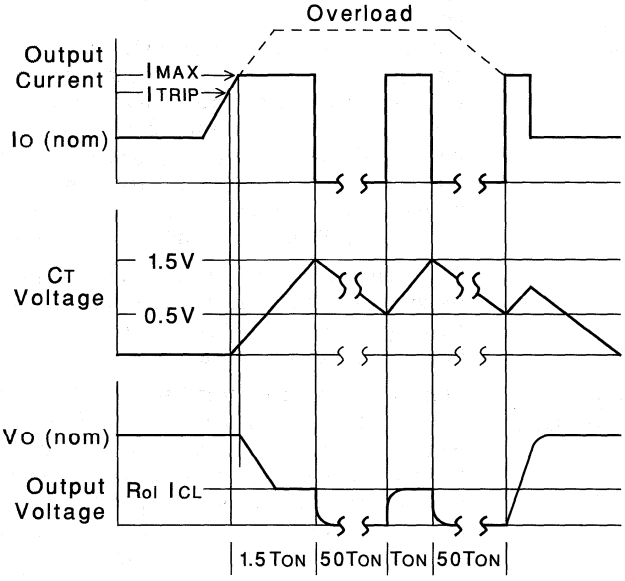


Figure 1. Evaluation circuit

APPLICATION INFORMATION (cont.)



Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current, current-limited application, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \quad I_{MAX} - I_{LOAD} \bullet \frac{16.1 \bullet 10^3 \bullet C_T}{V_{OUT}}$$

Where V_{OUT} is the output voltage.

For a resistive load of value R_l, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \quad \frac{16.1 \bullet 10^3 \bullet C_T}{R_L \bullet \ell n \frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}}}$$

Figure 2. Load current, timing capacitor voltage, and output voltage of the UCC3915 under fault conditions.

SAFETY RECOMMENDATIONS

Although the UCC3915 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3915 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3915 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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UNITRODE

15V Programmable Hot Swap Power Manager

FEATURES

- Integrated 0.15Ω Power MOSFET
- 7V to 15V Operation
- Digital Programmable Current Limit from 0A to 3A
- Programmable ON Time
- Programmable Start Delay
- Fixed 2% Duty Cycle
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC and TSSOP, Low Thermal Resistance Packaging

DESCRIPTION

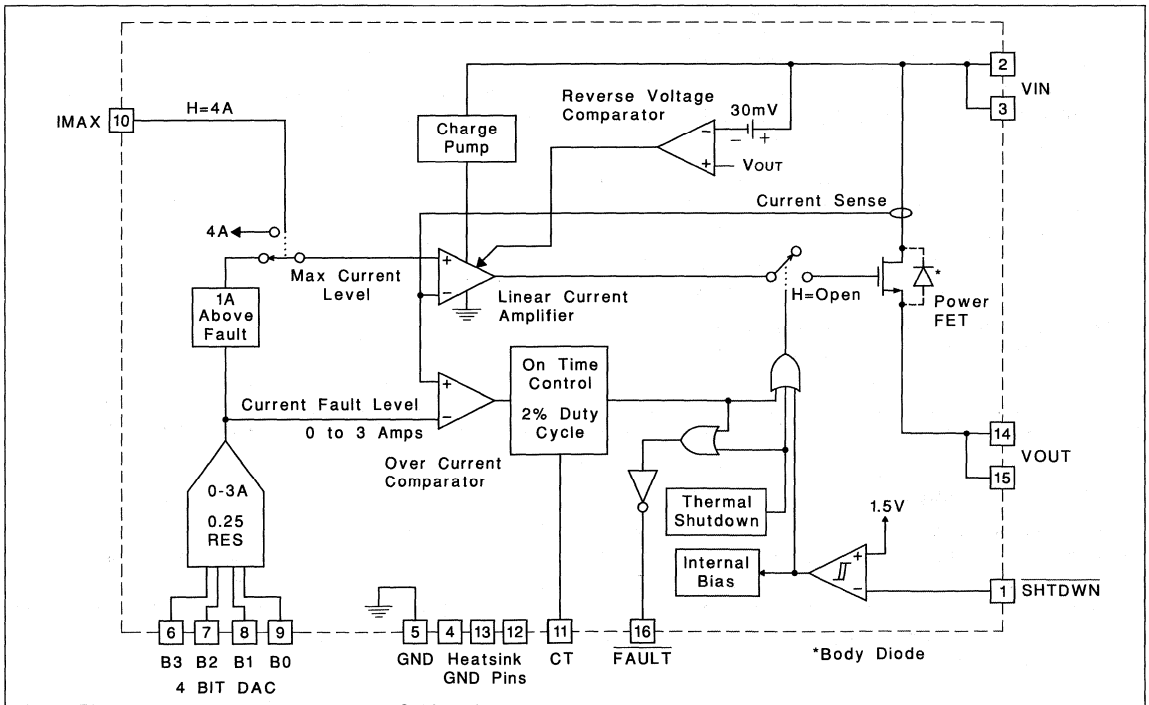
The UCC39151 Programmable Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only external component required to operate the device, other than power supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the Internal fixed 2% duty cycle ratio limits average output power.

The internal 4 bit DAC allows programming of the fault level current from 0A to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the trip level or to a full 4A of output current for fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched ON with a nominal ON resistance of 0.15Ω. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched ON, but the fault timer starts, charging CT. Once CT charges to a preset threshold, the switch is turned OFF, and remains OFF for 50 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

(continued)

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-16 and SOIC-16 packages.

UDG-94136-3

ABSOLUTE MAXIMUM RATINGS

VIN . . . . . +15.5 Volts
VOUT – VIN 0.3V
FAULT Sink Current 50mA
FAULT Voltage . . . . . –0.3 to 8V
Output Current . . . . . Self Limiting
TTL Input Voltage . . . . . –0.3 to V_{IN}
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

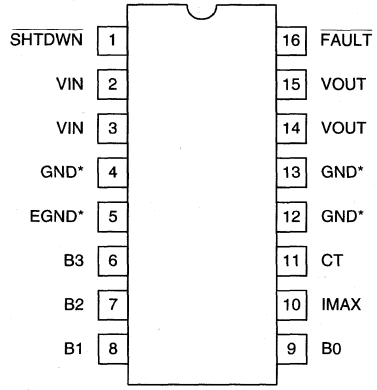
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

DESCRIPTION (cont.)

The UCC39151 can be put into sleep mode, drawing only 20mA of supply current. Other features include an open drain Fault Output Indicator, Thermal Shutdown, Undervoltage Lockout, 7V to 15V operation, and low thermal resistance SOIC and TSSOP Power Packages.

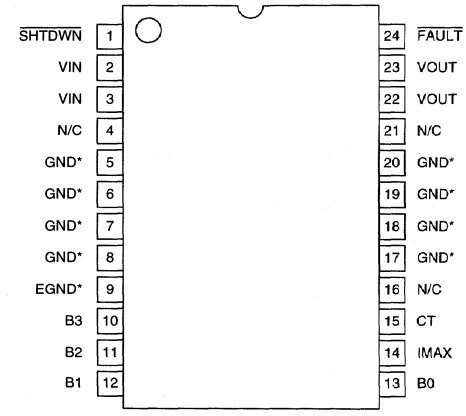
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
N, DP Package



**Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.*

PWP-24 (Top View)
TSSOP Package



**Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.*

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC39151, VIN = 12V, IMAX = 0.4V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		7.0		15.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	$\overline{SHTDWN}$ = 0.2V, No load		100	150	µA
Output Leakage	$\overline{SHTDWN}$ = 0.2V			20	mA
Output Section					
Voltage Drop	I_{OUT} = 1A (10V to 12V)		0.15	0.3	V
	I_{OUT} = 2A (10V to 12V)		0.3	0.6	V
	I_{OUT} = 3A (10V to 12V)		0.45	0.9	V
	I_{OUT} = 1A, VIN = 7V and 15V		0.2	0.4	V
	I_{OUT} = 2A, VIN = 7V and 15V		0.4	0.8	V
	I_{OUT} = 3A, VIN = 7V, 12V Max.		0.6	1.2	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC39151, VIN = 12V, IMAX = 0.4V, SHTDWN = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (continued)					
Initial Startup Time	(Note 2)		100		µs
Short Circuit Response	(Note 2)		100		ns
DAC Section					
Trip Current	Code = 0000-0011 (Device Off)				
	Code = 0100	0.07	0.25	0.45	A
	Code = 0101	0.32	0.50	0.7	A
	Code = 0110	0.50	0.75	0.98	A
	Code = 0111	0.75	1.00	1.3	A
	Code = 1000	1.0	1.25	1.6	A
	Code = 1001	1.25	1.50	1.85	A
	Code = 1010	1.5	1.75	2.15	A
	Code = 1011	1.70	2.00	2.4	A
	Code = 1100	1.90	2.25	2.7	A
	Code = 1101	2.1	2.50	2.95	A
	Code = 1110	2.30	2.75	3.25	A
	Code = 1111	2.50	3.0	3.5	A
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 0V	0.35	1.0	1.65	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 2.4V	3.0	4.0	5.2	A
Fault Output Section					
CT Charge Current	V_{CT} = 1.0V	–83	–62	–47	µA
CT Discharge Current	V_{CT} = 1.0V	0.8	1.2	1.8	µA
Output Duty Cycle	V_{OUT} = 0V	1.0	1.9	3.3	%
CT Fault Threshold		1.2	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			150		mV
Input Current			100	500	nA
Open Drain Output Section					
High Level Output Current	$\overline{FAULT}$ = 5V			250	µA
Low Level Output Voltage	I_{OUT} = 5mA		0.2	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High		2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	V_{IH} = 2.4V		3	10	µA
TTL Input Low Current	V_{IL} = 0.4V			1	µA

Note 1: All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

B0, B1, B2, B3: These pins provide digital input to the DAC, which sets the fault current threshold. They can be used to provide a digital soft-start and adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time required to charge the external capacitance in one cycle. The maximum fault time is defined as:

$$T_{FAULT} = 16.1 \bullet 10^3 \bullet C_T.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 833 \bullet 10^3 \bullet C_T,$$

this equates to a 1.9% duty cycle.

$\overline{\text{FAULT}}$: Open drain output, which pulls low upon any fault or interrupt condition, Fault, or Thermal Shutdown.

IMAX: When this pin is set to a logic low, the maximum sourcing current will always be 1A above the programmed fault level. When set to a logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 100µA of I_{CC} (with V_{OUT} unloaded). The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: Input voltage to the UCC39151. The recommended voltage range is 7V to 15V. Both VIN pins should be connected together and connected to power source.

VOUT: Output voltage from the UCC39151. Both VOUT pins should be connected together and connected to the load. When switched:

$$V_{OUT} \approx V_{IN} - (0.15\Omega \bullet I_{OUT})$$

VOUT must not exceed VIN by more than 0.3V.

APPLICATIONS INFORMATION

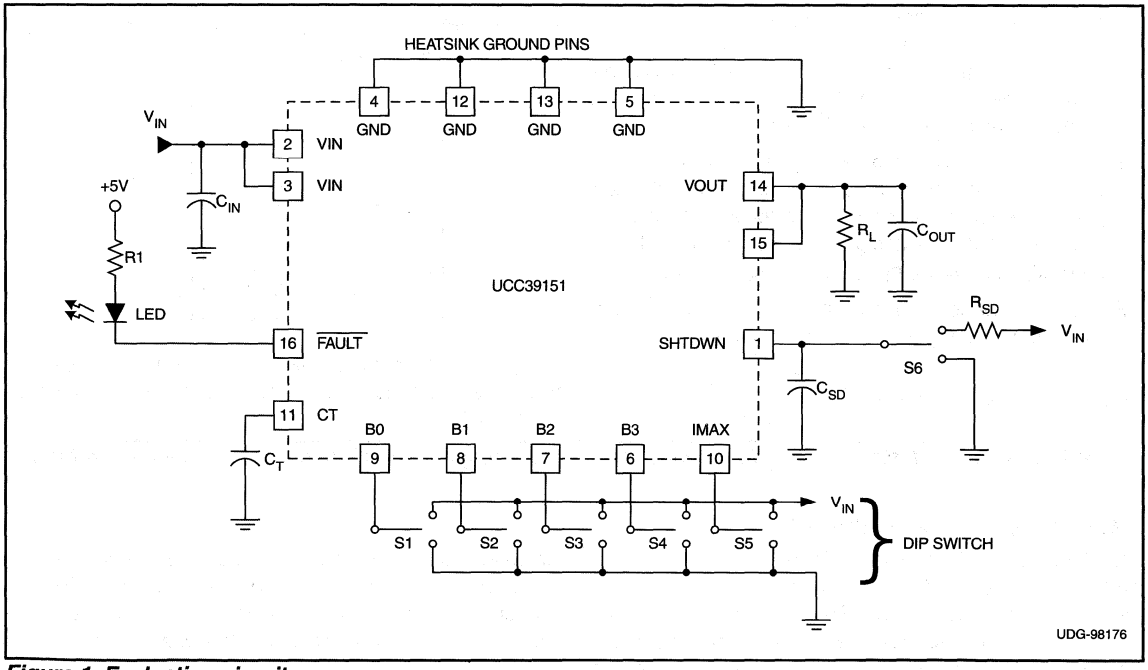
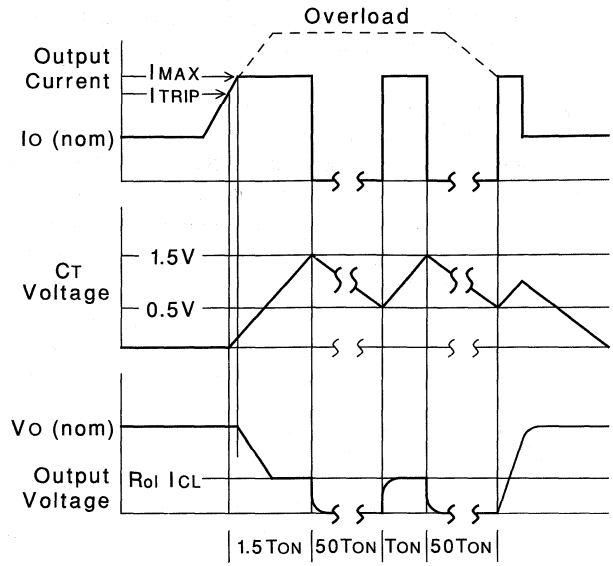


Figure 1. Evaluation circuit.

APPLICATION INFORMATION (cont.)



Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current, current-limited application, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{16.1 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value R_l, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{16.1 \bullet 10^3 \bullet C_T}{R_L \bullet \ell n \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$

Long C_T times must consider the maximum temperature. Thermal shutdown protection may be the limiting Fault time.

Figure 2. Load current, timing capacitor voltage, and output voltage of the UCC39151 under fault conditions.

SAFETY RECOMMENDATIONS

Although the UCC39151 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC39151 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC39151 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
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UNITRODE

SCSI Termpower Manager

FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2Ω Power FET
- SCSI, SCSI-2, SCSI-3 Compliant
- 1µA ICC When Disabled
- Programmable On Time
- Accurate 1.65A Trip Current/ 2.1A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

DESCRIPTION

The UCC3916 SCSI termpower manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other than supply bypassing, is a timing capacitor which sets the fault time.

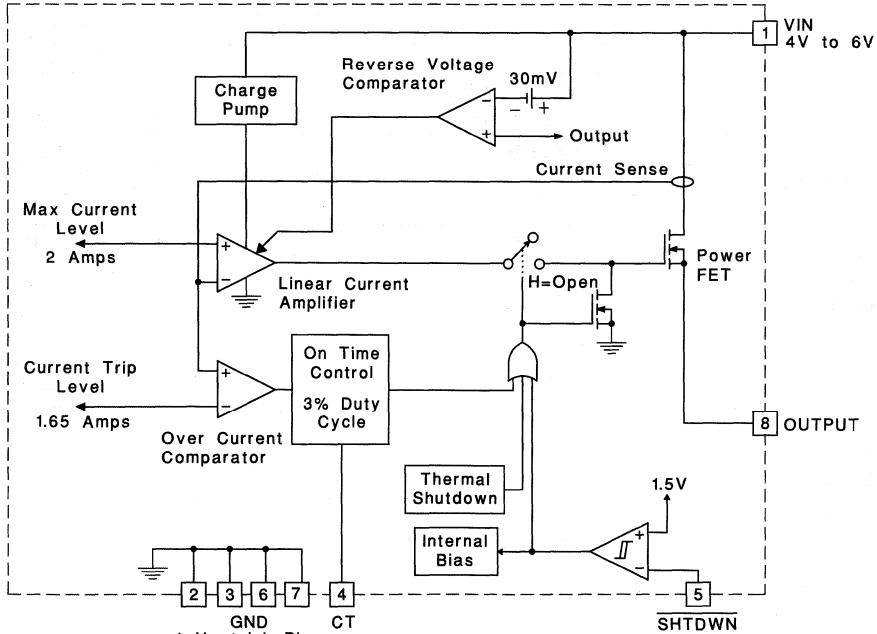
The current trip level is internally set at 1.65A, and the maximum current level is also internally programmed for 2A. While the output current is below the trip level of 1.65A, the internal power MOSFET is switched on at a nominal 220mΩ. When the output current exceeds the trip level but remains less than the maximum current level, the MOSFET remains switched on, but the fault timer starts charging CT. Once the fault time is reached, the circuit will shut off for a time which equates to a 3% duty cycle. Finally, when the output current reaches the maximum current level, the MOSFET transitions from a switch to a constant current source.

The UCC3916 is designed for uni-directional current flow, emulating a diode in series with the power MOSFET.

The UCC3916 can be put in a sleep mode, drawing only 1µA of supply current.

Other features include thermal shutdown and low thermal resistance Small Outline Power package.

BLOCK DIAGRAM



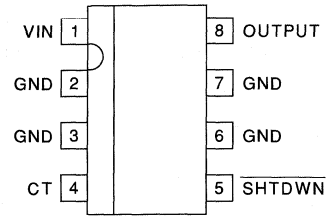
ABSOLUTE MAXIMUM RATINGS

VIN ..... +6V
Output Current
DC ..... Self Limiting
Pulse (Less than 100ns) 20A
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = 0°C to +70°C; VIN = 5V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
ICC			1.00	2.00	mA
ICC - Sleep Mode	$\overline{SHTDWN}$ = 0.2V		0.50	5	µA
Output Section					
Voltage Drop	I_{OUT} = 1A		0.22	0.33	V
	I_{OUT} = 1.5A		0.33	0.50	V
	I_{OUT} = 1.8A		0.40	0.60	V
Trip Current		–1.8	–1.65	–1.5	A
Max Current		–2.4	–2	–1.8	A
Reverse Leakage	VIN = 4.5V, V_{OUT} = 5V		6	20	µA
	VIN = 0V, V_{OUT} = 5V		0.50	9	µA
Soft Start Time	Initial Startup		50		µs
Short Circuit Response			100		ns
Fault Section					
CT Charge Current	V_{CT} = 1.0V	–45	–36.0	–27	µA
CT Discharge Current	V_{CT} = 1.0V	0.90	1.0	1.50	µA
Output Duty Cycle	V_{OUT} = 0V	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		°C
Thermal Hysteresis			10		°C
Shutdown Section					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	$\overline{SHTDWN}$ = 1.0V		100	500	nA

Note 1: All voltages are with respect to ground.

PIN DESCRIPTIONS

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{FAULT} = 28 \bullet 10^3 \bullet CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \bullet 10^6 \bullet CT$$

this results in a 3% duty cycle. 0.1µF is recommended for SCSI applications to achieve the normal maximum capacitance on the Termpwr line.

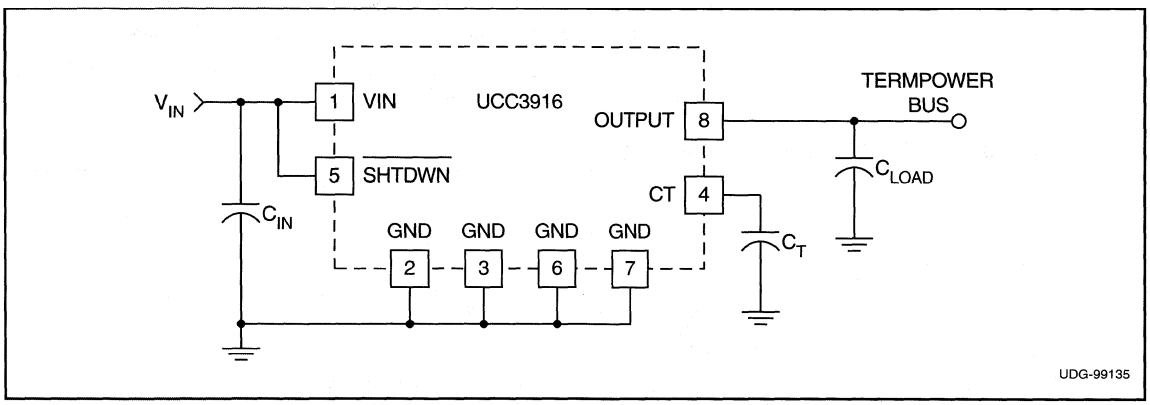
$\overline{SHTDWN}$: The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

VIN: Input voltage to the circuit breaker, ranging from 4V to 6V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = VIN - (220m\Omega) \bullet I_{OUT}.$$

TYPICAL APPLICATION



SAFETY RECOMMENDATIONS

Although the UCC3916 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3916 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3916 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

Low Current Hot Swap Power Manager

FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2Ω Power FET
- 1μA ICC When Disabled
- Programmable On Time
- Accurate 0.8A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

DESCRIPTION

The UCC39161 low current hot swap power manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other then supply bypassing, is a timing capacitor which sets the fault time.

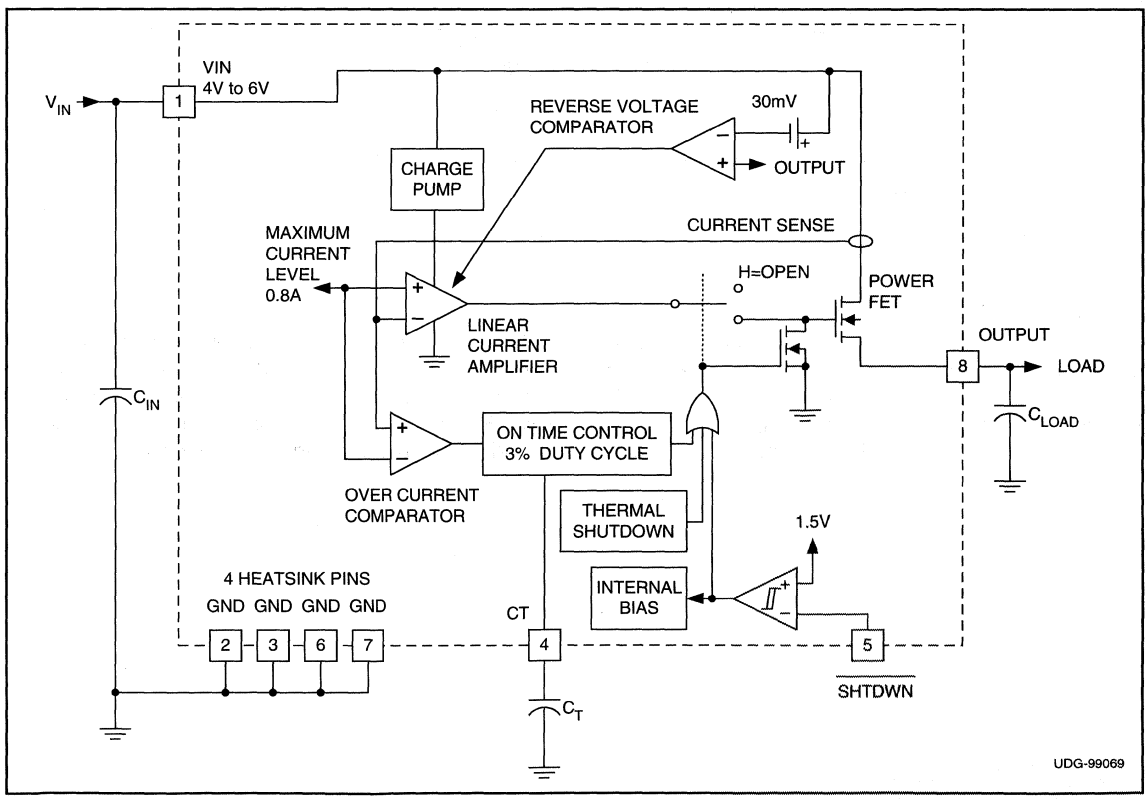
The maximum current level is internally programmed for 0.8A. While the output current is below 0.8A, the internal power MOSTFET is switched on at a nominal 220mΩ. When the output current exceeds 0.8A, the MOSFET transitions from a switch to a constant current source and the fault timer starts charging CT. Once the fault time is reached, the current will shut off for a time, which equates to a 3% duty cycle.

The UCC39161 also provides unidirectional current flow, emulating a diode in series with the power MOSFET.

The UCC39161 can be put into sleep mode by grounding the $\overline{\text{SHTDWN}}$ pin. In sleep mode, the UCC39161 draws under 5μA of supply current.

Other features include thermal shutdown and a low thermal resistance Small Outline Power package.

BLOCK DIAGRAM AND TYPICAL APPLICATION



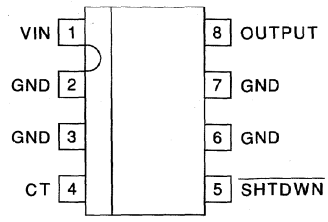
ABSOLUTE MAXIMUM RATINGS

VIN ..... +6V
Output Current
DC ..... Self Limiting
Pulse (Less than 100ns) 20A
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = 0°C to +70°C; VIN = 5V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
ICC			1.00	2.00	mA
ICC - Sleep Mode	$\overline{SHTDWN}$ = 0.2V		0.50	5	µA
Output Section					
Voltage Drop	I_{OUT} = 0.5A		0.10	0.16	V
Max Current		–1.0	–0.8	–0.6	A
Reverse Leakage	VIN = 4.5V, V_{OUT} = 5V		6	20	µA
	VIN = 0V, V_{OUT} = 5V		0.50	9	µA
Soft Start Time	Initial Startup		50		µs
Short Circuit Response			100		ns
Fault Section					
CT Charge Current	V_{CT} = 1.0V	–45	–36.0	–27	µA
CT Discharge Current	V_{CT} = 1.0V	0.90	1.0	1.50	µA
Output Duty Cycle	V_{OUT} = 0V	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		°C
Thermal Hysteresis			10		°C
Shutdown Section					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	$\overline{SHTDWN}$ = 1.0V		100	500	nA

Note 1: All voltages are with respect to ground.

PIN DESCRIPTIONS

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{FAULT} = 28 \bullet 10^3 \bullet CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \bullet 10^6 \bullet CT$$

this results in a 3% duty cycle.

$\overline{\text{SHTDWN}}$: The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

VIN: Input voltage to the circuit breaker, ranging from 4V to 6V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = VIN - 220m\Omega \bullet I_{OUT}.$$

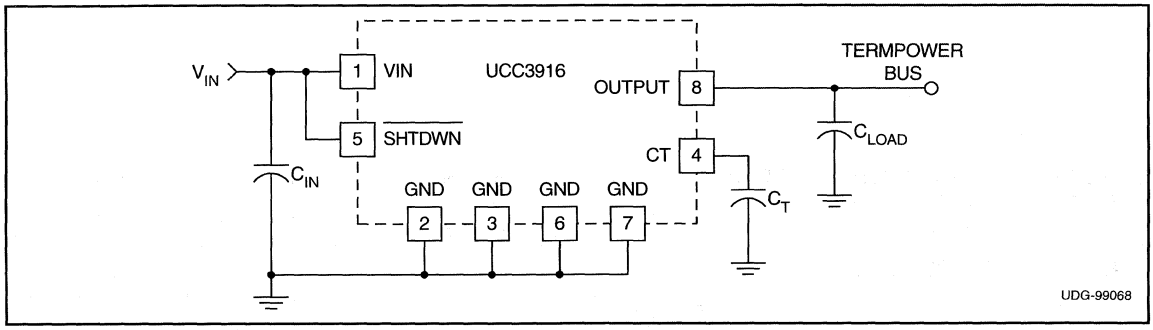


Figure 1. Typical application.

SAFETY RECOMMENDATIONS

Although the UCC39161 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC39161 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC39161 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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UNITRODE

application INFO available

UCC1917
UCC2917
UCC3917
PRELIMINARY

Positive Floating Hot Swap Power Manager

FEATURES

- Manages Hot Swap of 15V and Above
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Programmable Fault Time
- Internal Charge Pump to Control External NMOS Device
- Fault Output and Catastrophic Fault Indication
- Fault Mode Programmable to Latch or Retry
- Shutdown Control
- Undervoltage Lockout

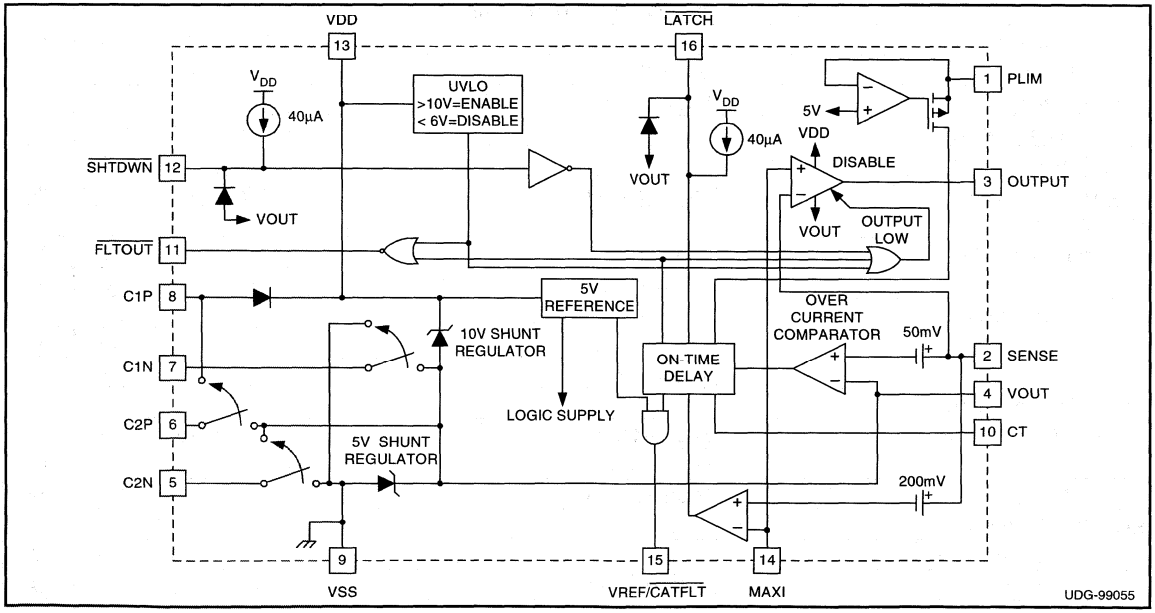
DESCRIPTION

The UCC3917 family of positive floating hot swap managers provides complete power management, hot swap, and fault handling capability. The voltage limitation of the application is only restricted by the external component voltage limitations. The IC provides its own supply voltage via a charge pump off of VOUT. The onboard 10V shunt regulator protects the IC from excess voltage. The IC also has catastrophic fault indication to alert the user that the ability to shut off the output NMOS has been bypassed. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average NMOS power limiting.

The fault level across the current sense amplifier is fixed at 50mV to minimize total drop out. Once 50mV is exceeded across the current sense resistor, the fault timer will start. The maximum allowable sourcing current is programmed with a voltage divider from the VREF/CATFLT pin to generate a fixed voltage on the MAXI pin. The current level at which the output appears as a current source is equal to V_{MAXI} divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on MAXI.

When the output current is below the fault level, the output device is switched on with full gate drive. When the output current exceeds the fault level, but is less than maximum allowable sourcing level programmed by MAXI, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and attempts either a retry sometime later or waits for the state on the LATCH pin to change if in latch mode. When the output current reaches the maximum sourcing current level, the output device appears as a current source.

BLOCK DIAGRAM

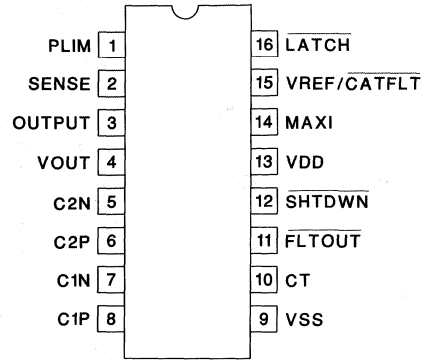


ABSOLUTE MAXIMUM RATINGS

IDD 20mA
SHTDWN Current . . . . . –500µA
LATCH Current . . . . . –500µA
VREF Current . . . . . –500µA
PLIM Current 10mA
MAXI Input Voltage . . . . . VDD + 0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3917, –40°C to 85° for the UCC2917 and –55°C to 125°C for the UCC1917, C_T = 4.7nF. $T_A = T_J$. All voltages are with respect to VOUT. Current is positive into and negative out of the specified terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD	From VOUT (Note 2)	3.0	5	11	mA
UVLO Turn On Threshold		8	9	10	V
UVLO Off Voltage		5.5	6.5	7.5	V
VSS Regulator Voltage		–6	–5	–4	V
Fault Timing Section					
Overcurrent Threshold	T_A = 25°C	47.5	50	53	mV
	Over Operating Temperature	46	50	54	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1V	–70	–50	–36	µA
CT Discharge Current	V_{CT} = 1V	0.9	1.5	2.1	µA
CT Fault Threshold		2.25	2.5	2.75	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition	1.7	2.7	3.7	%
Output Section					
Output High Voltage	I_{OUT} = 0	6	8	10	V
	I_{OUT} = –500µA	5	7	9	V
Output Low Voltage	I_{OUT} = 0		0	0.05	V
	I_{OUT} = 500µA		0.1	0.5	V
	I_{OUT} = 1mA		0.5	0.9	V
Linear Current Section					
Sense Control Votlage	MAXI = 100mV	85	100	115	mV
	MAXI = 400mV	370	400	430	mV
Input Bias	MAXI = 200mV		50	500	nA
SHUTDOWN Section					
Shutdown Threshold		2.0	2.4	2.8	V
Input Current	$\overline{SHTDWN}$ = 0V	24	40	60	µA
Shutdown Delay			100	500	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3917, –40°C to 85° for the UCC2917 and –55°C to 125°C for the UCC1917, C_T = 4.7nF. $T_A = T_J$. All voltages are with respect to VOUT. Current is positive into and negative out of the specified terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LATCH Section					
Latch Threshold		1.7	2	2.3	V
Input Current	LATCH = 0V	24	40	60	µA
Fault Out Section					
Fault Output High		6	8	10	V
Fault Output Low			0.01	0.05	V
Power Limiting Section					
VSENSE Regulator Voltage	IPLIMIT = 64µA	4.5	5	5.5	V
Duty Cycle Control	IPLIMIT = 64µA	0.6	1.2	1.7	%
	IPLIMIT = 1mA	0.045	0.1	0.2	%
VREF/CATFLT Section					
VREF Regulator Voltage		4.5	5	5.5	V
Fault Output Low			0.01	0.05	V
Output Sink Current	VCT = 5V	2	5	8	mA
Overload Comparator Threshold	Relative to MAXI	140	200	260	mV

Note 2: Set by user with Rss.

PIN DESCRIPTIONS

C1N: Negative side of the upper charge pump capacitor.

C1P: Positive side of the upper charge pump capacitor.

C2N: Negative side of the lower charge pump capacitor.

C2P: Positive side of lower charge pump capacitor.

CT: A capacitor is connected to this pin to set the fault time. The fault time must be more than the time to charge the external load capacitance (see Application Information).

FLTOUT: This pin provides fault output indication. Interface to this pin is usually performed through level shift transistors. Under a non-fault condition, FLTOUT will pull to a high state. When a fault is detected by the fault timer or the under voltage lockout, this pin will drive to a low state, indicating the output NMOS is in the off state.

LATCH: Pulling this pin low causes a fault to latch until this pin is brought high or a power on reset is attempted. However, pulling this pin high before the reset time is reached will not clear the fault until the reset time is reached. Keeping LATCH high will result in normal operation of the fault timer. Users should note there will be an RC delay dependent upon the external capacitor at this pin.

MAXI: This pin programs the maximum allowable sourcing current. Since VREF/CATFLT is a regulated voltage, a voltage divider can be derived to generate the program level for MAXI. The current level at which the output appears as a current source is equal to the voltage on MAXI divided by the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on MAXI (to VOUT), and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUTPUT: Gate drive to the NMOS pass element.

PLIM: This feature ensures that the average external NMOS power dissipation is controlled. A resistor is connected from this pin to the drain of the external NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the 3% level.

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VOUT, a fault is sensed, and CT starts to charge.

SHTDWN: This pin provides shutdown control. Interface to this pin is usually performed through level shift transistors. When shutdown is driven low, the output disables the NMOS pass device.

VDD: Power to the I.C. Is supplied by an external current limiting resistor on initial power-up or if the load is shorted. As the load voltages rises (VOUT), a small amount of power is drawn from VOUT by an internal charge pump. The charge pump's input voltage is regulated by an on-chip 5V zener. Power to VDD is supplied by the charge pump under normal operation (i.e., external FET is on).

PIN DESCRIPTIONS (cont.)

VOUT: Ground reference for the IC.

VREF/CATFLT: This pin primarily provides an output reference for the programming of MAXI. Secondarily, it provides catastrophic fault output indication. Under a catastrophic fault, when the IC is unsuccessfully attempting to shutdown the NMOS pass device, this pin will pull to a low state. In an application, this pin could be connected to a second NMOS transistor in series with the main NMOS for redundancy. Due to the primary function of this pin, full gate drive would not be available to the second NMOS.

VSS: Negative reference out of the chip. Normally current fed via a resistor to ground.

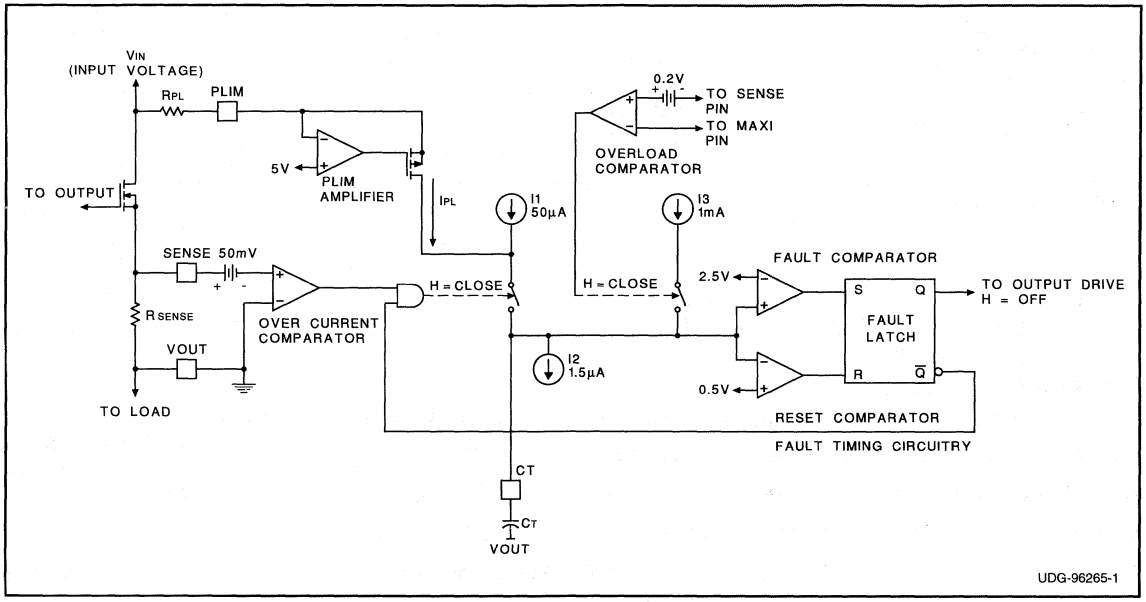


Figure 1. Fault timing circuitry for the UCC3917, including power limit and overload.

APPLICATION INFORMATION

Fault Timing

Fig. 1 shows the detailed circuitry for the fault timing function of the UCC3917. For simplicity, we first consider a typical fault mode where the overload comparator and the current source I3 do not come into play. A typical fault occurs once the voltage across the current sense resistor, RS, exceeds 50mV. This causes the over current comparator to trip and the timing capacitor to charge with current source I1 plus the current from the power limiting amplifier, or PLIM amplifier. The PLIM amplifier is designed to only source current into the CT pin once the voltage across the output FET exceeds 5V. The current IPL is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{(V_{IN} - VOUT) - 5V}{R_{PL}}$$

Note that under normal fault conditions where the output current is just above the fault level, VOUT ≅ V_{IN}, I_{PL} = 0, and the C_T charging current is just I1.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor, CT. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with current source I2 until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets (assuming LATCH is high, otherwise the fault latch will not reset until the LATCH pin is brought high or a power-on reset occurs) which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{I2}{I_{PL} + I1} \cong \frac{1.5\mu A}{I_{PL} + 50\mu A}$$

APPLICATION INFORMATION (cont.)

where I_{PL} is 0µA under normal operations (see Fig. 2).

However, under large transients, average power dissipation can be limited using the PLIM pin. A proof follows, average dissipation in the pass element is given by:

$$P_{FET\,AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \text{Duty Cycle}$$

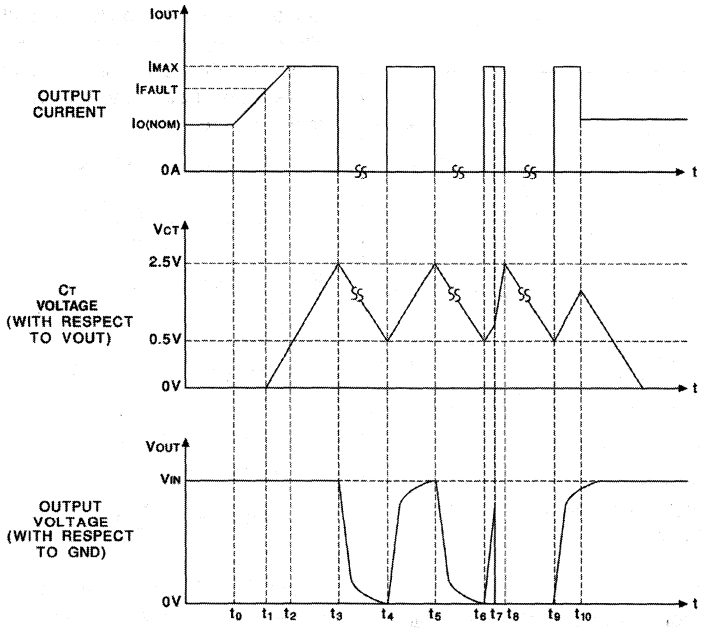
$$= (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1.5\mu A}{I_{PL} + 50\mu A}$$

Where (V_{IN} – VOUT) >> 5V,

$$I_{PL} \cong \frac{V_{IN} - VOUT}{R_{PL}}$$

and where I_{PL} >> 50µA, the duty cycle can be approximated as:

$$\frac{1.5\mu A \bullet R_{PL}}{V_{IN} - VOUT}.$$



UDG-96266

t0: Safe condition - output current is nominal, output voltage is at the positive rail, V_{IN}.

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 50µA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs - CT has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharges to ground.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT rises to V_{IN}.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4:

t7: Output short circuit - if VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for V_{IN} and R_{PL}.

t8: Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition - return to normal operation of the circuit breaker.

Note that t6 – t5 ≅ 36 • (t5 – t4).

Figure 2. Nominal timing diagram.

APPLICATION INFORMATION (cont.)

Therefore the average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1.5\mu A \bullet R_{PL}}{V_{IN} - VOUT}$$

$$= I_{MAX} \bullet 1.5\mu A \bullet R_{PL}$$

Notice that since (V_{IN} – VOUT) cancels, average power dissipation is limited in the NMOS pass element (see Fig. 3). Also, a value for R_{PL} can be roughly determined from this approximation.

$$R_{PL} = \frac{P_{FET\ AVG}}{I_{MAX} \bullet 1.5\mu A}$$

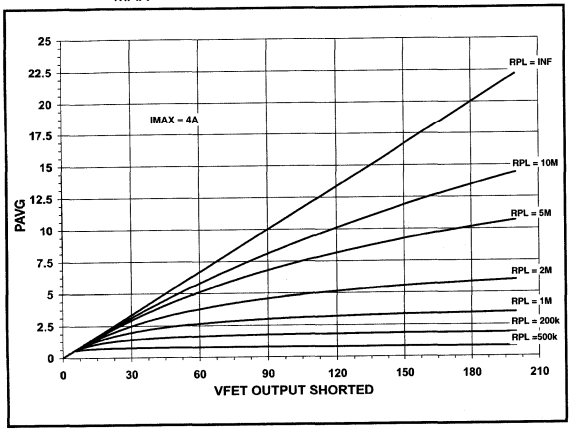


Figure 3. Plot of average power vs. FET voltage for increasing values of R_{PL}.

Overload Comparator

The overload comparator provides protection against a shorted load during normal operation when the external N-channel FET is fully enhanced. Once the FET is fully enhanced the linear current amplifier essentially saturates and the system is in effect operating open loop. Once the FET is fully enhanced the linear current amplifier requires a finite amount of time to respond to a shorted output possibly destroying the external FET. The overload comparator is provided to quickly shutdown the external MOSFET in the case of a shorted output (if the FET is fully enhanced). During an output short CT is charged by I3 at ~ 1mA. The current threshold for the overload comparator is a function of I_{MAX} and a fixed offset and is defined as:

$$I_{OVERLOAD} = I_{MAX} + 200mV / R_S$$

Once the overcurrent comparator trips the UCC3917 will enter programmed fault mode (hiccup or latched). It should be noted that on subsequent retries during Hiccup mode or if a short should occur when the UCC3917 is actively limiting the current, the output current will not exceed I_{MAX}. In the event that the external FET does not respond during a fault the UCC3917 will set the VREF/CATFLT pin low to indicate a catastrophic failure.

Selecting the Minimum Timing Capacitance

To ensure that the IC will startup correctly the designer must ensure that the fault time programmed by CT exceeds the startup time of the load. The startup time (T_{START}) is a function of several components; load resistance and load capacitance, soft start components R1, R2 and C_{SS}, the power limit current contribution determined by R_{PL}, and C_{IN}. The equation for T_{START} will depend on whether the load is resistive or constant current in nature.

For a constant current load: (1)

$$T_{START} = \frac{C_{LOAD} \bullet VIN}{I_{MAX} - I_{LOAD}}$$

For a resistive load : (2)

$$T_{START} = -R_{LOAD} \bullet C_{LOAD} \bullet \ell n\left[1 - \frac{V_{OUT}}{I_{MAX} \bullet R_{LOAD}}\right]$$

If the power limit function is not be used then CT(min) can be easily found:

$$CT(\min) = \frac{I_{CH} \bullet T_{START}}{dV_{CT}} \quad (3)$$

where dV_{CT} is the hysteresis on the fault detection circuitry. During operation in the latched fault mode configuration dVCT = 2.5V. When the UCC3917 is configured for the hiccup or retry mode of fault operation dV_{CT}=2.0V.

If the power limit function is used the CT charging current becomes a function of I_{CH} + I_{PL}. And CT(min) is found from:

$$CT(\min) \cong \left[I_{CH} + \frac{VIN - I_{MAX} \bullet R_{LOAD} \bullet \left(1 - e^{\frac{-t}{R_{LOAD} \bullet C_{LOAD}}}\right)}{R_{PL}} \right] \bullet \frac{dt}{dV_{CT}} \quad (4)$$

APPLICATION INFORMATION (cont.)

Since I_{PL} is a function of the output voltage, V_{OUT}, which varies over time, equation 4 must be integrated to solve for CT(min). However equation 4 can be easily approximated if the output voltage slews. If the output voltage slews linearly then the CT charge current contribution from the power limit circuitry is shown to be at a peak when V_{OUT} = 0V and at 0A when V_{OUT}=VIN-V_{PL}, where V_{PL} is the power limit voltage threshold. I_{PL} is shown in Fig. 4 below.

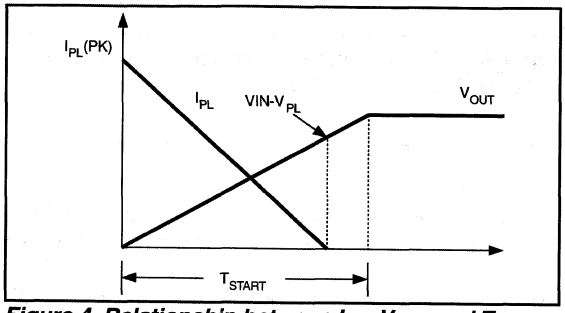


Figure 4. Relationship between I_{PL}, V_{OUT} and T_{START}.

Where I_{PL} is defined as:

$$I_{PL} \equiv \frac{(VIN - V_{OUT} - V_{PL})}{R_{PL}} \quad (5)$$

The average I_{PL} current for the interval (0, T_{START}) from Fig. 4 is defined as:

$$I_{PL}(AVG) \equiv \frac{(VIN - V_{PL})^2}{2 \bullet R_{PL} \bullet VIN} \quad (6)$$

Equation 4 can now be simplified to:

$$CT(\min) \cong \frac{I_{CH} + I_{PL}(AVG)}{dV_{CT}} \bullet T_{START} \quad (7)$$

Please note that the actual on-time in hiccup mode when operating into a short is defined by:

$$T(on) = \frac{CT \bullet dV_{CT}}{I_{CH} + I_{PL}(pk)} \ seconds \quad (8)$$

where dV_{CT} ~2.0V and

$$I_{PL}(pk) = \frac{VIN}{R_{PL}} \ A \quad (9)$$

Selecting Other External Components

Other external components are necessary for correct operation of the IC. Referring to the application diagram at the back of the data sheet, resistors R_{SENSE}, R_{SS}, R1, R2 and R3 are required and follow certain equations with a brief description following where applicable:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}} \text{ (Sense Resistor)}$$

$$R_{SS} = \frac{V_{IN} - 5V}{5mA} \text{ (Connected between VSS and GND)}$$

$$R3 = \frac{V_{IN} - 10}{5mA} \text{ (Used in series with a diode to connect VIN to VDD)}$$

$(R1 + R2) > 20k\Omega$ (Current limit out of VREF)

Lastly, the external capacitors used for the charge pump are required and need to equal 0.1µF, i.e. C_{IN} = CH = C1 = C2 = 0.1µF.

LEVEL Shift Circuitry (Optional)

The level shift circuitry shown in Fig. 5 and Fig.6 represents a way of interfacing to LATCH, SHTDWN, and FLTOUT. These pins provide functionality that is not necessary for normal operation of the IC but may prove useful to the application. The resistor, R, shown in both figures is used for the current limiting and follows R_{MAX} = V_{SD}/I_{SD}. The capacitor, C, shown in both figures is operational to the level shift circuitry and keeps spurious signals from occurring during transients. It's recommended value is C_{MIN} = 0.1nF. It should be noted that the use of the capacitor, C, will cause delays into and out of these pins.

APPLICATION INFORMATION (cont.)

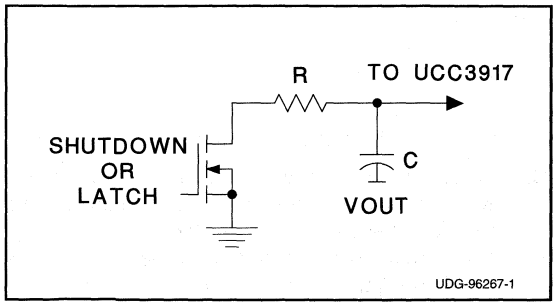


Figure 5. Potential level shift circuitry to interface to LATCH and SHTDWN on the UCC3917.

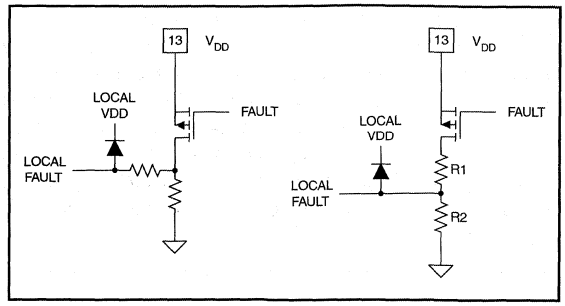


Figure 6. Potential level shift circuitry to interface to FLTOUT on the UCC3917.

SAFETY RECOMMENDATIONS

Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3917 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

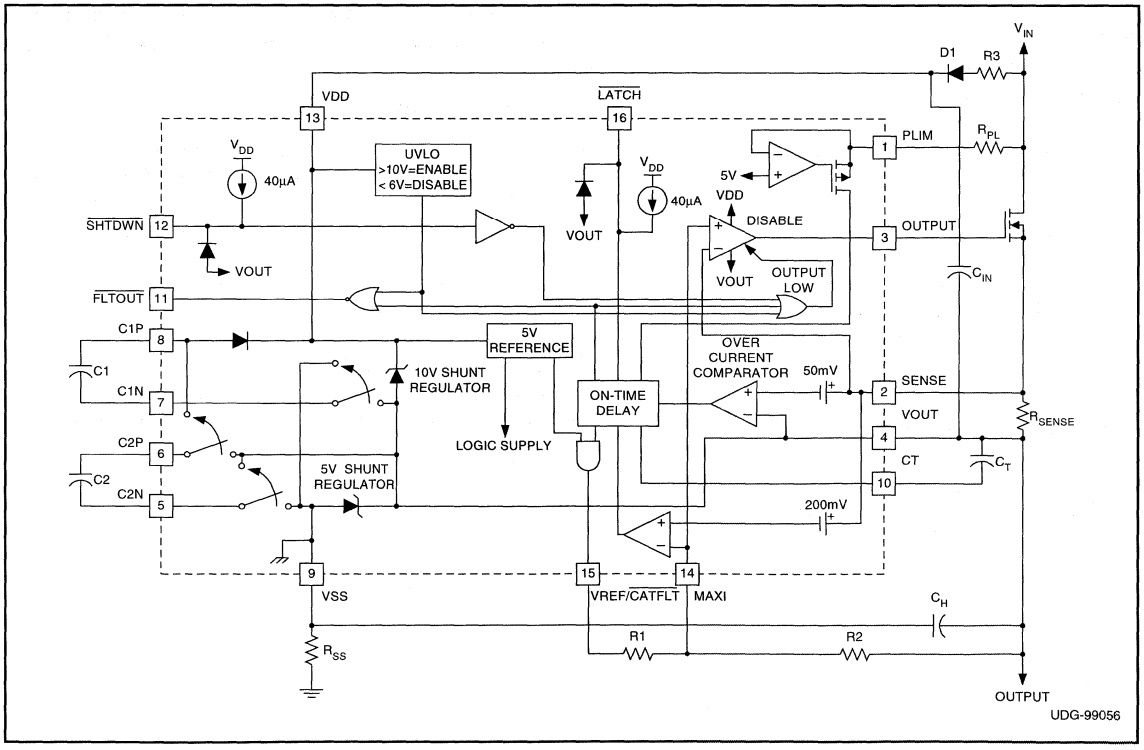


Figure 7. Positive floating hot swap power manager UCC1917, UCC2917 and UCC3917.

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application INFO available

UCC2918
UCC3918

Low On Resistance Hot Swap Power Manager

FEATURES

- Integrated 0.06Ω Power MOSFET
- 3V to 6V Operation
- External Analog control of Fault Current from 0A to 4A
- Independent Analog Control of Current Limit up to 5A
- Fast Overload Protection
- Minimal External Components
- 1μA I_{CC} when Disabled
- Programmable On Time
- Programmable Start Delay
- Fixed 3% Duty Cycle

DESCRIPTION

The UCC3918 Low on Resistance Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only components needed to operate the device, other than supply bypassing, are a timing capacitor, and 2 programming resistors. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits the average output power. The IFAULT pin allows linear programming of the fault level current from 0A to 4A.

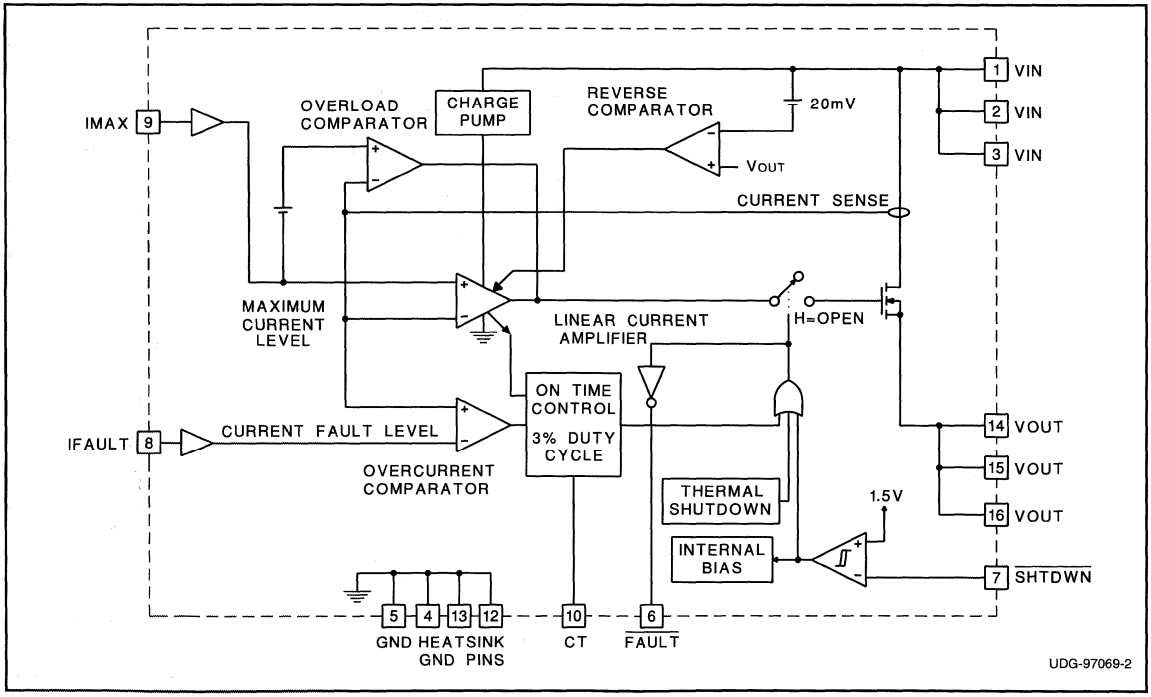
Fast overload protection is accomplished by an additional overload comparator. Its threshold is internally set above the maximum sourcing current limit setting. In the event of a short circuit or extreme current condition, this comparator is tripped, shutting down the output. This function is needed since the maximum sourcing current limit loop has a finite bandwidth.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.06Ω. When the output current exceeds the fault level or the maximum sourcing level, the output remains on, but the fault timer starts charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions form a switch to a constant current source.

5

BLOCK DIAGRAM

(continued)



DESCRIPTION (continued)

The UCC3918 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr. The UCC3918 can also be put into the sleep mode, drawing only 1µA of supply current.

Other features include an open drain fault output indicator, thermal shutdown, undervoltage lockout, 3V to 6V operation, and a low thermal resistance small outline power package.

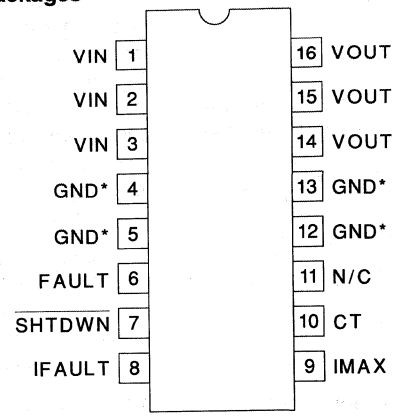
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN) 8V
SOIC Power Dissipation 2.5W
Fault Output Sink Current. 50mA
Fault Output Voltage . . . . . VIN
Output Current (DC) . . . . . Internally Limited
TTL Input Voltage . . . . . –0.3V to VIN
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Consult Packaging Section of Databook for thermal limitations and considerations of package.

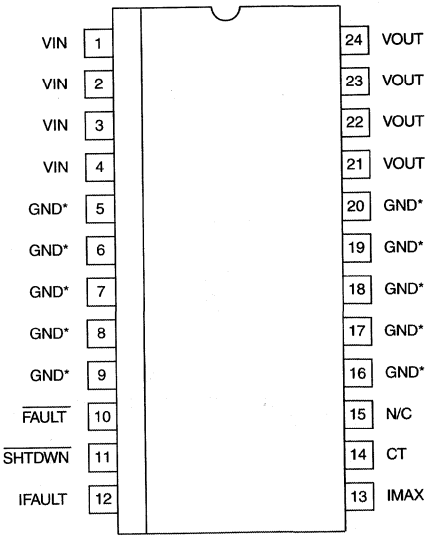
CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N Package, DP Package
Q,L Packages



** Pin 5 serves as the lowest impedance to the electrical ground. Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch PCB areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.*

TSSOP-24 (Top View)
PWP Package



** Pin 9 serves as the lowest impedance to the electrical ground. Pins 5, 6, 7, 8, 16, 17, 18, 19 and 20 serve as heat sink/ground.*

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3918, –40°C to 85° for the UCC2918, VIN = 5V. R_{IMAX} = 42.2k, R_{IFAULT} = 52.3k, $\overline{SHTDWN}$ = 2.4. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range, VIN		3	5	6	V
V_{DD} Supply Current	No Load		1	2	mA
Sleep Mode Current	$\overline{SHTDWN}$ = 0.2V		0.5	5	µA
Output Section					
RDS_{ON}	I_{OUT} = 1A to 4A, VIN = 5V, TA = 25°C		0.075	0.095	Ω
	I_{OUT} = 1A to 4A, VIN = 3V, TA = 25°C		0.09	0.116	Ω
	I_{OUT} = 1A to 4A, VIN = 5V		0.75	0.125	Ω
	I_{OUT} = 1A to 4A, VIN = 3V		0.09	0.154	Ω
Initial Startup Time	(Note 1)		100		µS
Thermal Shutdown	(Note 1)		170		DEG
Output Section (cont)					
Thermal Hysteresis	(Note 1)		10		DEG
Output Leakage	$\overline{SHTDWN}$ = 0.2V			20	µA
Trip Current	R_{IFAULT} = 105k	0.75	1	1.25	A
	R_{IFAULT} = 52.3k	1.7	2	2.3	A
	R_{IFAULT} = 34.8k	2.5	3	3.5	A
	R_{IFAULT} = 25.5k	3.3	4	4.7	A
Maximum Output Current	R_{IMAX} = 118k	0.3	1	1.7	A
	R_{IMAX} = 60.4k	1	2	3	A
	R_{IMAX} = 42.2k	2	3	4	A
	R_{IMAX} = 33.2k	2.5	3.8	5.1	A
	R_{IMAX} = 27.4k	3.0	4.6	6.2	A
Fault Section					
C_T Charge Current	V_{CT} = 1V	–50	–36	–22	µA
C_T Discharge Current	V_{CT} = 1V	0.5	1.2	2.0	µA
Fault Section (cont.)					
Output Duty Cycle	VOUT = 0V	1.5	3	6	%
C_T Fault Threshold		0.8	1.3	1.8	V
C_T Reset Threshold		0.25	0.5	0.75	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	2.0	V
Shutdown Hysteresis			100		mV
Input Low Current	$\overline{SHTDWN}$ = 0V	–500	0	500	nA
Input High Current	$\overline{SHTDWN}$ = 2V	–2	–1	–0.5	µA
Open Drain Fault Output					
High Level Output Current				1	µA
Low Level Output Voltage	I_{OUT} = 1mA		0.4	0.9	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor connected to this pin sets the maximum fault time. The maximum must be more than the time to charge external load capacitance. The maximum fault time is defined as

$$T_{FAULT} = 27.8 \bullet 10^3 \bullet C_T$$

Once the fault time is reached the output will shutdown for a time given by

$$T_{SD} = 0.833 \bullet 10^6 \bullet C_T,$$

this equates to a 3% duty cycle.

FAULT: Open drain output, which pulls low upon any condition which causes the output to open; Fault, Thermal Shutdown, Shutdown, and maximum sourcing current greater than the fault time.

GND: This is the most negative voltage in the circuit. All 4 ground pins should be used, and properly heat sunk on the PCB.

IFAULT: A resistor connected from this pin to ground sets the fault threshold. The resistor vs fault current is set by the formula

$$R_{FAULT} = \frac{105k}{I_{TRIP}}$$

IMAX: A resistor connected from this pin to ground sets the maximum sourcing current. The resistor vs the output sourcing current is set by the formula,

$$R_{FAULT} = \frac{126k}{Maximum\,Sourcing\,Current}$$

$\overline{\text{SHTDWN}}$: When this pin is brought low, the IC is put into sleep mode. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: This is the input voltage to the UCC3918. The recommended operating voltage range is 3V to 6V. All VIN pins should be connected together and to the power source.

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately VIN – 0.06Ω • I_{OUT}. All VOUT pins should be connected together and to the load.

APPLICATION INFORMATION

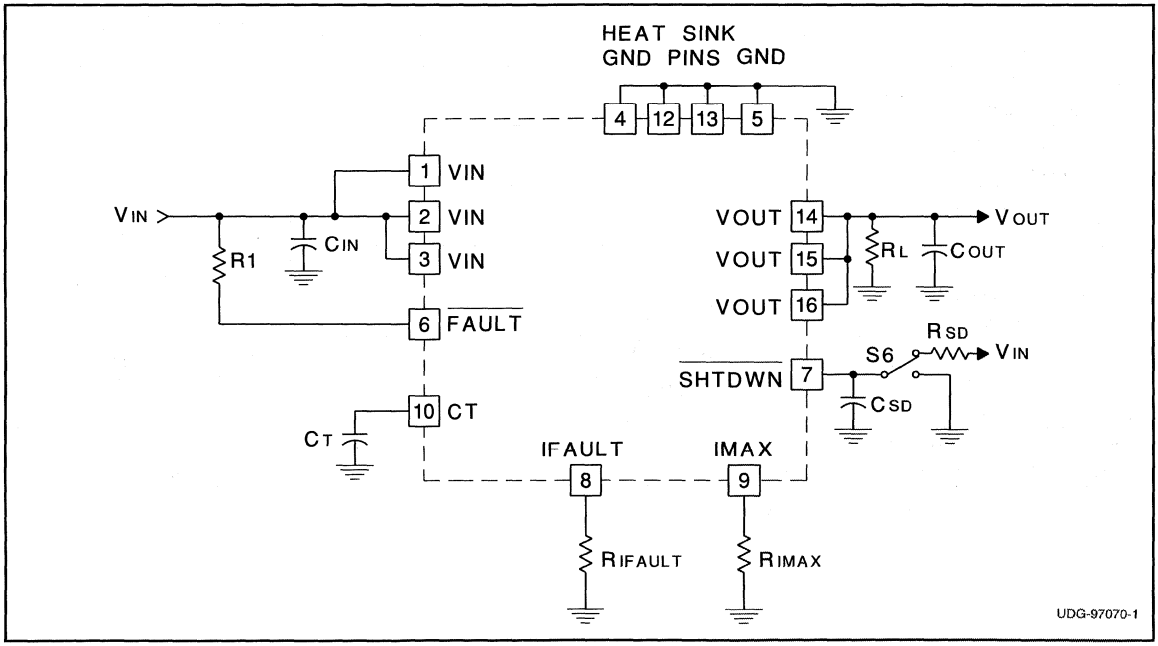


Figure 1. Evaluation Circuit

APPLICATION INFORMATION (cont.)

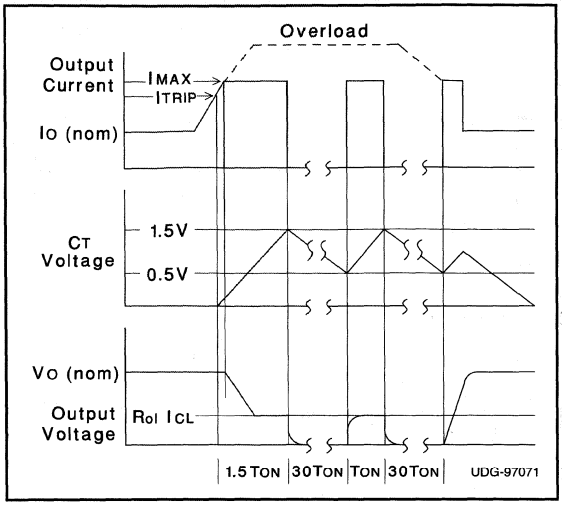


Figure 2. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3918 Under Fault

Estimating Maximum Load Capacitance

For circuit breaker applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit breaker, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle of the current-limited circuit breaker from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

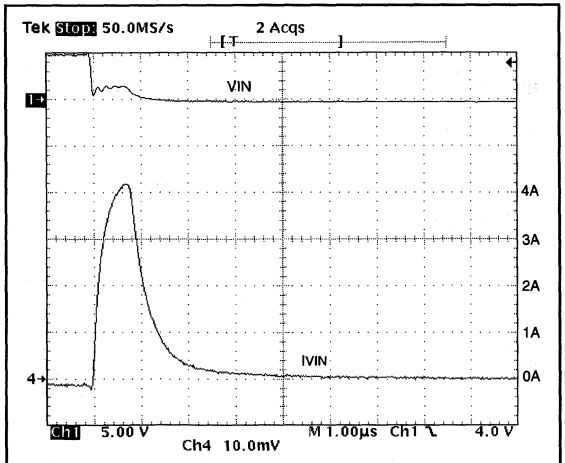
For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT}(\max) \approx (I_{MAX} - I_{LOAD}) \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage and I_{MAX} is the maximum, sourcing current.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

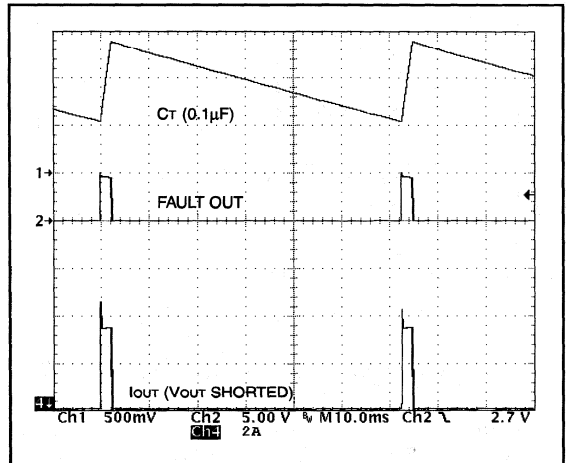
$$C_{OUT}(\max) \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet ln\left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$



COUT	RL	CIN	RIFAULT	RIMAX
22µF	5Ω	5µF	52.3k	42.0k

Input driven with a pulse generator, shows C_{OUT} discharging through R_L and conducting through UCC3918 FET in the reverse direction.

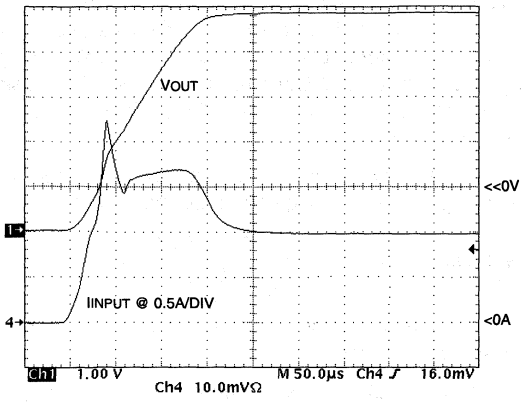
Figure 3.



VOUT	RL	CIN	RIFAULT	RIMAX
0V	SHORT	5µF	52.3k	42.2k

Figure 4. UCC3918 in Shorted Condition

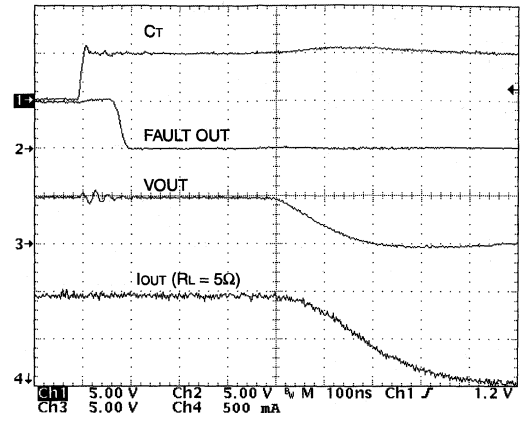
APPLICATION INFORMATION



COUT	RL	CIN	RIFAULT	RIMAX
22µF	5Ω	5µF	52.3k	60.4k

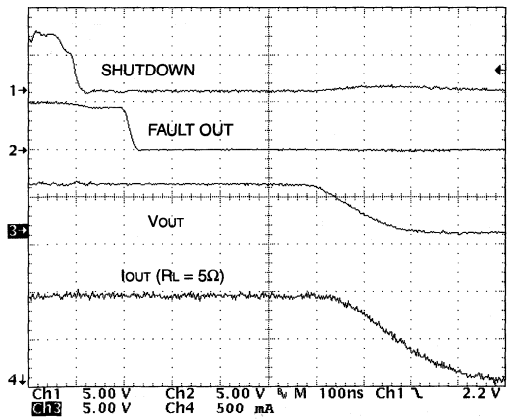
Input switched on through external FET. V_{OUT} shows I_{MAX} linear amplifier limiting the changing current of C_{OUT}.

Figure 5. Input Hot Swap



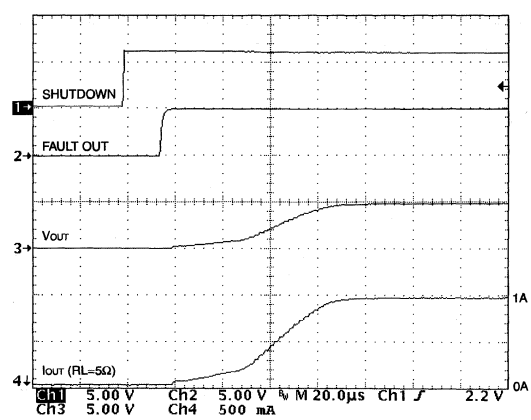
COUT	RL	CIN	RIFAULT	RIMAX	CT
0µF	5Ω	5µF	52.3k	42.4k	OPEN

Figure 6. CT to VOUT Delay (Fault Condition)



COUT	RL	CIN	RIFAULT	RIMAX
0µF	5Ω	5µF	52.3k	42.4k

Figure 7. Shutdown Delay to V_{OUT} Off



COUT	RL	CIN	RIFAULT	RIMAX
0µF	5Ω	5µF	52.3k	42.4k

Figure 8. Shutdown Delay to VOUT On

APPLICATION INFORMATION

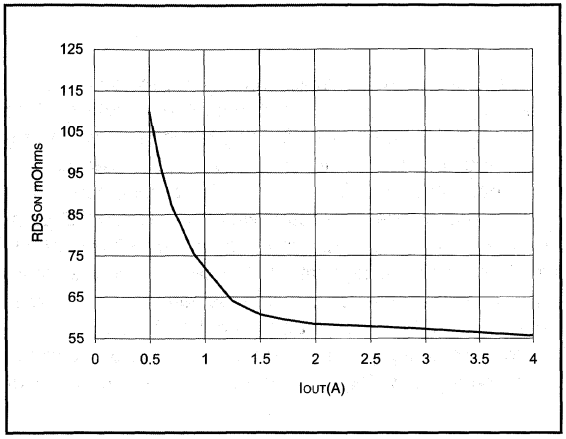


Figure 9. RDS_{ON} vs I_{OUT}

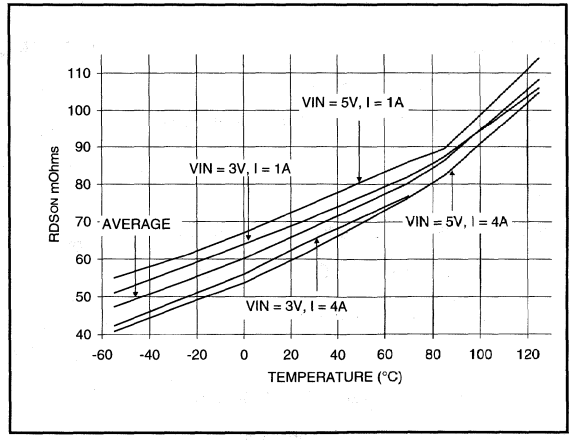


Figure 10. RDS_{ON} vs Temperature

SAFETY RECOMMENDATIONS

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3918 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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UNITRODE

application INFO available

UCC1919
UCC2919
UCC3919
PRELIMINARY

3V to 8V Hot Swap Power Manager

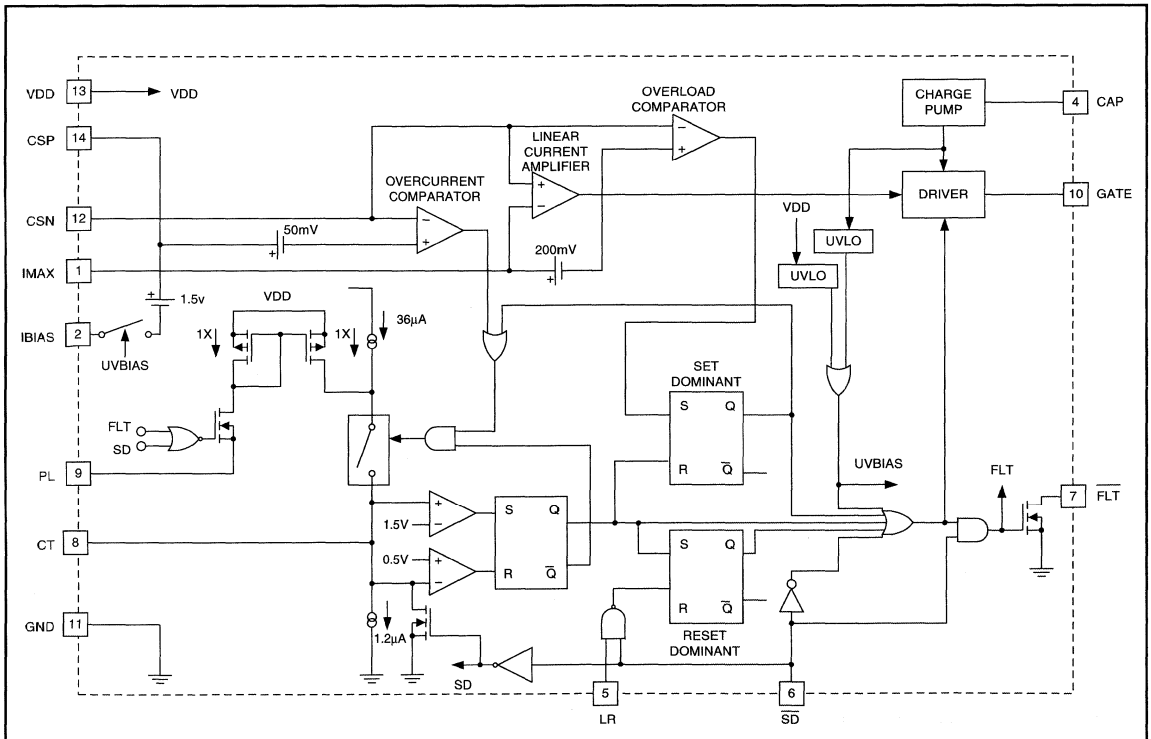
FEATURES

- Precision Fault Threshold
- Charge Pump for Low RDS_{ON} High Side Drive
- Differential Sense Inputs
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Fault Time
- Fault Output Indicator
- Manual and Automatic Reset Modes
- Shutdown Control w/Programmable Softstart
- Undervoltage Lockout
- Electronic Circuit Breaker Function

DESCRIPTION

The UCC3919 family of Hot Swap Power Managers provide complete power management, hot swap, and fault handling capability. The UCC3919 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The UCC3919 has two reset modes, selected with the TTL/CMOS compatible L/R pin. In one mode, when a fault occurs the IC repeatedly tries to reset itself at a user defined rate, with user defined maximum output current and pass transistor power dissipation. In the other mode the output latches off and stays off until either the L/R pin is reset or the shutdown pin is toggled. The on board charge pump circuit provides the necessary gate voltage for an external N-channel power FET.

BLOCK DIAGRAM



UDG-98123

Note: Pins shown for 14-pin package.

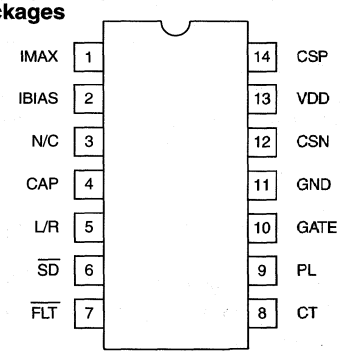
ABSOLUTE MAXIMUM RATINGS

VDD . . . . . –0.3V to 10V
Pin Voltage
(All pins except CAP and GATE) . . . . . –0.3V to VDD + 0.3V
Pin Voltage
(CAP and GATE) . . . . . –0.3V to 15V
PL Current . . . . . 0.5mA to –10mA
IBIAS Current . . . . . 0mA to 3mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

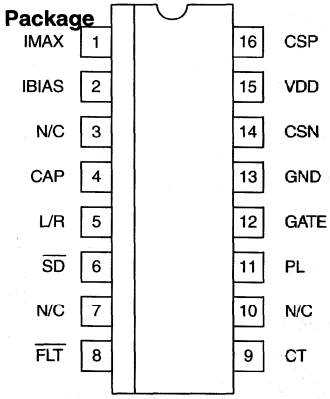
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-14, (Top View)
N, J Packages



SOIC-16, TSSOP-16 (Top View)
D or PW Package



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ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 5V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85° for the UCC2919 and –55°C to 125°C for the UCC1919. All voltages are with respect to GND. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	VDD = 3V		0.5	1	mA
	VDD = 8V		1	1.5	mA
Shutdown Current	$\overline{SD}$ = 0.2V		1	5	µA
Undervoltage Lockout					
Minimum Voltage to Start		2.5	2.75	3	V
Minimum Voltage after Start		2	2.25	2.5	V
Hysteresis		0.25	0.5	0.75	V
IBIAS					
Output Voltage, (0µA < I_{OUT} < 15µA)	25°C, referred to CSP	1.47	1.5	1.53	V
	Over Temperature Range, referred to CSP	1.44	1.5	1.56	V
Maximum Output Current		1	2		mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 5V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85° for the UCC2919 and –55°C to 125°C for the UCC1919. All voltages are with respect to GND. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense					
Over Current Comparator Offset	Referred to CSP, 3V ≤ VDD ≤ 8V	–55	–50	–45	mV
Linear Current Amplifier Offset	V_{IMAX} = 100mV, Referred to CSP, 3V ≤ VDD ≤ 8V	–110	–100	–90	mV
	V_{IMAX} = 400mV, Referred to CSP, 3V ≤ VDD ≤ 8V	–410	–400	–390	mV
Overload Comparator Offset	V_{IMAX} = 100mV, Referred to CSP, 3V ≤ VDD ≤ 8V	–360	–300	–240	mV
CSN Input Common Mode Voltage Range	Referred to VDD, 3V ≤ VDD ≤ 8V, (Note 1)	–1.5		0.2	V
CSP Input Common Mode Voltage Range	Referred to VDD, 3V ≤ VDD ≤ 8V, (Note 1)	0		0.2	V
Input Bias Current CSN			1	5	µA
Input Bias Current CSP			100	200	µA
Current Fault Timer					
CT Charge Current	V_{CT} = 1V	–56	–35	–16	µA
CT Discharge Current	V_{CT} = 1V	0.5	1.2	1.9	µA
On Time Duty Cycle in Fault	I_{PL} = 0	1.5	3	6	%
CT Fault Threshold		1.0	1.5	1.7	V
CT Reset Threshold		0.25	0.5	0.75	V
IMAX					
Input Bias Current	V_{IMAX} = 100mV, Referred to CSP	–1	0	1	µA
Power Limiting Section					
Voltage on PL	I_{PL} = –250µA, Referred to VDD	–1.0	–1.4	–1.9	V
	I_{PL} = –1.5mA, Referred to VDD	–0.5	–1.8	–2.2	V
On Time Duty Cycle in Fault	I_{PL} = –250µA	0.25	0.5	1	%
	I_{PL} = –1.5mA	0.05	0.1	0.2	%
$\overline{SD}$ and L/R Inputs					
Input Voltage Low				0.8	V
Input Voltage High		2			V
L/R Input Current		1	3	6	mA
$\overline{SD}$ Internal Pulldown Impedance		100	270	500	kΩ
$\overline{FLT}$ Output					
Output Leakage Current	VDD = 5V			10	µA
Output Low Voltage	I_{OUT} = 10mA			1	V
FET GATE Driver and Charge Pump					
Peak Output Current	V_{CAP} = +15V, V_{GATE} = 10V	–3	–1	–0.25	mA
Peak Sink Current	V_{GATE} = 5V		20		mA
Fault Delay			100	300	nS
Maximum Output Voltage	VDD = 3V, Average I_{OUT} = 1µA	8	10	12	V
	VDD = 8V, Average I_{OUT} = 1µA	12	14	16	V
Charge Pump UVLO Minimum Voltage to Start	VDD = 3V	6.5	7.5		V
	VDD = 8V	6.5	8		V
Charge Pump Source Impedance	VDD = 5V, Average I_{OUT} = 1µA	50	100	150	kΩ

Note 1: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

CAP: A capacitor is placed from this pin to ground to filter the output of the on board charge pump. A .01µF to 0.1µF capacitor is recommended .

CSN: The negative current sense input signal.

CSP: The positive current sense input signal.

CT: Input to the duty cycle timer. A capacitor is connected from this pin to ground, setting the off time and the maximum on time of the overcurrent protection circuits.

$\overline{\text{FLT}}$: Fault indicator. This open drain output will pull low under any fault condition where the output driver is disabled. This output is disabled when the IC is in low current standby mode.

GATE: The output of the linear current amplifier. This pin drives the gate of an external N-channel MOSFET pass transistor. The linear current amplifier control loop is internally compensated, and guaranteed stable for output load (gate) capacitance between 100pF and .01µF. In applications where the GATE voltage (or charge pump voltage) exceeds the maximum Gate-to-Source voltage ratings (V_{GS}) for the external N-channel MOSFET, a Zener clamp may be added to the gate of the MOSFET. No additional series resistance is required since the internal charge pump has a finite output impedance of 100kΩ typical.

GND: The ground reference for the device.

IBIAS: Output of the on board bias generator internally regulated to 1.5V below CSP. A resistor divider between this pin and CSP can be used to generate the IMAX voltage. The bias circuit is internally compensated, and requires no bypass capacitance. If an external bypass is required due to a noisy environment, the circuit will be stable with up to .001µF of capacitance. The bypass must be to CSP, since the bias voltage is generated with respect to CSP. Resistor R2 (Figure 4) should be greater than 50kΩ to minimize the effect of the finite input impedance of the IBIAS pin on the IMAX threshold.

IMAX: Used to program the maximum allowable sourcing current. The voltage on this pin is with respect to CSP. If the voltage across the shunt resistor exceeds this voltage the linear current amplifier lowers the voltage at GATE to limit the output current to this level. If the voltage across the shunt resistor goes more than 200mV beyond this voltage, the gate drive pin GATE is immediately driven low and kept low for one full off time interval.

L/R: Latch/Reset. This pin sets the reset mode. If L/R is low and a fault occurs the device will begin duty ratio current limiting. If L/R is high and a fault occurs, GATE will go low and stay low until L/R is set low. This pin is internally pulled low by a 3µA nominal pulldown.

PL: Power Limit. This pin is used to control average power dissipation in the external MOSFET. If a resistor is connected from this pin to the source of the external MOSFET, the current in the resistor will be roughly proportional to the voltage across the FET. As the voltage across the FET increases, this current is added to the fault timer charge current, reducing the on time duty cycle from its nominal value of 3% and limiting the average power dissipation in the FET.

$\overline{\text{SD}}$: Shutdown pin. If this pin is taken low, GATE will go low, and the IC will go into a low current standby mode and CT will be discharged. This TTL compatible input must be driven high to turn on.

VDD: The power connection for the device.

APPLICATION INFORMATION

The UCC3919 monitors the voltage drop across a high side sense resistor and compares it against three different voltage thresholds. These are discussed below. Figure 1 shows the UCC3919 waveforms under fault conditions.

Fault Threshold

The first threshold is fixed at 50mV. If the current is high enough such that the voltage on CSN is 50mV below CSP, the timing capacitor C_T begins to charge at about 35µA if the PL pin is open. (Power limiting will be discussed later). If this threshold is exceeded long enough for C_T to charge to 1.5V, a fault is declared and the external MOSFET will be turned off. It will either be latched off (until the power to the circuit is cycled, the L/R pin is taken low, or the $\overline{\text{SD}}$ pin is toggled), or will retry after a fixed off time (when C_T has discharged to 0.5V), depending on whether the L/R pin is set high or low by the user. The equation for this current threshold is simply:

$$I_{FAULT} = \frac{0.05}{R_{SENSE}} \quad (1)$$

The first time a fault occurs, C_T is at ground, and must charge 1.5V. Therefore:

$$t_{FAULT} = t_{ON}(\text{sec}) = \frac{C_T(\mu F) \bullet 1.5}{35} \quad (2)$$

APPLICATION INFORMATION

In the retry mode, the timing capacitor will already be charged to 0.5V at the end of the off time, so all subsequent cycles will have a shorter ton time, given by:

$$t_{FAULT} \cong t_{ON}(\text{sec}) = \frac{C_T(\mu F)}{35} \quad (3)$$

Note that these equations for ton are without the power limiting feature (R_{PL} pin open). The effects of power limiting on ton will be discussed later.

The off time in the retry mode is set by C_T and an internal 1.2µA sink current. It is the time it takes C_T to discharge from 1.5V to 0.5V. The equation for the off time is therefore:

$$t_{OFF}(\text{sec}) = \frac{C_T \mu F}{1.2} \quad (4)$$

Shutdown Characteristics

When the $\overline{SD}$ pin is set to TTL high (above 2V) the UCC3919 is guaranteed to be enabled. When $\overline{SD}$ is set to a low TTL (below 0.8V) the UCC3919 is guaranteed to be disabled, but may not be in ultra low current sleep mode. When $\overline{SD}$ is set to 0.2V or less, the UCC3919 is guaranteed to be disabled and in ultra low current sleep mode. See Fig. 1.

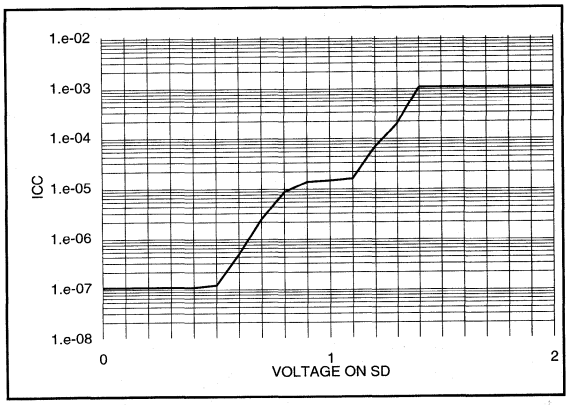


Figure 1. Typical Shutdown Current

IMAX Threshold

The second threshold is programmed by the voltage on IMAX (measured with respect to the CSP pin). This controls the maximum current, IMAX, that the UCC3919 will allow to flow into the load during the MOSFET on time. A resistive divider connected between IBIAS and CSP generates the programming voltage. When the drop across the sense resistor reaches this voltage, a linear amplifier reduces the voltage on GATE to control the external MOSFET in a constant current mode.

During this time C_T is charging, as described above. If this condition lasts long enough for C_T to charge to 1.5V, a fault will be declared and the MOSFET will be turned off. The I_{MAX} current is calculated as follows:

$$I_{MAX} = \frac{V_{CSP} - V_{IMAX}}{R_{SENSE}} \quad (5)$$

Note that if the voltage on the IMAX pin is programmed to be less than 50mV below CSP, then the UC3919 will control the MOSFET in a constant current mode all the time. No fault will be declared and the MOSFET will remain on because I_{MAX} is less than I_{FAULT}.

Overload Threshold

There is a third threshold which, if exceeded, will declare a fault and shutdown the external MOSFET immediately, without waiting for CT to charge. This "Overload" threshold is 200mV greater than the IMAX threshold (again, this is with respect to CSP). This feature protects the circuit in the event that the external MOSFET is on, with a load current below IMAX, and a short is quickly applied across the output. This allows hot-swapping in cases where the UCC3919 is already powered up (on the backplane) and capacitors are added across the output bus. In this case, the load current could rise too quickly for the linear amplifier to reduce the voltage on GATE and limit the current to IMAX. If the overload threshold is reached, the MOSFET will be turned off quickly and a fault declared. A latch is set so that C_T can be charged, guaranteeing that the MOSFET will remain off for the same period as defined above before retrying. The overload current is:

$$I_{OVERLOAD} = \frac{V_{CSP} - V_{IMAX} + 0.2}{R_{SENSE}} = I_{MAX} + \frac{0.2}{R_{SENSE}} \quad (6)$$

Note that $I_{OVERLOAD}$ may be much greater than IMAX, depending on the value of R_{SENSE}.

Power Limiting

A power limiting feature is included which allows the power dissipated in the external MOSFET to be held relatively constant during a short, for different values of input voltage. This is accomplished by connecting a resistor from the output (source of the external MOSFET) to PL. When the output voltage drops due to a short or overload, an internal bias current is generated which is equal to:

$$I_{PL} \cong \frac{(V_{IN} - V_{OUT} - V_{PL})}{R_{PL}} \quad (7)$$

APPLICATION INFORMATION (cont.)

This current is used to help charge the timing capacitor in the event that the load current exceeds I_{FAULT}. (A simplified schematic of the circuit internal to the UCC3919 is shown in Figure 2.) The result is that the on time of the MOSFET during current limit is reduced as the input voltage is increased. This reduces the effective duty cycle, holding the average power dissipated constant.

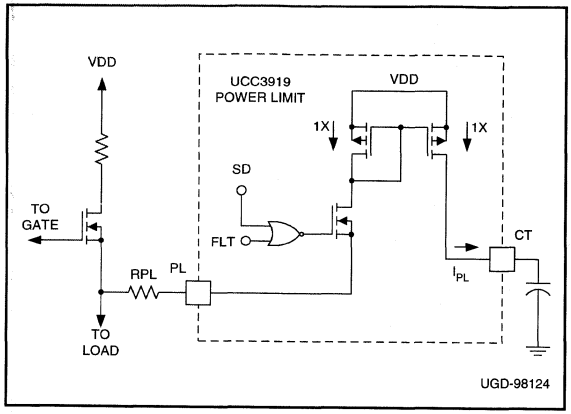


Figure 2. Power limiting circuit.

It can be seen that power limiting will only occur when I_{PL} is > 0 (it cannot be negative). For power limiting to begin to occur, the voltage drop across the MOSFET must be greater than VDD-V_{PL} or 1.4V(typ).

$$V_{IN} - V_{OUT} \geq 1.4V \tag{8}$$

The on time using R_{PL} is defined as:

$$t_{ON} = \frac{C_T \bullet \Delta V}{I_{PL} + 35 \bullet 10^{-6}} \quad \text{where } \Delta V = 1V \tag{9}$$

The graph in Figure 4 illustrates the effect of R_{PL} on the average MOSFET power dissipation into a short. The equation for the average power dissipation during a short is:

$$P_{DISS} = \frac{I_{MAX} \bullet V_{IN} \bullet 1.2 \bullet 10^{-6}}{I_{PL} + 35 \bullet 10^{-6}}, \text{ or} \tag{10}$$

$$P_{DISS} = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}}$$

If PL is left unconnected, the power limiting feature will not be exercised. In the retry mode, the duty cycle during a fault will be nominally 3%, independent of input voltage. The average power dissipation in the external MOSFET with a shorted output will be proportional to input voltage, as shown by the equation:

$$P_{DISS} = I_{MAX} \bullet V_{IN} \bullet 0.033 \tag{11}$$

Calculating C_T(min) for a Given Load Capacitance without Power Limiting

To guarantee recovery from an overload when operating in the retry mode, there is a maximum total output capacitance which can be charged for a given t_{ON} (fault time) before causing a fault. For a worst case situation of a constant current load below the fault threshold, $C_{T(min)}$ for a given output load capacitance (without power limiting) can be calculated from:

$$C_T(\text{min}) = \frac{V_{IN} \bullet C_{OUT} \bullet 35 \bullet 10^{-6}}{I_{MAX} - I_{LOAD}} \tag{12}$$

A larger load capacitance or a smaller C_T will cause a fault when recovering from an overload, causing the circuit to get stuck in a continuous hiccup mode. To handle larger capacitive loads, increase the value of C_T. The equation can be easily re-written, if desired, to solve for $C_{OUT(max)}$ for a given value of C_T.

For a resistive load of value RL and an output cap C_{OUT}, C_{Tmin} can be smaller than in the constant current case, and can be estimated from:

$$C_T(\text{min}) = \frac{-C_{OUT} \bullet R_L \bullet \ell n\left(1 - \frac{V_{IN}}{I_{MAX} \bullet R_L}\right)}{28 \bullet 10^3} \tag{13}$$

Note that in the latch mode (or when first turning on in the retry mode), since the timing capacitor is not recovering from a previous fault, it is charging from 0V rather than 0.5V. This allows up to 50% more load capacitance without causing a fault.

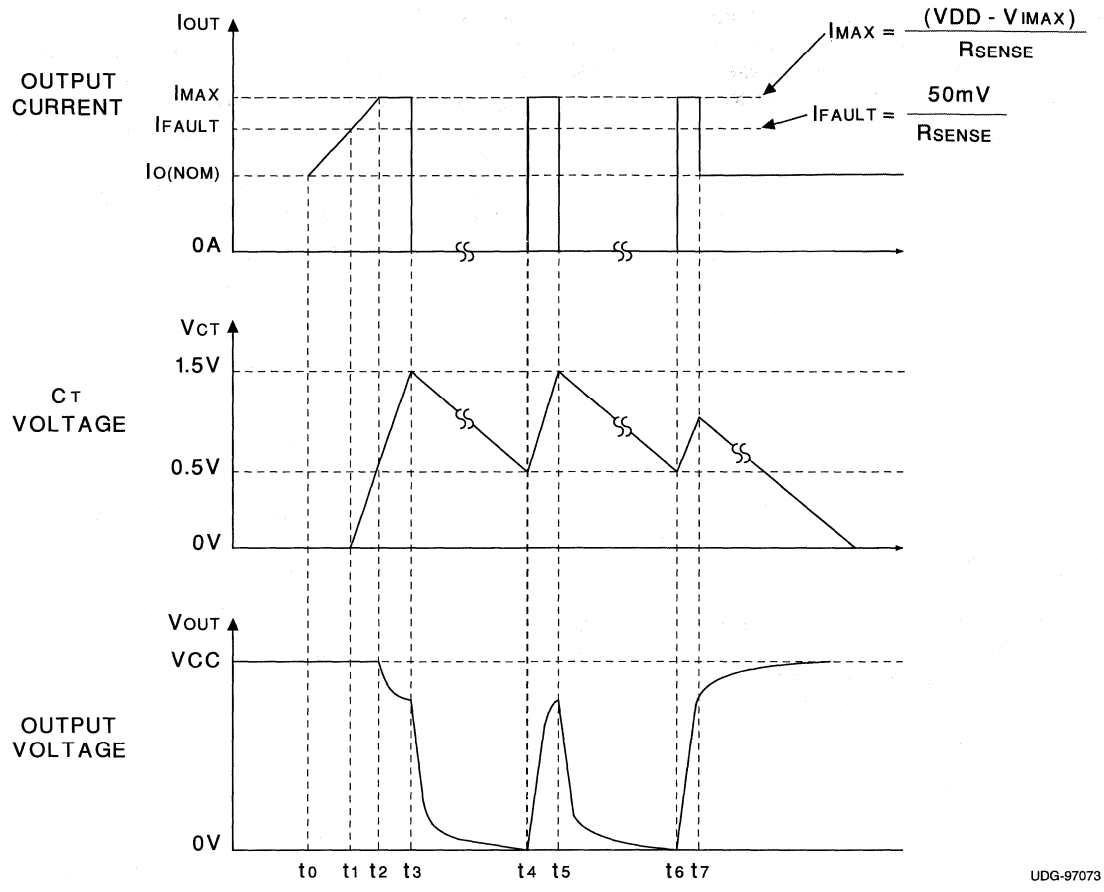
Estimating C_T(min) When Using Power Limiting

If power limiting is used, the calculation of $C_T$min for a given C_{OUT} becomes considerably more complex, especially with a resistive load. This is because the C_T charge current becomes a function of V_{OUT}, which is changing with time. The amount of capacitance that can be charged (without causing a fault) when using power limiting will be significantly reduced for the same value C_T, due to the shorter ton time.

The charge current contribution from the power limiting circuit is defined as:

$$I_{PL} \cong \frac{(V_{IN} - V_{OUT} - V_{PL})}{R_{PL}} \tag{14}$$

APPLICATION INFORMATION (cont.)



t0: Normal condition - Output current is nominal, output voltage is at positive rail, V_{CC}.

t1: Fault control reached - Output current rises above the programmed fault value, C_T begins to charge with 35µA + I_{PL}.

t2: Maximum current reached - Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs - C_T has charged to 1.5V, fault output goes low, the FET turns off allowing no output current to flow, V_{OUT} discharges to GND.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT increases.

t3 to t5: Illustrates <3% duty cycle depending upon RPL selected.

t6 = t4

t7: Fault released, normal condition - return to normal operation of the circuit breaker

Figure 3. Typical Timing Diagram

APPLICATION INFORMATION (cont.)

Constant Current Load

For a constant current load, the output capacitor will charge linearly. During that time:

$$I_{PL}(avg) \cong \frac{(V_{IN} - V_{PL})^2}{2 \bullet R_{PL} \bullet V_{IN}} \quad (15)$$

Modifying equation (12) yields:

$$C_T(\min) \cong \frac{V_{IN} \bullet C_{OUT} \bullet \left[\frac{(V_{IN} - V_{PL})^2}{2 \bullet R_{PL} \bullet V_{IN}} + 35 \bullet 10^{-6} \right]}{I_{MAX} - I_{LOAD}} \quad (16)$$

Resistive Load

Determining C_T(min) for a resistive load is more complex. First, the expression for the output voltage as a function of time is:

$$V_{OUT}(t) = I_{MAX} \bullet R_{LOAD} \left(1 - e^{-\frac{T_{START}}{R_{LOAD} \bullet C_{OUT}}} \right) \quad (17)$$

Solving for T_{START} when $V_{OUT} = V_{IN}$ yields:

$$T_{START} = -R_{LOAD} \bullet C_{OUT} \bullet \ell n \left(1 - \left(\frac{V_{IN}}{I_{MAX} \bullet R_{LOAD}} \right) \right) \quad (18)$$

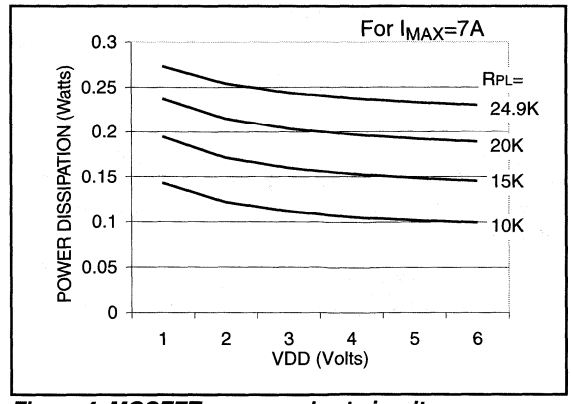


Figure 4. MOSFET average short circuit power dissipation vs. V_{IN} for values of R_{PL}.

Assuming that the device is operating in the retry mode, where C_T is charging from 0.5V to just below 1.5V in time t, C_T is defined as:

$$C_T = \frac{I_{CT} \bullet dt}{dV} = I_{CT} \bullet dt \quad \text{Where}$$

$$I_{CT} = \left(I_{PL} + 35 \bullet 10^{-6} \right) \quad (19)$$

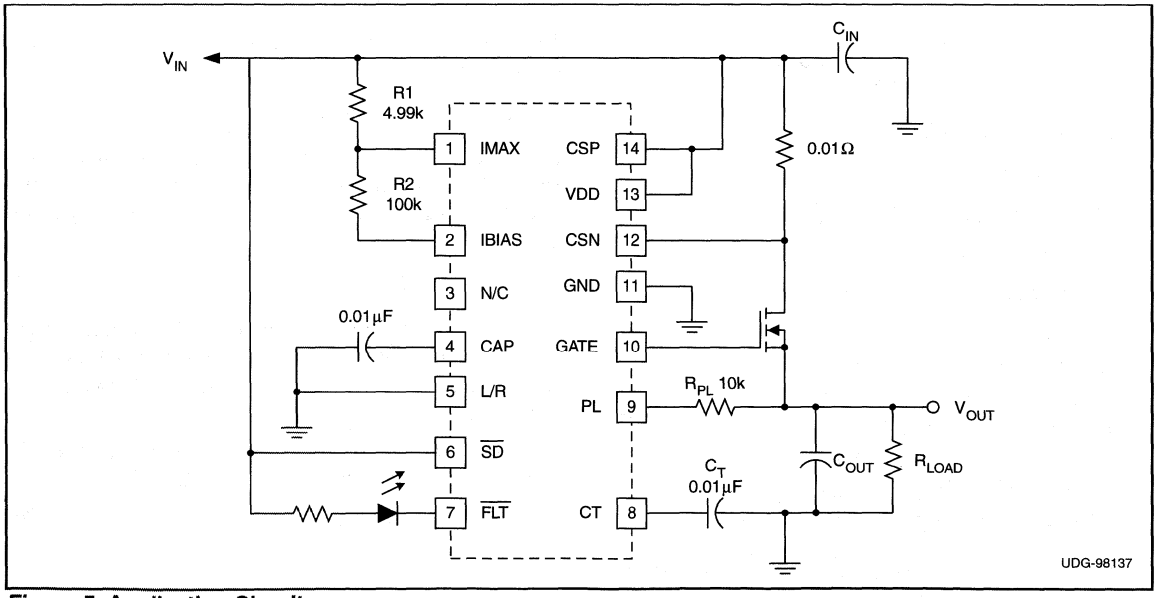


Figure 5. Application Circuit

APPLICATION INFORMATION (cont.)

Substituting equation (15) into (19) yields:

$$C_T(\text{min}) = \left(\frac{(V_{IN} - V_{PL})^2}{2 \bullet R_{PL} \bullet V_{IN}} + 35 \bullet 10^{-6} \right) \bullet dt \quad (20)$$

This yields the following expression for C_T(min) for a resistive load with power limiting. By substituting the value calculated for T_{START} in equation (18) for dt, C_T(min) is determined.

$$C_T(\text{min}) = \left[\frac{(V_{IN} \bullet V_{PL})^2}{2 \bullet R_{PL} \bullet V_{IN}} + 35 \bullet 10^{-6} \right] \bullet T_{START} \quad (21)$$

Example

The example in Figure 5 shows the UCC3919 in a typical application. A low value sense resistor and N-channel MOSFET minimize losses. With the values shown for R1, R2, and Rs, the overcurrent fault will be 5A nominal. Linear current limiting (I_{MAX}) will occur at 7.14A and the overload comparator will trip at 27A. The calculations are shown below.

$$I_{FAULT} = \frac{0.05}{R_S} = \frac{0.05}{0.01} = 5A \quad (22)$$

$$I_{MAX} = \frac{V_{CSP} - V_{IMAX}}{R_S} = \frac{1.5 \bullet R1}{(R1 + R2) \bullet R_S} = 7.14A \quad (23)$$

$$I_{OVERLOAD} = I_{MAX} + \frac{0.2}{R_S} = 7.14A + \frac{0.2}{0.01} = 27.14A \quad (24)$$

$$T_{OFF}(\text{sec}) = \frac{C_T \mu F}{1.2} = \frac{0.01}{1.2} = 8.33\,ms \quad (25)$$

With the value shown for R_{PL}:

$$I_{PL(typ)}(\textit{output shorted}) = \left(\frac{V_{IN} - V_{PL}}{R_{PL}} \right) = \left(\frac{5 - 1.6}{10k} \right) = 340\mu A \quad (26)$$

$$t_{ON}(\textit{shorted}) = \frac{C_T}{I_{PL} + 35 \bullet 10^{-6}} = \frac{0.01 \bullet 10^{-6}}{375\mu A} = 27\mu s \quad (27)$$

$$P_{DISS}(\textit{shorted}) = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}} = \frac{7.14 \bullet 5 \bullet 27\mu s}{27\mu s + 8.33 \bullet 10^{-3}} = 0.12W \quad (28)$$

For a worst case 1Ω resistive load: C_{OUT}(max) ≅ 47µF.

For a worst case 5A constant current load: C_{OUT}(max) ≅ 27µF.

With L/R grounded, the part will operate in the retry or "hiccup" mode. The values shown for C_T and R_{PL} will yield a nominal duty cycle of 0.32% and an off time of 8.3ms. With a shorted output, the average steady state power dissipation in Q1 will be less than 100mW over the full input voltage range.

If power limiting is disabled by opening R_{PL}, then:

$$t_{FAULT} = t_{ON}\,\text{sec} = \frac{C_T \mu F \bullet 1}{35} = 287\mu s \quad (29)$$

$$P_{DISS}(\textit{shorted}) = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{OFF} + t_{ON}} = \frac{7.14 \bullet 5 \bullet 287 \bullet 10^{-6}}{287 \bullet 10^{-6} + 8.33 \bullet 10^{-3}} = 1.2W\ (\textit{with}\ V_{IN} = 5V) \quad (30)$$

For a worst case 1Ω resistive load: C_{OUT}(max) ≅ 220µF.

For a worst case 5A constant current load: C_{OUT}(max) ≅ 120µF.

THERMAL CONSIDERATIONS

Steady State Conditions

In normal operation, with a steady state load current below I_{FAULT}, the power dissipation in the external MOSFET will be:

$$P_{DISS} = RDS_{ON} \bullet {I_{LOAD}}^2 \quad (31)$$

The junction temperature of the MOSFET can be calculated from:

$$T_J = T_A + (P_{DISS} \bullet \theta_{JA}) \quad (32)$$

Where T_A is the ambient temperature and θJA is the MOSFET's thermal resistance from junction to ambient. If the device is on a heatsink, then the following equation:

$$\theta_{JA} + \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (33)$$

Where θ_{JC} is the MOSFET's thermal resistance from junction to case, θCS is the thermal resistance from case to sink, and θ_{SA} is the thermal resistance of the heatsink to ambient.

The calculated T_J must be lower than the MOSFET's maximum junction temperature rating, therefore:

$$\theta_{JA} < \frac{T_J(\text{max}) - T_A}{P_{DISS}} \quad (34)$$

APPLICATION INFORMATION

Transient Thermal Impedance

During a fault condition in the retry mode, the average MOSFET power dissipation will generally be quite low due to the low duty cycle, as defined by:

$$P_{DISS}(avg) = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}} \text{ (w/output shorted)} \quad (35)$$

(In the latch mode, t_{OFF} will be the time between a fault and the time the device is reset.)

However, the pulse power in the MOSFET during t_{ON}, with the output shorted, is:

$$P_{DISS}(pulse) = I_{MAX} \bullet V_{IN} \text{ (w/output shorted)} \quad (36)$$

In choosing t_{ON} for a given V_{IN}, I_{MAX}, and duty cycle it is important to consult the manufacturer's transient thermal impedance curves for the MOSFET to make sure the device is within its safe operating area. These curves provide the user with the effective thermal impedance of the device for a given time duration pulse and duty cycle. Note that some of the impedance curves are normalized to one, in which case the transient impedance values must be multiplied by the DC (steady state) thermal resistance, θ_{JC}.

For duty cycles not shown in the manufacturer's curves, the transient thermal impedance for any duty cycle and ton time (given a square pulse) can be estimated from [1]:

$$\theta_{JC}(trans) = (D \bullet \theta_{JC}) + (1 - D) \bullet \theta_{SP} \quad (37)$$

where D is the duty cycle: $\frac{t_{ON}}{t_{ON} + t_{OFF}}$.

and θ_{SP} is the single pulse thermal impedance given in the transient thermal impedance curves for the time duration of interest (t_{ON}). Note that these are absolute numbers, not normalized. If the given single pulse impedance is normalized, it must first be multiplied by θ_{JC} before using in the equation above.

This effective transient thermal impedance, when multiplied by the pulse power, will give the transient temperature rise of the die. To keep the junction temperature below the maximum rating, the following must be true:

$$\theta_{JC}(trans) = \frac{T_J(\max) - T_C}{P_{DISS}(pulse)} \quad (38)$$

If necessary, the junction temperature rise can be reduced by reducing ton (using a smaller value for C_T), or by reducing the duty cycle using the power limiting feature already discussed. Note that in either case, the amount of load capacitance, C_{OUT}, that can be charged before causing a fault, will also be reduced.

Safety Recommendations

Although the UCC3919 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. for this reason, if the UCC3919 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3919 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

References

[1] International Rectifier, HEXFET Power MOSFET Designer's Manual, Application Note 949B, *Current Ratings, Safe Operating Area, and High Frequency Switching Performance of Power HEXFETs,* pp.1553-1565, September 1993.

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Latchable Negative Floating Hot Swap Power Manager

FEATURES

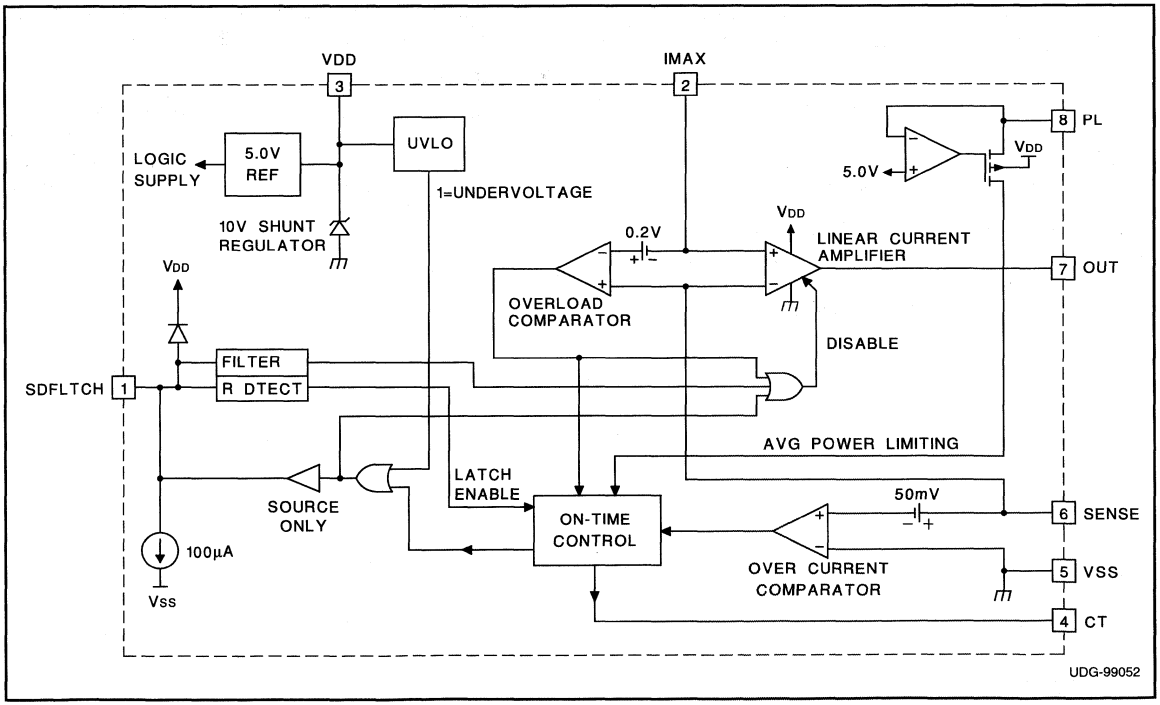
- Precision Fault Threshold
- Programmable: Average Power Limiting, Linear Current Control, Overcurrent Limit and Fault Time
- Fault Output Indication Signal
- Automatic Retry Mode or Latched Operation Mode
- Shutdown Control
- Undervoltage Lockout
- 250µs Glitch Filter on the SDFLTCH pin
- 8-Pin DIL and SOIC

DESCRIPTION

The UCC3921 family of negative floating hot swap power managers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is powered through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The onboard 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, selection of Retry or Latched mode, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on time from less than 0.1% to a maximum of 3% duty cycle. The duty cycle modulation depends on the current into PL, which is a function of the voltage across the FET, thus limiting average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

dropout. The fault current level is set with an external current sense resistor, while the maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on IMAX. The current level, when the output acts as a current source, is equal to VIMAX/RSENSE. If desired, a controlled current start up can be programmed with a capacitor on IMAX.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later (provided that the selected mode of operation is Automatic Retry Mode). When the output current reaches the maximum sourcing current level, the output acts as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC3921 include undervoltage lockout, 8-pin Small Outline (SOIC) and Dual-In-Line (DIL) packages, and a Latched Operation Mode option, in which the output is latched off once CT charges to 2.5V and stays off until either SDFLTCH is toggled (for greater than 1ms) or the IC is powered down and then back up.

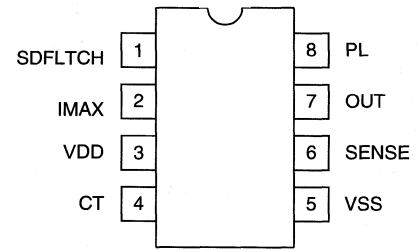
ABSOLUTE MAXIMUM RATINGS

IVDD 50mA
SDFLTCH Current 10mA
PL Current 10mA
IMAX Input Voltage . . . . . VDD
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to V_{SS} (the most negative voltage). Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8 , SOIC-8 (Top View)
N or J, D Packages



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ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; I_{VDD} = 2mA, C_T = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1	2	mA
Regulator Voltage	I_{SOURCE} = 2mA	9	9.5	10.0	V
	I_{SOURCE} = 10mA	9.15	9.6	10.15	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C	47.5	50	53.5	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1V, I_{PL} = 0	–50	–36	–22	µA
	Overload Condition, V_{SENSE} - V_{IMAX} = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	V_{CT} = 1V, I_{PL} = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.45	2.6	V
CT Reset Threshold		0.41	0.49	0.57	V
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; I_{VDD} = 2mA, C_T = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output High Voltage	I_{OUT} = 0mA	8.5	10		V
	I_{OUT} = –1mA	6	8		V
Output Low Voltage	I_{OUT} = 0mA, $V_{SENSE} - V_{IMAX}$ = 100mV		0	10	mV
	I_{OUT} = 2mA, $V_{SENSE} - V_{IMAX}$ = 100mV		200	600	mV
Linear Amplifier Section					
Sense Control Voltage	V_{IMAX} = 100mV	85	100	115	mV
	V_{IMAX} = 400mV	370	400	430	mV
Input Bias			50	500	nA
Power Limiting Section					
VSENSE Regulator Voltage	I_{PL} = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	I_{PL} = 64µA	0.6	1.2	1.7	%
	I_{PL} = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	Note 1		300	500	ns
Output Sink Current	$V_{SENSE} - V_{IMAX}$ = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV
Shutdown/Fault/Latch Section					
Shutdown Threshold		3	5	VDD+1	V
Input Current	$V_{SDFLTCH}$ = 5V	50	110	250	µA
Filter Delay Time (Delay to Output)		250	500	1000	µs
Fault Output High		6	9.5		V
	$I_{SDFLTCH}$ = –100µA	5	8.5		V
Fault Output Low			0	10	mV
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%
	$I_{SDFLTCH}$ = –100µA, Fault Condition, I_{PL} = 0			0	%

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the fault time. The fault time must be longer than the time to charge external load capacitance. The fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}}$$

where ICH = 36µA + IPL, and IPL is the current into the power limit pin. Once the maximum fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 2 \bullet 10^6 \bullet C_T$$

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for IMAX. The current level at which the output appears as a current source is equal to the voltage on IMAX over the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on IMAX, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: This pin provides gate output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When IPL>>36µA, then the average MOSFET power dissipation is given by:

$$P_{MOSFET}avg = IMAX \bullet 1 \bullet 10^{-6} \bullet R_{PL}$$

PIN DESCRIPTIONS (continued)

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and C_T starts to charge.

SDFLTCH: This pin provides fault output indication, shutdown control, and operating mode selection. Interface into and out of this pin is usually performed through level shift transistors. When open, and under a non-fault condition, this pin pulls to a low state with respect to VSS. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state with respect fo VSS, indicating the NMOS pass element is OFF. When > 250µA is sourced into this pin for > 1ms, it drives high causing the output to disable the NMOS pass device.

If an 5k < R_{LATCH} < 250kΩ resistor is placed from this pin to VSS, then the latched operating mode will be invoked. Upon the occurrence of a fault, under the latched mode of operation, once the C_T capacitor charges up to 2.5V the NMOS pass element latches off. A retry will not periodically occur. To reset the latched off device, either SDFLTCH is toggled high for a duration greater than 1ms or the IC is powered down and then up.

VDD: Current driven with a resistor to a voltage approximately 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD approximately 10V above VSS, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

APPLICATION INFORMATION

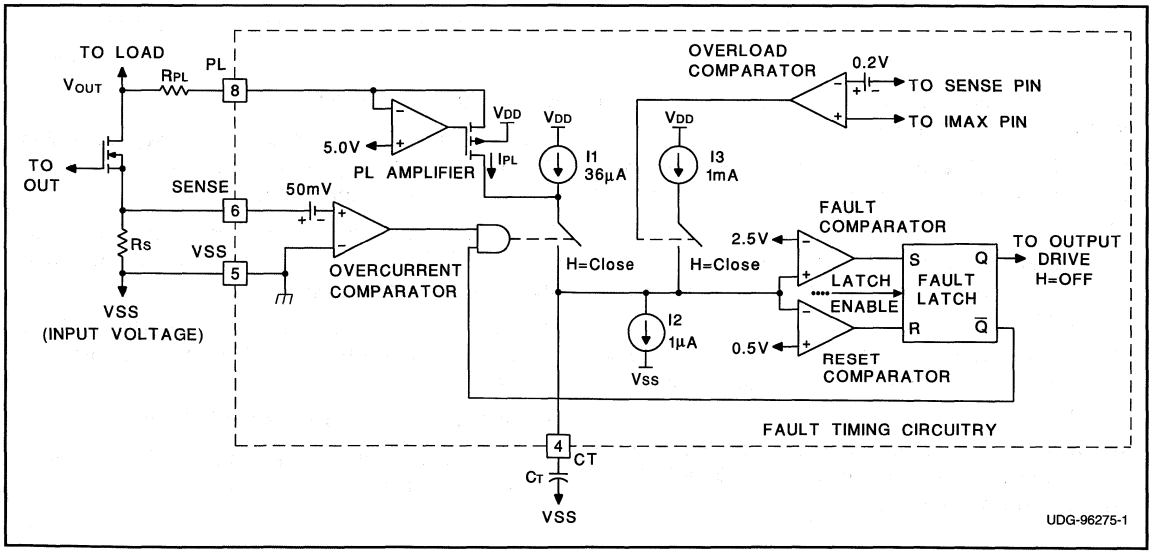


Figure 1. Fault Timing Circuitry for the UCC3921, Including Power Limit Overload

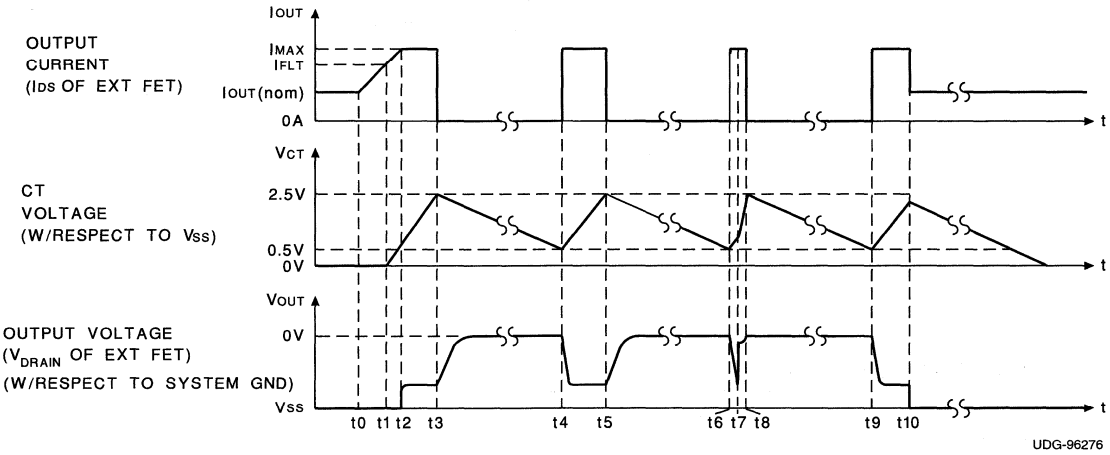
APPLICATION INFORMATION (continued)

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3921. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, Rs, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36μA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

where V_{FET} is the voltage across the NMOS pass device. Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, $V_{OUT} \approx$ VSS (input voltage), $I_{PL} = 0$, the CT charging current is 36μA.

During a fault, CT will charge at a rate determined by the



t0: Safe condition. Output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached. Output current rises above the programmed fault value, CT begins to charge at ~36μA.

t2: Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs. CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground.

t4: Retry. CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4: Retry. CT has discharged to 0.5V, but fault is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t7: Output short circuit. If VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.

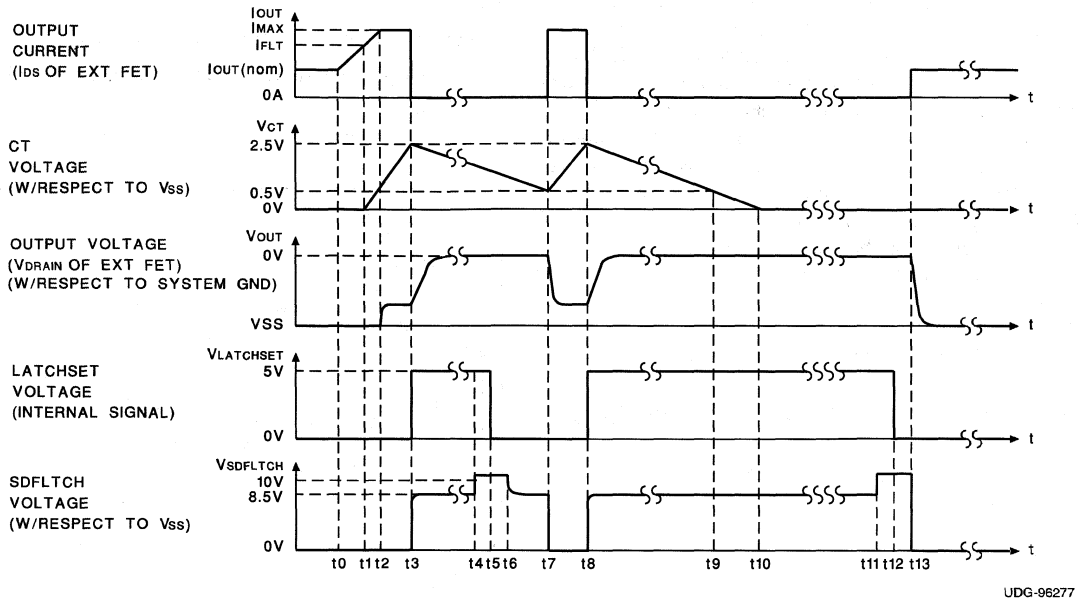
t8: Fault occurs. Output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition. Return to normal operation of the hot swap power manager.

Figure 2. Retry Operation Mode

APPLICATION INFORMATION (cont.)



t0: Safe condition. Output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached. Output current rises above the programmed fault value, CT begins to charge at ~36μA.

t2: Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs. CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage. The FET turns off allowing no output current to flow, V_{OUT} floats up to ground, and since there is an 82kΩ resistor from the SDFLTCH pin to VSS, the internal latchset signal goes high.

t4: Since the user does not want the chip to LATCH off during this cycle, he toggles SDFLTCH high for greater than 1ms {t6 - t4 > 1ms}.

t5: The latchset signal is reset.

t6: Forcing of SDFLTCH is released after having been applied for > 1ms.

t7: Retry (since the latchset signal has been reset to its' low state) - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t8 = t3: Fault occurs. CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground, and since there is an 82kΩ resistor from SDFLTCH to VSS, the internal latchset signal goes high.

t9: Output is latched off. Even though CT has discharged to 0.5V, there will not be a retry since the latchset signal was allowed to remain high.

t10: Output remains latched off. CT has discharged all the way to 0V.

t11: The output has been latched off for quite some time. The user now wishes to reset the latched off output, thus toggling SDFLTCH high for greater than 1ms {t13 - t11}.

t12 = t5: The latchset signal is reset.

t13: Forcing of SDFLTCH is released after having been applied for > 1ms. The fault had also been released during the time the output was latched off, safe condition, return to normal operation of the hot swap power manager.

Figure 3. Latched Operation Mode: R_{LATCH} = 82k

APPLICATION INFORMATION (continued)

internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to repeat. Under a constant fault, the duty cycle is given by:

$$Duty\ Cycle = \frac{1\mu A}{I_{PL} + 36\mu A}$$

Average power dissipation in the pass element is given by:

$$P_{FET_{AVG}} = V_{FET} \bullet I_{MAX} \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

Where V_{FET}>>5V I_{PL} can be approximated as:

$$\frac{V_{FET}}{R_{PL}}$$

and where I_{PL}>>36µA, the duty cycle can be approximated as :

$$\frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = V_{FET} \bullet I_{MAX} \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

$$= IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels, thereby limiting the average power dissipation in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC3921 ensures that the output NMOS does not pass more than I_{MAX} (which is V_{IMAX}/R_{SENSE}). In the event the output current exceeds the programmed I_{MAX} by 0.2V/R_{SENSE}, which can only occur if the output FET is not responding to a command from the IC, CT will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SDFLTCH pin, and also since the voltage on CT will continue charging past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build redundancy into the system.

Determining External Component Values

To set R_{VDD} (see Fig. 4) the following must be achieved:

$$\frac{V_{IN}\ min}{R_{VDD}} > \frac{10V}{R1 + R2} + 2mA$$

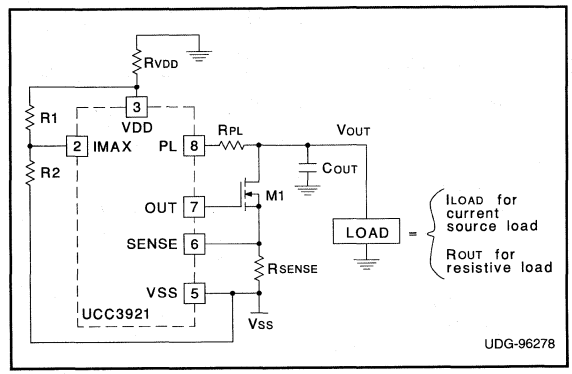


Figure 4.

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic in Figure 4 as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate C_{TMIN}. Now, given the values of C_{OUT}, Load, R_{SENSE}, V_{SS}, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for C_T to charge to 2.5V (relative to V_{SS}), and is the basis for estimating the minimum value of C_T. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

Next, the variable I_{MAX} must be calculated. I_{MAX} is the maximum current that the UCC3921 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value I_{MAX} where

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}}$$ where V_{IMAX} = voltage on pin IMAX.

Given this information, calculation of the startup time is now possible via the following:

APPLICATION INFORMATION (continued)

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |V_{SS}|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} =$$

$$C_{OUT} \bullet R_{OUT} \bullet \ell n\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |V_{SS}|}\right)$$

Once T_{START} is calculated, the power limit feature of the UCC3921 must be addressed and component values derived. Assuming the user chooses to limit the maximum

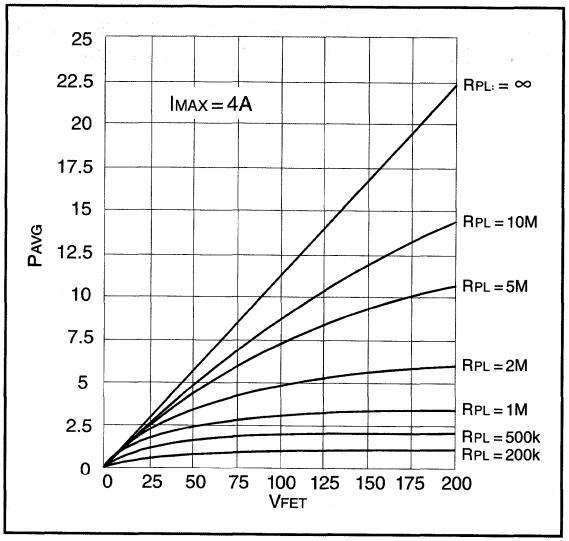


Figure 5. Plot Average Power vs FET Voltage for Increasing Values of R_{PL}

allowable average power that will be associated with the hot swap power manager, the power limiting resistor, R_{PL}, can be easily determined by the following:

$$R_{PL} = \frac{P_{FET\ avg}}{1\mu A \bullet I_{MAX}}$$ where a minimum R_{PL} exists

defined by $R_{PL}\ min = \frac{|V_{SS}|}{5mA}$ (Refer to Figure 5).

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_T\ min =$$

$$\frac{3 \bullet T_{START} \bullet (72\mu A \bullet R_{PL} + |V_{SS}| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_T\ min =$$

$$\frac{3 \bullet T_{START} \bullet (36\mu A \bullet R_{PL} + |V_{SS}| - 5V - I_{MAX} \bullet R_{OUT})}{5 \bullet R_{PL}}$$

$$+ \frac{3 \bullet R_{OUT} \bullet |V_{SS}| \bullet C_{OUT}}{5 \bullet R_{PL}}$$

Level Shift Circuitry to Interface with SDFLTCH

Some type of circuit is needed to interface with the UCC3921 via SDFLTCH, such as opto-couplers or level shift circuitry. Figure 6 depicts one implementation of level shift circuitry that could be used, showing component values selected for a typical –48V telecommunications application. There are three communication conditions which could occur; two of which are Hot Swap Power Manager (HSPM) state output indications, and the third being an External Shutdown.

1) When open, and under a non-fault condition, SDFLTCH is pulled to a low state. In Figure 6, the N-channel level shift transistor is off, and the FAULT OUT signal is pulled to LOCAL VDD through R3. This indicates that the HSPM is not faulted.

2) When a fault is detected by the fault timer or undervoltage lockout, this pin will drive to a high state, indicating that the external power FET is off. In Figure 6, the N-channel level shift transistor will conduct, and the FAULT OUT signal will be pulled to a Schottky Diode voltage drop below LOCAL GND. This indi-

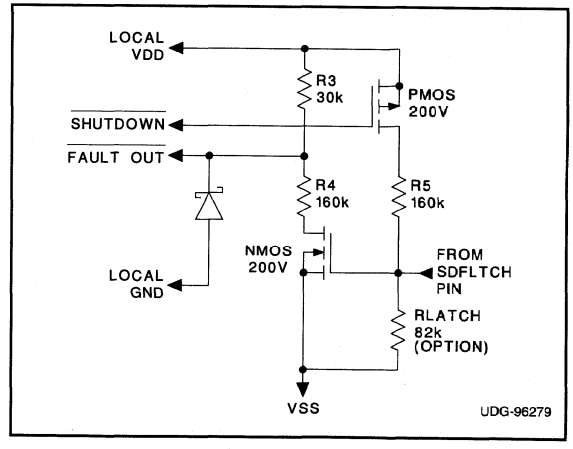


Figure 6. Possible Level Shift Circuitry to Interface to the UCC3921, showing component values selected for a typical telecom application.

APPLICATION INFORMATION (continued)

cates that the HSPM is faulted. The Schottky Diode is necessary to ensure that the FAULT OUT signal does not traverse too far below LOCAL GND, making fault detection difficult.

If a 5k < R_{LATCH} < 250kΩ resistor is tied between SDFLTCH & VSS, as optionally shown in Figure 6, then the latched operating mode (described earlier) will be invoked upon the occurrence of a fault.

3) To externally shutdown the HSPM, the $\overline{\text{SHUTDOWN}}$ signal (typically held at LOCAL VDD) must be pulled to LOCAL GND. Assuming $\overline{\text{SHUTDOWN}}$ is tied to LOCAL GND, the P-channel level shift transistor will conduct, driving SDFLTCH high (to roughly VDD plus a diode). By sourcing > 250µA into SDFLTCH for > 1ms the output to the external power FET will be disabled. The current sourced into SDFLTCH must be limited to 10mA or less: $I_{SDFLTCHMAX}$ < 10mA.

SAFETY RECOMMENDATIONS

Although the UCC3921 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3921 is intended for use in safety critical applications where UL® or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the external power FET. The UCC3921 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

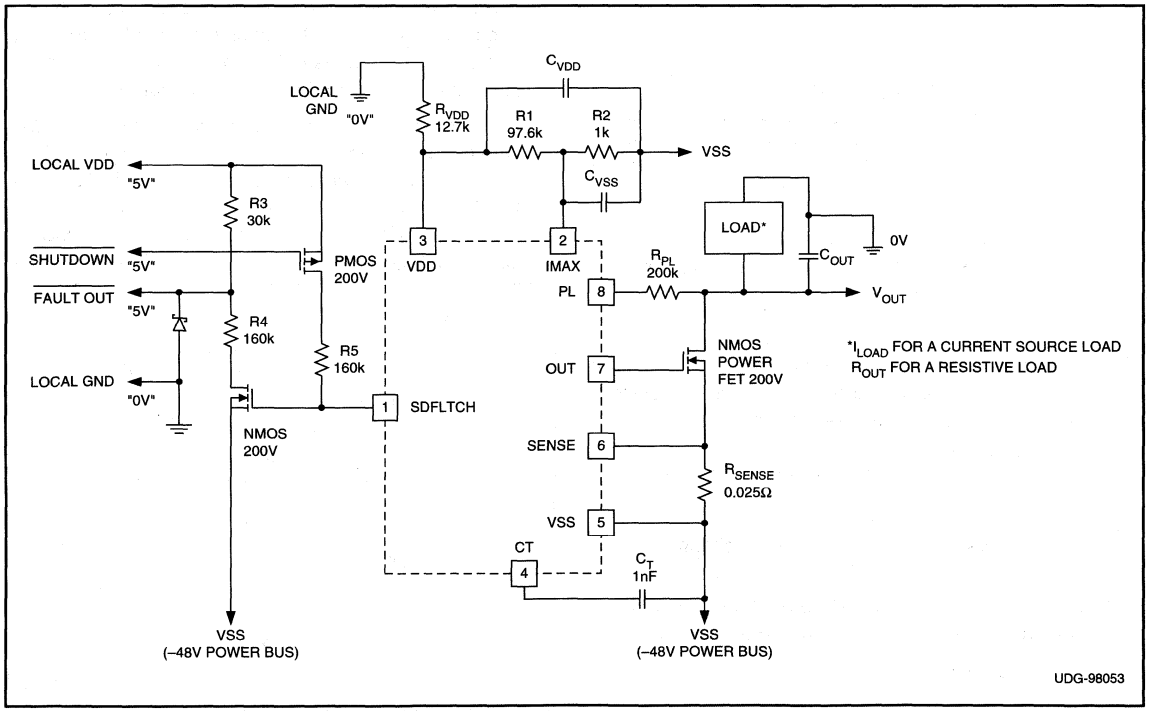


Figure 7. Typical Telecommuications Application

(The "Negative Magnitude-Side" of the Supply is Switched in)

APPLICATION INFORMATION (continued)

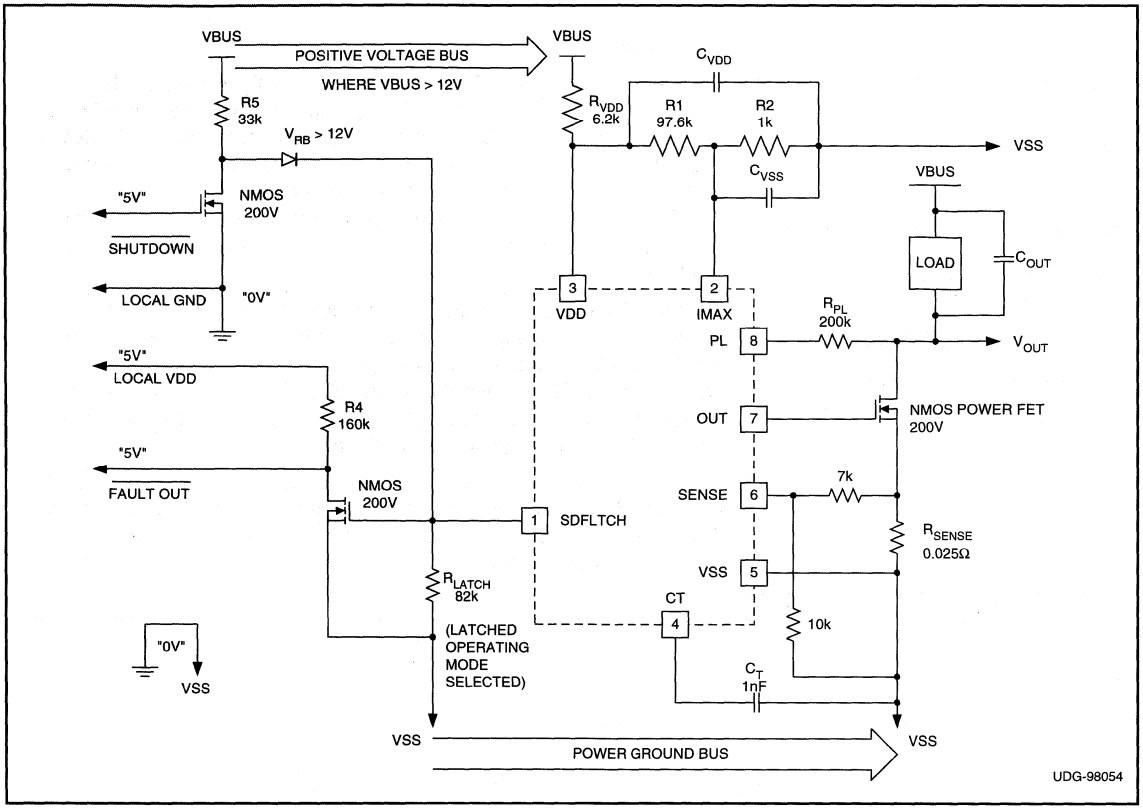


Figure 8. Floating Positive Application

The "Ground-side" of the Supply is Switched In

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Universal Serial Bus Hot Swap Power Controller

FEATURES

- Fully USB Compliant
- Support Four 5V Peripherals and One USB 3.3V Controller
- Separate Power Enables
- 500mA Current Limiting per Channel
- Separate Open Drain Fault Indicator for Each Channel
- 3.3V Output for USB Controller
- Available in 28 Pin Wide Surface Mount and DIP

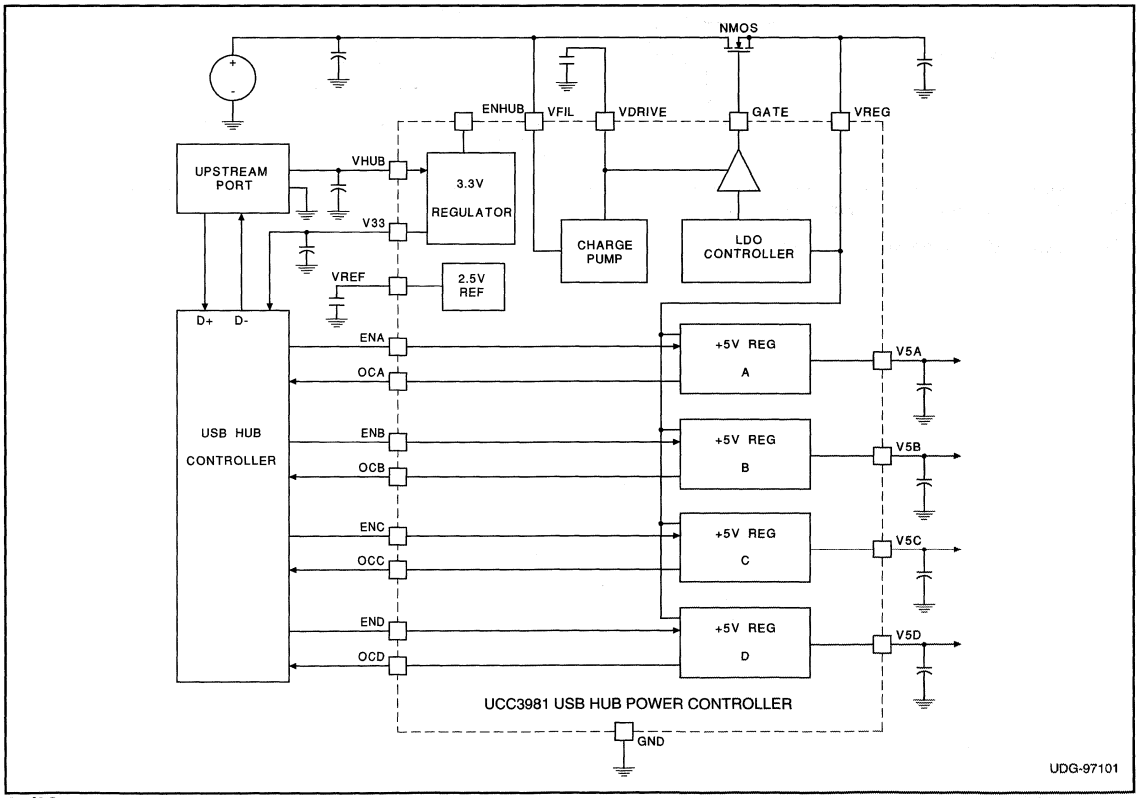
DESCRIPTION

The UCC3981 Hot Swap Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage and four 5V regulated voltages for USB ports. Each of the 5V output ports is individually enabled for optimal port control. Each port also provides an overcurrent fault signal indicating that the port has exceeded a 500mA current limit. The 3.3V linear regulator is used to power the local USB microcontroller. This regulator is protected with a 100mA current limit and has a logic level enable input.

The UCC3981 can be configured to provide USB port power from a loosely regulated voltage such as a Filament voltage internal to a monitor. Pre-regulation is provided by an internal linear regulator controller and one external logic level N-channel MOSFET. The UCC3981 can also be configured without using the pre-regulator stage by connecting the VREG pins to a regulated 5.5V 2A source.

The UCC3981 comes in a 28-pin wide SOIC power package optimized for power dissipation, and is protected by internal over-temperature shutdown mechanism, which disables the outputs should the internal junction temperature exceed 150°C.

APPLICATION AND BLOCK DIAGRAM



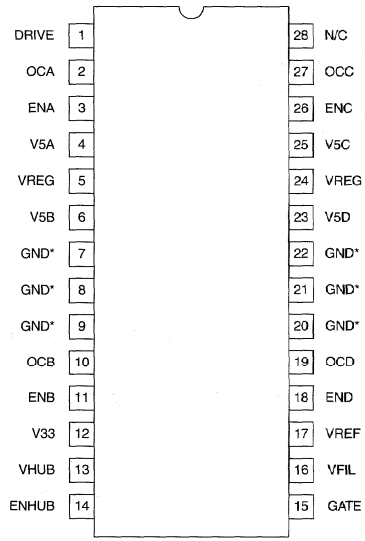
ABSOLUTE MAXIMUM RATINGS

VFIL 9V
VCON Supply Votage 9V
Logic Inputs (ENA-D, ENHUB)
  Maximum Forced Voltage . . . . . –0.3V to 7V
  Maximum Forced Current . . . . . ±1mA
V33
  Maximum Forced Voltage 5V
  Maximum Current 200mA
V5A-D
  Maximum Voltage 9V
  Maximum Current 750mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; Pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 0°C to 125°C for the UCC3981. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Currents					
VHUB Supply Current	No External Load on V33		1	3	mA
VFIL Supply Current			1	3	mA
Reference					
VREF Voltage	Over Temperature	2.35	2.5	2.65	V
Line Regulation	VHUB = 4.5V to 9V		3	10	mV
3.3V Regulator					
V33 Voltage	T_J = 25°C, I_{LOAD} = 10mA	3.2	3.3	3.4	V
	0mA to 100mA, 0°C to 125°C, VHUB = 4.5V to 9V	3.165	3.3	3.435	V
Short Circuit Current Limit	VHUB = 6V, Output shorted to Ground	100	120	150	mA
Pre-Regulator					
VREG Voltage	0A to 2A, 0°C to 125°C, VFIL = 6V to 9V	5.25	5.5	5.7	V
5V Regulator					
V5A-D Voltage	T_J = 25°C, I_{LOAD} = 250mA, V_{REG} = 5.5V	4.85	5	5.15	V
	0mA to 500mA, 0°C to 125°C	4.8	5	5.2	V
Short Circuit Current Limit	VREG = 5.5V, Output Shorted to Ground	500	600	750	mA
Charge Pump					
Quiescent Output Voltage	T_J = 25°C, VFIL = 6V, ENA-D = 5V, ENHUB = 5V	11	11.45	12	V
	0°C to 125°C, VFIL = 6V	10.5	11.45	12	V
Output Impedance			9	15	kΩ

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_J = 0°C to 125°C for the UCC3981. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Inputs					
ENA-D Inputs - Guaranteed Low				0.7	V
ENA-D Inputs - Guaranteed High		3			V
ENHUB Input - Guaranteed Low				0.7	V
ENHUB Input - Guaranteed High		3			V
Overcurrent Signals					
Active Sink Current	locx =100µA		140	500	mV

PIN DESCRIPTIONS

ENA-D: Separate enables pins for each of the four 5V supplies.

ENHUB: Enables the 3.3V output V33. Pulling this pin low disables V33.

GATE: Gate drive for an external NMOS used to regulate the 5.5V VREG supply. Minimum available drive is 11V.

GND: All 6 GND pins must be tied to the system ground. In addition to serving as electrical conductors, these 6 pins are heat sinks. Refer to the Packaging Device Temperature Management guide in the Packaging section of the Unitrode Databook.

OCA-D: Open drain overcurrent indicator. OCA-D can be wire OR'ed by the user to create a single overcurrent indicator.

V5A-D: 5V regulated output with enable, 500mA (minimum) current limit, and overcurrent indicator.

V33: 3.3V regulator output. Enable when ENHUB is high. Current limit is 100mA minimum.

VDRIVE: Internal charge pump voltage is brought out for external decoupling. Nominal voltage is between 11V and 13V. No external loading permitting. Decouple with at least 0.001µF capacitor.

VFIL: Bias supply for all four of the 5V regulators. VFIL voltage must be between 6V and 9V.

VHUB: Supply for the 3.3V USB controller power supply and bandgap reference.

VREF: Internal 2.5V reference is brought out for external decoupling only. Decouple with 0.01µF capacitor.

VREG: Regulated to 5.5V by means of an external NMOS. Two pins supply up to a total of 2.5A to the four 5V bus voltages (V5A, V5B, V5C, V5D).

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TEL. (603) 424-2410 • FAX (603) 424-3460

Universal Serial Bus Hot Swap Power Controller

FEATURES

- Support Four 5V Peripherals and One USB 3.3V Controller
- Separate Power Enables
- 650mA Current Limiting per Channel
- Separate Open Drain Fault Indicator for Each Channel
- 3.3V Output for USB Controller
- Available in 20 Pin DIP

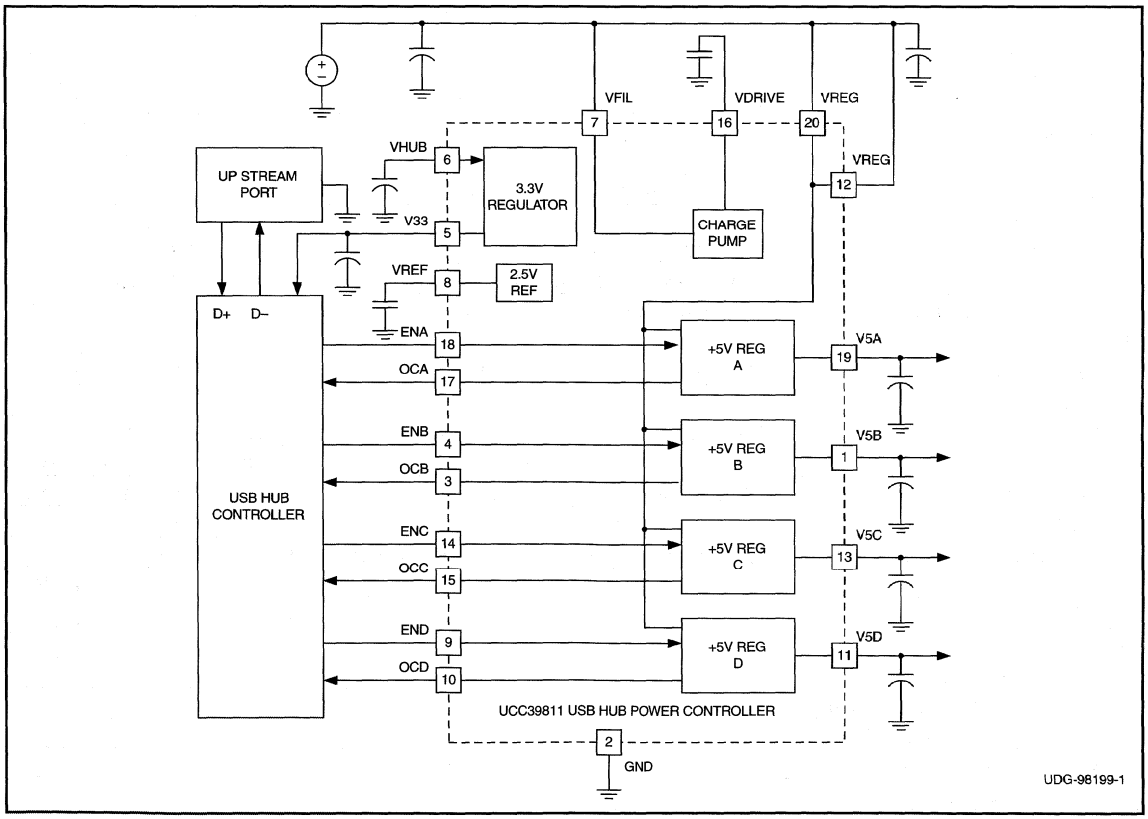
DESCRIPTION

The UCC39811 Hot Swap Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage and four 5V regulated voltages for USB ports. Each of the 5V output ports is individually enabled for optimal port control. Each port also provides an overcurrent fault signal indicating that the port has exceeded a 650mA current limit. The 3.3V linear regulator is used to power the local USB microcontroller. This regulator is protected with a 100mA current limit and has a logic level enable input.

The UCC39811 can be configured to provide USB port power from a loosely regulated voltage such as a Filament voltage internal to a monitor. Pre-regulation is provided by an internal linear regulator controller and one external logic level N-channel MOSFET. The UCC39811 can also be configured without using the pre-regulator stage by connecting the VREG pins to a regulated 5.5V 2A source.

The UCC39811 comes in a 20-pin DIP package and is protected by internal over-temperature shutdown mechanism, which disables the outputs should the internal junction temperature exceed 150°C.

APPLICATION AND BLOCK DIAGRAM



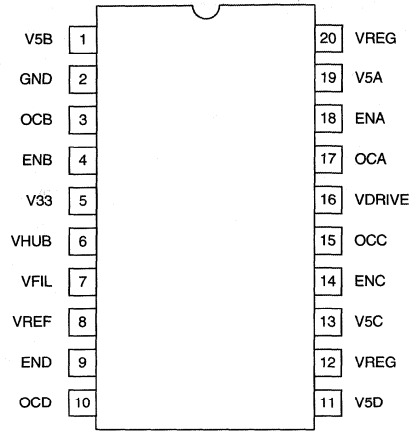
ABSOLUTE MAXIMUM RATINGS

VFIL 9V
VHUB Supply Voltage 9V
Logic Inputs (ENA-D, ENHUB)
  Maximum Forced Voltage . . . . . –0.3V to 7V
  Maximum Forced Current 1mA
V33
  Maximum Forced Voltage 5V
  Maximum Current 200mA
V5A-D
  Maximum Voltage 9V
  Maximum Current 900mA
Storage Temperature . . . . . 65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIP 20 (Top View)
N Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 0°C to 125°C for the UCC39811. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Currents					
VHUB Supply Current	No External Load on V33		1	3	mA
VFIL Supply Current			1	3	mA
Reference					
VREF Voltage	Over Temperature	2.35	2.5	2.65	V
Line Regulation	VHUB = 4.5V to 9V		3	10	mV
3.3V Regulator					
V33 Voltage	T_J = 25°C, I_{LOAD} = 10mA	3.2	3.3	3.4	V
	0mA to 100mA, 0°C to 125°C, VHUB = 4.5V to 9V	3.165	3.3	3.435	V
Short Circuit Current Limit	VHUB = 6V, Output shorted to Ground	100	120	150	mA
Pre-Regulator					
VREG Voltage	0A to 2A, 0°C to 125°C, VFIL = 6V to 9V	5.25	5.5	5.7	V
5V Regulator					
V5A-D Voltage	T_J = 25°C, I_{LOAD} = 250mA, V_{REG} = 5.5V	4.85	5	5.15	V
	0mA to 500mA, 0°C to 125°C	4.8	5	5.2	V
Short Circuit Current Limit	VREG = 5.5V, Output Shorted to Ground	650	750	900	mA
Charge Pump					
Quiescent Output Voltage	T_J = 25°C, VFIL = 6V, ENA-D = 5V, ENHUB = 5V	11	11.45	12	V
	0°C to 125°C, VFIL = 6V	10.5	11.45	12	V
Output Impedance			9	15	k
Enable Inputs					
ENA-D Inputs - Guaranteed Low				0.7	V
ENA-D Inputs - Guaranteed High		3			V
ENHUB Input - Guaranteed Low				0.7	V
ENHUB Input - Guaranteed High		3			V
Overcurrent Signals					
Active Sink Current	I_{OCX} =100µA		140	500	mV

PIN DESCRIPTIONS

ENA-D: Separate enables pins for each of the four 5V supplies.

ENHUB: Enables the 3.3V output V33. Pulling this pin low disables V33.

GATE: Gate drive for an external NMOS used to regulate the 5.5V VREG supply. Minimum available drive is 11V.

GND: All 6 GND pins must be tied to the system ground. In addition to serving as electrical conductors, these 6 pins are heat sinks. Refer to the Packaging Device Temperature Management guide in the Packaging section of the Unitrode Databook.

OCA-D: Open drain overcurrent indicator. OCA-D can be wire OR'ed by the user to create a single overcurrent indicator.

V5A-D: 5V regulated output with enable, 500mA (minimum) current limit, and overcurrent indicator.

V33: 3.3V regulator output. Enable when ENHUB is high. Current limit is 100mA minimum.

VDRIVE: Internal charge pump voltage is brought out for external decoupling. Nominal voltage is between 11V and 13V. No external loading permitting. Decouple with at least 0.001µF capacitor.

VFIL: Bias supply for all four of the 5V regulators. VFIL voltage must be between 5.5V and 9V Can be tied to VRE.

VHUB: Supply for the 3.3V USB controller power supply and bandgap reference.

VREF: Internal 2.5V reference is brought out for external decoupling only. Decouple with 0.01µF capacitor.

VREG: Regulated to 5.5V by means of an external NMOS. Two pins supply up to a total of 2.5A to the four 5V bus voltages (V5A, V5B, V5C, V5D).

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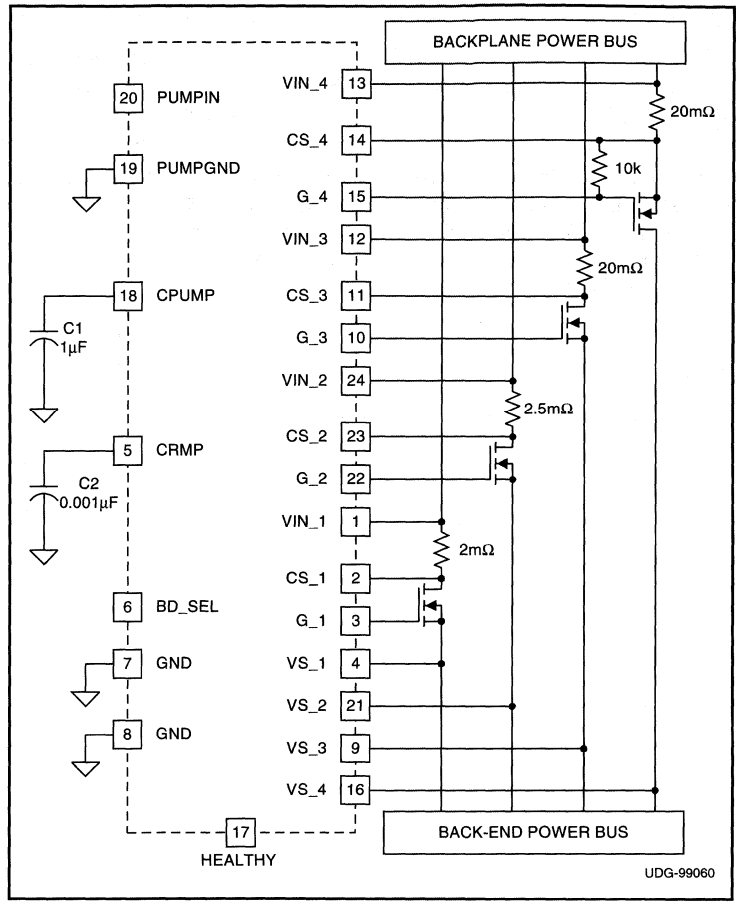
Programmable CompactPCI™ Hot Swap Manager

FEATURES

- Fully CompactPCI™ compliant
- Features and ranges programmable using internal non-volatile memory
- Four Channels for individual control of 4 supplies
- Minimal external parts count
- Precise Linear Current Amplifier for controlled current ramping
- True ramp-up and ramp-down current slew control
- Precision 2X over-current detection
- High voltage charge pump permits design with lower cost external NFET devices
- Shutdown control with low sleep mode quiescent current
- Input under-voltage lockout (UVLO)
- Wide input operating range: –15V to 15V
- Easily programmable for other applications
- Windows 95/98 programming interface and utilities
- 24 Pin SOIC and TSSOP package

TYPICAL APPLICATION



DESCRIPTION

The UCC3985 family of Compact PCI Hot Swap Power Managers (HSPM) provides fully programmable supply management using an absolute minimum of external support components. The UCC3985 provides full management of 3 positive supplies and 1 negative power rail. The UCC3985 is the first HSPM to offer on-chip non-volatile memory, which allows the user to customize the performance of the part to the application. This feature enables interactive programming during the circuit development phase, leading to rapid product deployment. Programming during development is supported with an easy to use PC parallel port interface and a Windows 95/98 based Graphical User Interface (GUI). UCC3985 high volume delivery can be pre-programmed to the customer requirements at the factory. The programmable features of the UCC3985 include:

- Independent Linear Current Limit and Under-voltage detection
- Supply sequencing order
- Fault event behavior
- Common Voltage fault filter time

Like other Unitrode Hot Swap Power Managers the UCC3985 utilizes a Linear Current Amplifier (LCA) in each of its 4 channels to provide closed loop control of the inrush current profile during start-up. The LCA concept allows the designer to program the startup current slew rate and steady state level. The <lmV input offset voltage of the LCA allows for low value sense resistors, minimizing insertion loss across the hot swap interface, while not compromising performance in low current appli-

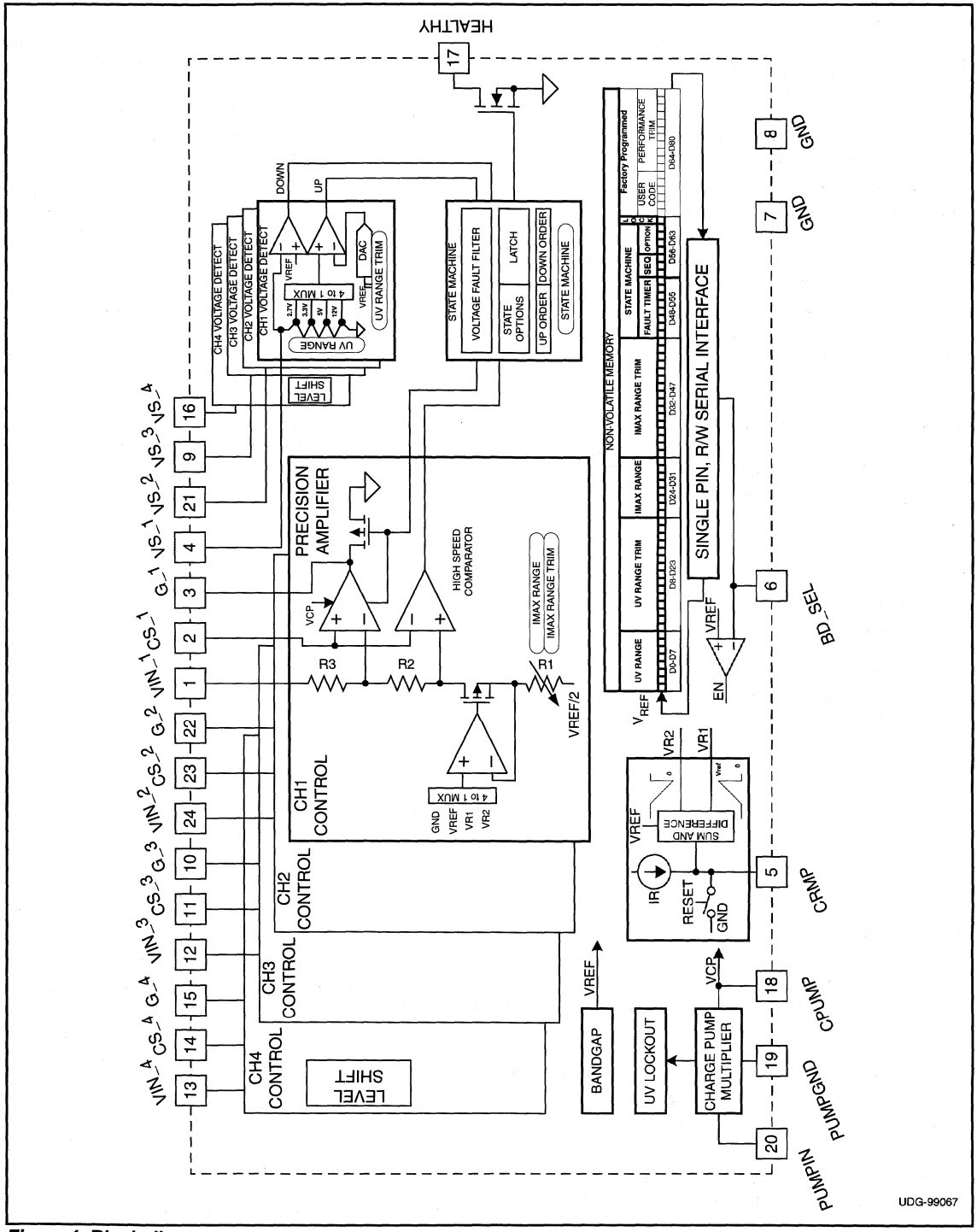


Figure 1. Block diagram.

DESCRIPTION (cont.)

cations. Current limit range and fine adjust for each channel are fully programmable to allow for an easy match of desired current limit and standard, low value, current sense resistors. Low input offset and set-point voltages make board copper trace resistors feasible for high current applications.

A versatile programmable state machine defines how the supplies are sequenced and how the device responds to a fault or over-current condition. A programmable Voltage Fault Delay Filter can be set to enable compatibility with the longer voltage ramps associated with large bus filter capacitance. To protect the host system power bus, the UCC3985 can provide fault protection in the form of an electronic circuit breaker with a programmable over-current threshold set to precisely 2 times the programmed current limit value. Detection of an over-current condition on any rail(s) can be set to cause the corresponding external N-channel MOSFET(s) device(s) to be latched off immediately with the remaining supplies being ramped down per the pre-programmed schedule.

The UCC3985 is designed to work with supplies ranging from –15V to +15V. A 24V onboard charge pump multiplier ensures maximum external N-channel MOSFET gate overdrive offering the use of lower cost devices for the equivalent insertion loss. A separate PUMPIN pin allows for pump connection to the highest input supply for maximum pump efficiency.

The UCC3985 is available in 24 pin SOIC (DW) and 24 pin TSSOP packages.

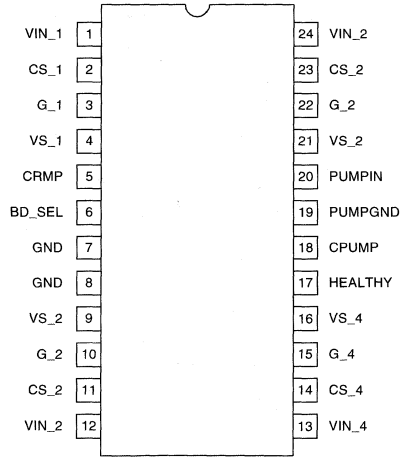
ABSOLUTE MAXIMUM RATINGS

VIN_1, VIN_2, VIN_3 . . . . . 0.3V to 15V
VS_1, VS_2, VS_3. . . . . –0.3 to VIN (corresponding channel)
CS_1, CS_2, CS_3 . . . . . –0.3 to VIN (corresponding channel)
VIN_4,VS_4. . . . . –15 to 0.3V
BD_SEL. . . . . –0.3 to 20V
PUMPIN. . . . . –0.3 to 15V
HEALTHY . . . . . –0.3 to 12V
Storage Temperature . . . . . –65°C to 150°C
Junction Temperature. . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAM

SOIC-24 or TSSOP-24 (Top View)
DW Package



PIN DESCRIPTIONS

BD_SEL: A logic low on this pin enables the UCC3985 to supply power to the Back-End Bus. The logic threshold for this pin is 1.5 Volts. When disabled, the UCC3985 enters a low current sleep mode. This pin also serves as the input to the UCC3985 serial interface to read and write memory data. This unique interface employs multi-threshold voltage/current mode methods to enable simultaneous Data In, Data Out and Clock on a single pin.

CRMP: A capacitor tied to this pin sets the linear ramp up/down of the LCA current limit for each supply during supply sequencing.

CS_1, CS_2, CS_3: These pins tie to the low end of the external current sense resistor and are used along with the VIN_1-3 pins as the input to the LCA.

CS_4: This pin ties to the more positive end of the current sense resistor of the negative supply rail. It is used with VIN_4 as the input to the LCA.

G_1, G_2, G_3: The Gate drive for the external NFETs for the positive rail switches. The gate drive is controlled as a function of sequencing and current to a value between 0 and 24 volts. The LCA is internally compensated and guaranteed stable for a wide range of gate capacitance.

PIN DESCRIPTIONS

G_4: Gate drive for the negative rail switch. This pin is driven in response to sequencing and load current to a voltage between VIN_4 and ground. An external pull-down resistor should be used between G_4 and CS_4.

GND: Analog grounds for the device.

HEALTHY: In the *CompactPCI*™ application, this pin is driven low to indicate the board's suitability to be connected to the bus. This is an open drain output which is driven false if the Back End power is not within the tolerances programmed into the under-voltage comparators, the result of an over-current on either supply controller or a fault time-out on either supply during linear ramp-up.

PUMPC: Charge Pump output. A 1µF capacitor should be connected from this pin to ground. This capacitor provides charge storage to drive the gate of the external NFET device for each channel.

PUMPGND: Ground for internal charge pump multiplier.

PUMPIN: This is the input to the charge pump multiplier. It should be connected to the highest input supply voltage to ensure sufficient gate overdrive for the NFET of the highest supply rail. It is recommended to place a 0.1µF de-coupling capacitor from this pin to PUMPGND to minimize board level noise due to internal charge pump switching.

VIN_1, VIN_2, VIN_3: These pins tie to the positive backplane supplies.

VIN_4: This pin ties to the negative backplane supply.

VS_1, VS_2, VS_3: These are the voltage sense pins for the positive Back-End power bus.

VS_4: This is the voltage sense pin for the negative Back-End power bus.

APPLICATION INFORMATION

Programmability:

The UCC3985 has 64 bits of user settable non-volatile memory. These bits are programmed through the BD_SEL pin and the self-clocking, multilevel, read-able and writ-able serial interface of the UCC3985. The UCC3985 PC Parallel Port Interface Kit and Windows 95/98 Drivers provides the user with a quick and easy means to customize the UCC3985 to the specific application. A "LOCK" bit can be set to disable the serial interface and prevent any future modification of memory contents. Once the customization is developed, high volume delivery can be fully preprogrammed at the factory.

Non-Volatile Memory Bits:

D0-D7, UV RANGE: These bits (2 per channel) set the coarse range of the under-voltage detection comparators. The positive and negative supplies can be individually set to 2.7V, 3.3V, 5.0V or 12V. The "UP" and "DOWN" comparison information is used to detect an output fault or to determine the completion of an individual supply ramp sequence.

D8-D23, UV RANGE TRIM: These bit positions provide additional resolution in the trim of the UV RANGE of each channel.

D24-D31, IMAX RANGE: The coarse range of the IMAX current limit can be set with 2 bits of resolution per channel. These bits allow a range adjustment of the equivalent voltage drop across the external current sense resistor while in closed loop linear current control. This value can be set from 10mV to 80mV.

D32-D47, IMAX RANGE TRIM: The current limit range set by IMAX RANGE can be fine tuned with an additional 4 bits of resolution per channel with these bits.

D48-D62, STATE MACHINE: Bits 48-55 set the amount of time that the UCC3985 is allowed to operate in the constant current mode during supply sequencing. This time can be set from 0 and 150 mSec and is common to all 4 channels. Bits 56-58 set the supply up/down sequence. Bits 59-63 determine how the state machine responds to a fault condition.

D63, LOCK: Once set, this bit permanently disables the serial interface and disconnects it from the BD_SEL pin, preventing any further change of memory contents.

D64-D80, FACTORY PRETRIM: These readable positions are permanently written at the factory. They contain customer specific and product version information as well as parametric pre-trim information.

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ADVANCE INFORMATION

Simple Single Channel External N-FET Hot Swap Manager

FEATURES

- Precise Linear Current Amplifier for precision inrush current profile programming
- Programmable over-current detection threshold
- Internal Charge Pump for control of external NMOS devices
- Shutdown Control with low sleep mode quiescent current
- Input undervoltage lockout (UVLO)
- Input operating range: 2.75V to 5.5V
- Simple 8-pin part

DESCRIPTION

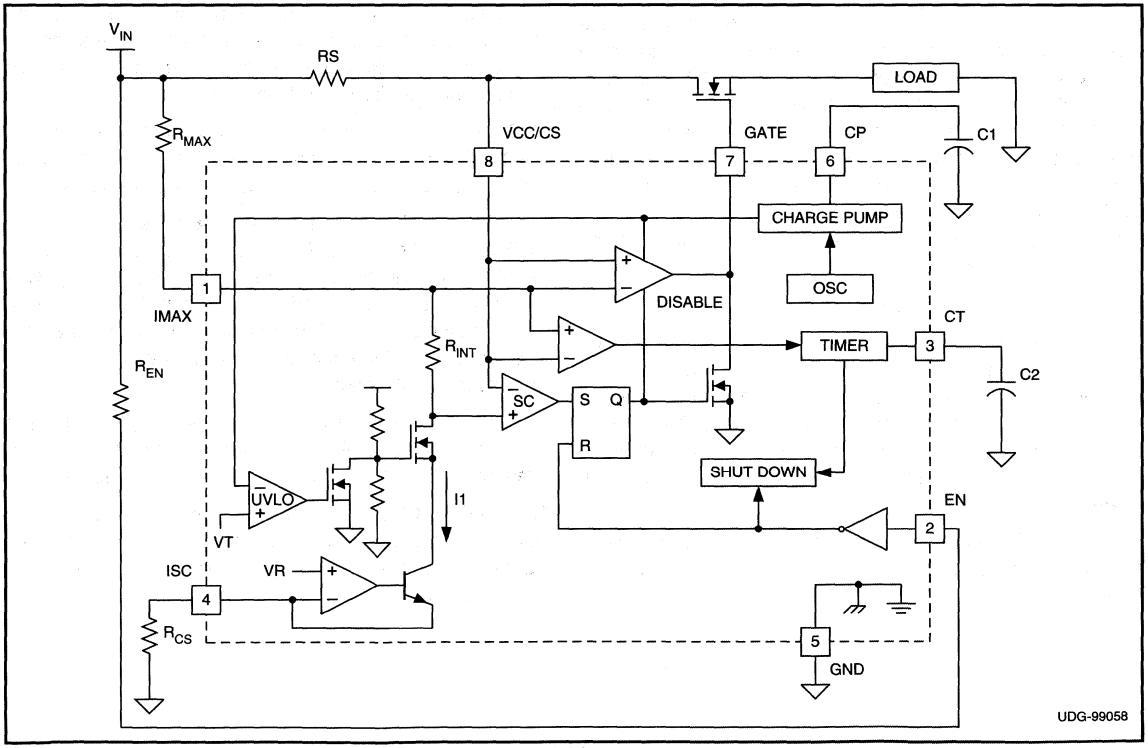
The UCC3995 family of Hot Swap Power Managers provides the most functions available in the industry in a simple 8 pin package requiring minimal external parts count. The UCC3995 needs few external components to operate, producing the lowest total system cost.

Like other Unitrode Hot Swap Power Managers (HSPM) the UCC3995 utilizes a Linear Current Amplifier (LCA) to provide closed loop control and direct programming of the inrush current profile during start-up. The LCA allows the designer to program the maximum inrush current level and the slew rate of the inrush current. In addition, the <1mV input offset voltage of the LCA allows for low value sense resistors while not compromising low current applications and minimizing insertion loss across the hot swap interface.

To maintain the integrity of the host system power bus, the UCC3995 provides fault protection in the form of an electronic circuit breaker with a programmable over-current threshold. Detection of an over-current condition will result in the external NMOS device being immediately latched off.

The UCC3995 allows the designer to program how long the HSPM can operate in the current control mode to satisfy system specific load current requirements.

BLOCK AND SIMPLIFIED APPLICATION DIAGRAM



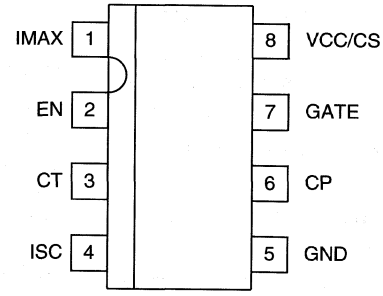
ABSOLUTE MAXIMUM RATINGS

V_{CC}/CS ..... –0.3V to 7V
Pin Voltage (Except CP Gate) ..... –0.3V to VCC+0.3V
Pin Voltage (CP and Gate) ..... –0.3V to 24V
I_{SET} current ..... 0mA to 1mA
Storage Temperature ..... –65°C to 150°C
Junction Temperature ..... –55°C to 150°C
Lead Temperature ..... 300°C

Currents are positive into, negative out of the specified terminal. Consult packaging section of Databook for thermal limitations and package considerations.

CONNECTION DIAGRAMS

SOIC-8 (Top View)
D Package



PIN DESCRIPTIONS

IMAX: This pin programs the constant current threshold level. The voltage across the resistor (R_{IMAX} connected between IMAX and the input voltage rail) will be equal to the voltage across R_S in constant current mode. The current sink on IMAX is determined by the resistor connected from the ISET pin to ground. The inrush current slew rate can be controlled by placing a capacitor in parallel with R_{IMAX}.

$$I_{MAX} = \frac{(V_R \bullet R_{MAX})}{(R_S \bullet R_{CS})}$$

$$I_{SC} = V_R \bullet \frac{(R_{MAX} + R_{INT})}{R_S \bullet R_{CS}}$$

$$I_{SC} = I_{MAX} \bullet \frac{(1 + R_{INT})}{R_{MAX}}$$

ISET: Output used to set the precision current sink on the IMAX pin as well as the Over-current threshold. A resistor should be connected from ISET to ground.

GND: Ground connection for the IC.

GATE: Output of the Linear Current Amplifier. This pin is used to drive the gate of the external NMOS device.

VCC/CS: This dual function pin is used for input power to the chip as well as current sense input for the LCA. The VCC current should have little effect on the accuracy of the constant current threshold due to the small valued sense resistor and the low supply current demands.

HI/EN: Pulling this pin below 0.8V will disable the external NMOS device and put the IC in sleep mode. Allowing this pin to float or driving to VIN will enable the UCC3995.

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Dual Sequencing Hot Swap Power Manager

FEATURES

- Precise Linear Current Amplifier for high efficiency and low voltage drop
- Controls inrush current and supply voltage ramp; ramp up sequence and slope and ramp down sequence
- Easily expandable to three or more supplies
- Programmable over-current detection threshold
- High voltage charge pump to drive low cost external NMOS devices
- Programmable soft start capability and fault timer
- Fault output indicator
- Shutdown Control with low sleep mode current (<1μA)
- Input undervoltage lockout
- Wide input operating range: 2.75V to 13.6V
- 16 pin SOIC and DIP packages

DESCRIPTION

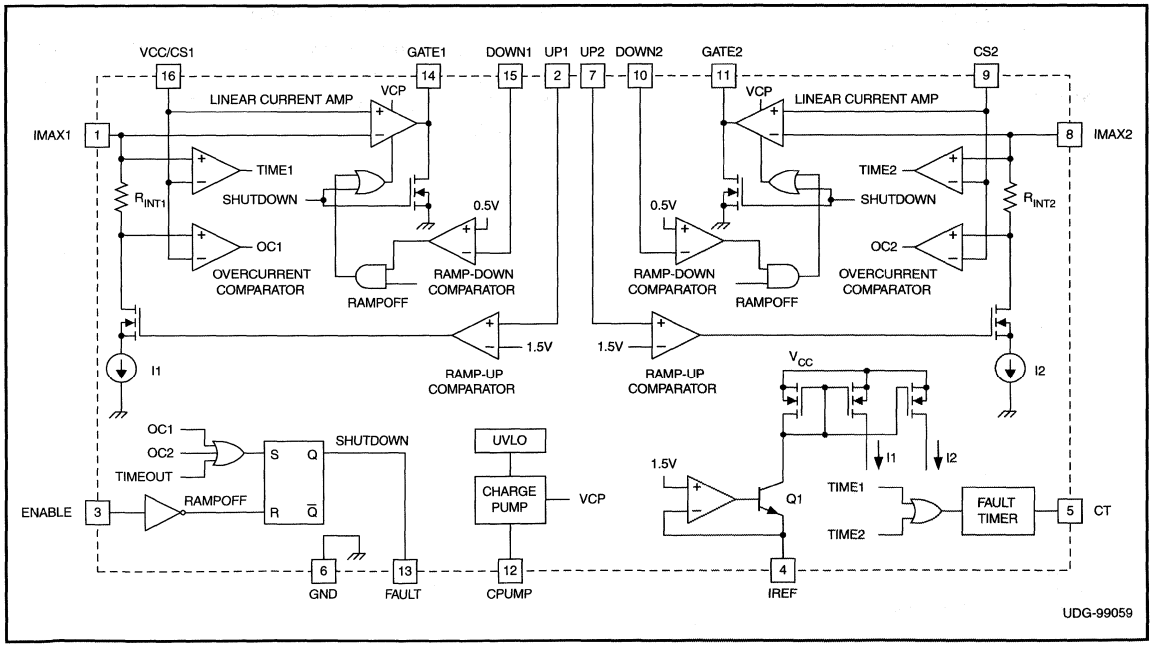
The UCC3996 family of Hot Swap Power Managers provides hot swap control, fault handling and power supply sequencing of two positive supplies. The UCC3996 operates over a wide supply range allowing single part inventory for a variety of output voltages.

Like other Unitrode Hot Swap Power Managers the UCC3996 utilizes a Linear Current Amplifier (LCA) to provide closed loop control and direct programming of the inrush current profile during start-up. The LCA allows the designer to program the maximum inrush current level and the slew rate of the inrush current. In addition, the <1mV input offset voltage of the LCA allows for low value sense resistors while not compromising low current applications and minimizing insertion loss across the hot swap interface.

To maintain the integrity of the host system power bus, the UCC3996 provides fault protection in the form of an electronic circuit breaker with a programmable overcurrent threshold. Detection of an overcurrent condition will result in the external NMOS device being immediately latched off.

The UCC3996 allows the designer to program how long the HSPM can operate in the current control mode to satisfy system specific load requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC}/CS1 . . . . . –0.3V to 15V
Pin Voltage
(Except V_{CC}/CS1, CP Gate1, Gate2) . . –0.3V to VCC +0.3V
IREF Current . . . . . 0 to –1mA
Storage Temperature . . . . . –65°C to 150°C
Junction Temperature . . . . . –55°C to 150°C
Lead Temperature . . . . . 300°C

Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and package considerations.

PIN DESCRIPTIONS

CPUMP: Charge pump output. A 0.1µF capacitor should be connected from this pin to ground. The capacitor provides charge storage to drive the gate of the external NMOS devices.

CS2: Current sense input 2. This pin is used as the current sense for the LCA on the second supply controller. This must be connected to the sense resistor on the input supply with the lowest voltage.

CT: Fault timer capacitor. A capacitor connected from this pin to ground determines the amount of time that the UCC3996 is allowed to operate in the constant current mode. The capacitance value must be selected to ensure that the load capacitance has adequate time to charge.

Note: *Connecting a scope probe or other metering device will alter the fault time.*

DOWN1, DOWN2: Ramp-down comparator inputs 1 and 2. These inputs are used to sequence the turn-off of the two supplies. The supply will start its turn-off when the voltage on the DOWN1, DOWN2 input pin falls below 0.5V.

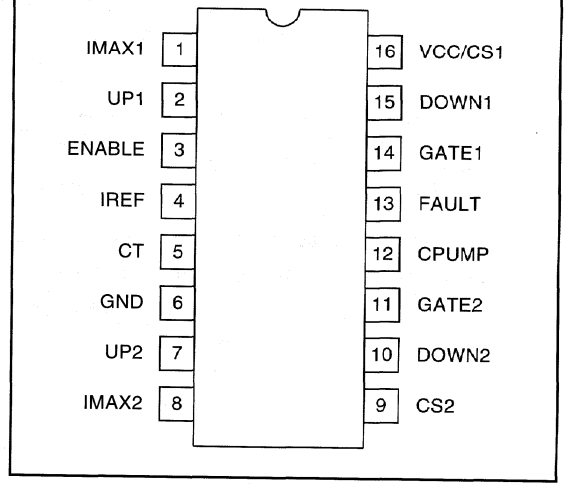
ENABLE: Device enable input. Pulling this pin below 0.8V will disable both external NMOS devices and put the IC in sleep mode. Allowing this pin to float above 0.8V or driving to VIN will enable the UCC3996.

FAULT: Fault output. This pin will be active high when a latched fault occurs. The fault can be the result of an overcurrent on either supply controller or a fault time-out on either supply during linear ramp-up.

GATE1, GATE2: Outputs of the Linear Current Amplifiers. These pins are used to drive the gates of the external NMOS devices. The LCA is internally compensated and guaranteed stable for gate capacitance between TBD and TBD.

CONNECTION DIAGRAMS

DIP-16, SOIC-16 (Top View)
Packages



GND: Ground connection for the IC.

IMAX1, IMAX2: Maximum source current. These pins program the constant current threshold level. The voltage across the resistor (R_{IMAX} connected between IMAX1, IMAX2 and the input voltage rail) will be equal to the voltage across R_{SENSE} in constant current mode. The current sink on IMAX1, IMAX2 is determined by the resistor connected from the IREF pin to ground. Placing a capacitor in parallel with R_{IMAX} controls the inrush current slew rate.

IREF: Reference current. This pin sets the precision current sink on the IMAX1, IMAX2 pins as well as the Overcurrent threshold. A resistor should be connected from IREF to ground.

UP1, UP2: Ramp-up comparator inputs 1 and 2. These inputs are used to sequence the ramp-up of the two supplies. The supply will ramp-up when the voltage on the UP1/UP2 input pin exceeds 1.5V.

VCC/CS1: Supply input and current sense1. This dual function pin is used for input power to the chip as well as current sense input for the LCA. VCC must be connected to the sense resistor on the input supply with the highest voltage. The VCC current should have little effect on the accuracy of thte constant current threshold due to the small valued sense resistor and the low supply current demands.

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UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information

by Bill Andreycak

The UCC3912 Demonstration Kit will enable designers to evaluate the performance of The UCC3912 Electronic Circuit Breaker in a typical application circuit. This kit features a number of programming options which include : individual "Hot Swap" of input and output connections, maximum current, Fault current level, and Shutdown. Each of these is programmed via switches located on the board. An LED indicates when the Current Fault Level comparator has been triggered and the device is in a low duty cycle mode.

List of switches, connections and functions:

SWITCH	CONNECTION (IC pin #)	FUNCTION
SW1	V_{IN} (2,3)	"Hot Swapping" of the input supply
SW2	V_{OUT} (14,15)	"Hot Swapping" of the output supply
SW3-1	I_{MAX} (10)	Sets maximum current level
SW3-3	B_3 (6)	Current Limit DAC Bit#3 input
SW3-4	B_2 (7)	Current Limit DAC Bit#2 input
SW3-5	B_1 (8)	Current Limit DAC Bit#1 input
SW3-6	B_0 (9)	Current Limit DAC Bit#0 input
SW3-8	Shutdown (1)	Shutdown input to disable IC

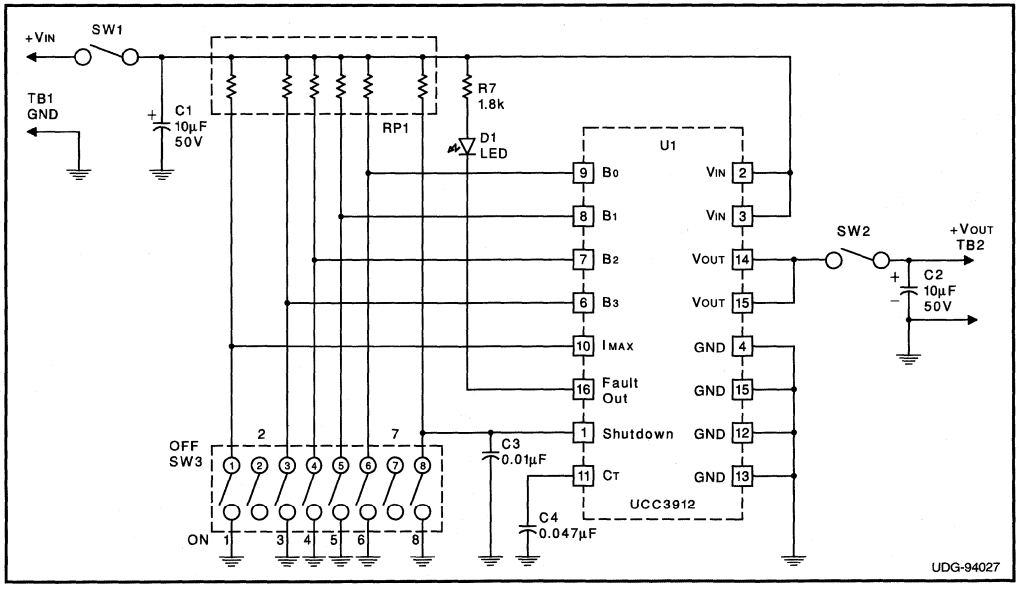

Figure 1. UCC3912 Demo Circuit Schematic

Programming the switches : Switch SW3 is a standard eight position DIP switch, but only six of these provide programming functions. The two switches located at positions 2 and 7 (SW3-2, SW3-7) are not used. Moving the switches toward the corresponding switch position number, or the "ON" direction GROUNDS the input and provides a digital "low", or zero. A digital "high" input is provided when the switches are in the "OFF" position, or facing towards switches SW1 and SW2.

Timing functions : The UCC3912 Demo Kit incorporates a 0.047 microfarad timing capacitor to provide fault protection. Using the equations found in the device's datasheet, the actual timing intervals can be determined by:

$FAULT = C_T \bullet 28 \bullet 10^3 = 1.3\ milliseconds$

$T_{SHUTDOWN} = C_T \bullet 10^6 = 47\ milliseconds$

The exact duty cycle during a fault condition is :

$$duty\ cycle = \frac{FAULT}{T_{SHUTDOWN}} = \frac{1.3ms}{47ms} = 2.8\%(typical)$$

Maximum load capacitance : The maximum load capacitance can also be calculated using the equations found in the UCC3912 datasheet. Since a wide range of maximum load currents, output voltages and timing capacitors can be used, the maximum load capacitance value will vary with each application. Note that the Demo Kit uses a 10µF electrolytic capacitor on the output (VOUT) connection which must be taken into account to determine the maximum capacitive load.

Supplying power : The Demo Kit has two terminal blocks for electrical connections to the input voltage supply and the output load. Terminal block TB1 is used for the input supply (VIN) and TB2 is used to connect the kit to an appropriate load. Observe the correct polarity (+/-) of the connections as indicated on the printed circuit board, or damage could result.

Input voltage range : 3 volts minimum to 8 volts maximum

Output load : An adjustable electronic load can be used to draw varying amplitudes of current through the UCC3912 Demo Kit. This type of load is much easier to use than fixed value power resistors to determine the exact current limiting threshold. One example of an adjustable electronic load is shown in Unitrode Design Note #DN-52 which can sink over 5 amps of DC current and dissipate over 35 Watts of heat without a fan. This design is adequate for comprehensive testing of the UCC3912 Demo Kit.

Output current range : 0 to 4 amps, 0 to 32 watts (approximate)

"Hot swap" testing should be performed using power resistors and/or capacitors to draw the specific load current and characteristics required. These should be placed across the Demo Kit output connections and testing performed by switching SW2 on and off while monitoring the load current and voltage. DO NOT USE AN ELECTRONIC LOAD unless it has been characterized for this "hot swap" application. Many electronic loads will attempt to draw very high current with a rapid application of input voltage and could falsely cause tripping of the UCC3912 Fault circuitry.

Other Applications : While primarily intended for "hot swap" data communications power supply applications, the UCC3912 also lends itself to any low

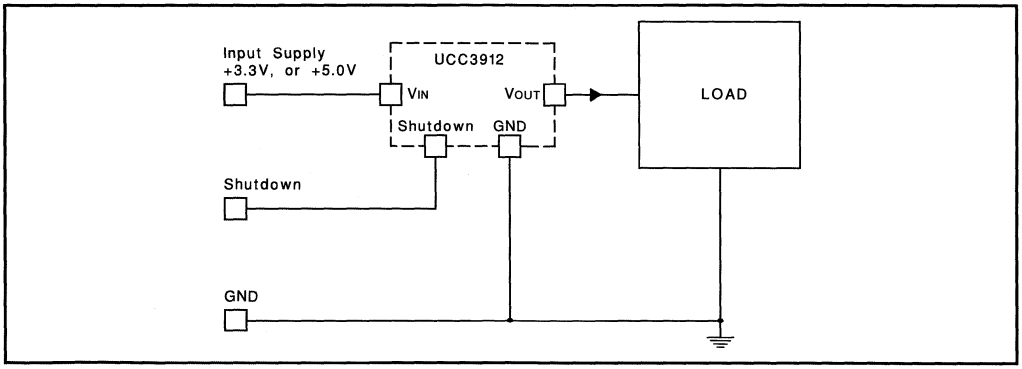

Figure 2. UCC3912 Used as a Low Current Standby (<5µA) Power Switch

voltage circuit breaker or protection application below 4 amps. Some of these include battery powered tools and equipment, PCMCIA card power switching and many 3.0V, 3.3V and 5.0 volt power supplies.

Summary: The features of the UCC3912 Electronic Circuit Breaker offer design flexibility and programmable maximum current protection for a wide variety of power applications including : data communications, computer, battery powered and portable equipment, PCMCIA card power, industrial controls and many low voltage power supplies.

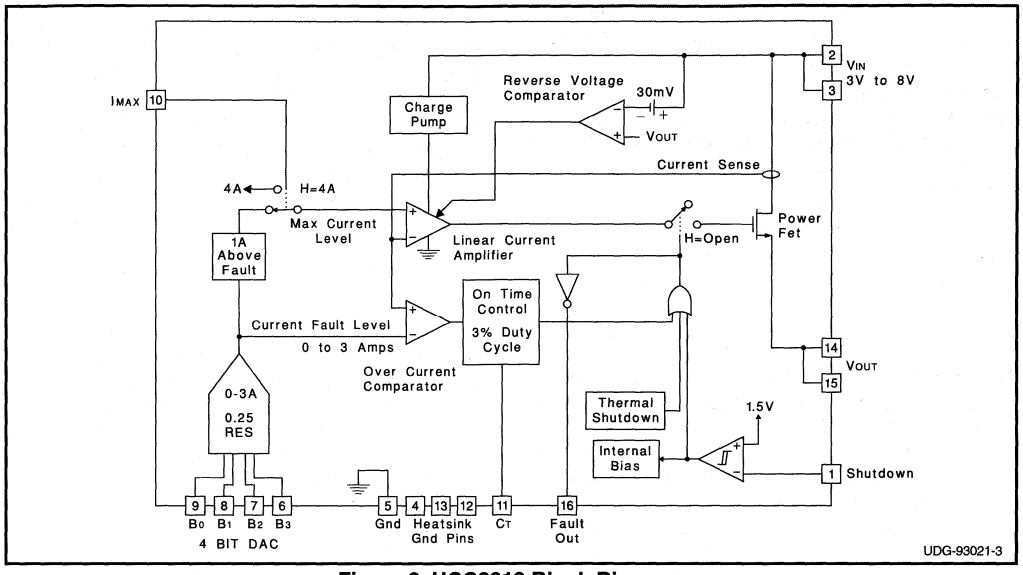

Figure 3. UCC3912 Block Diagram

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Design Note

UCC3913 Electronic Circuit Breaker for Negative Voltage Applications Evaluation Kit List of Materials for a -48V/1A Test Circuit

by Bill Andreycak

Many battery powered and Telecommunications power supplies use some form of protection to prevent high currents from flowing during a short circuit or overload condition. This function is often performed by a self-resetting circuit breaker -as opposed to a fuse, which would require manual replacement whenever triggered. Circuit breakers can be implemented in a number of different ways, but the most popular approach is use a MOSFET transistor which can be switched on and off as required. Load current is typically sensed with a low value resistor and compared to a reference level to determine when an overcurrent condition exists. This function can be achieved with discrete circuitry or with a fully integrated solution, such as the UCC3913 Negative Voltage Circuit Breaker. This Design Note highlights the UCC3913 Evaluation Board in a typical –48VDC, 1A application circuit. Complete details for programming the various features of the device can be obtained from the UCC3913 Datasheet, found in the Unitrode Product and Applications Handbook.

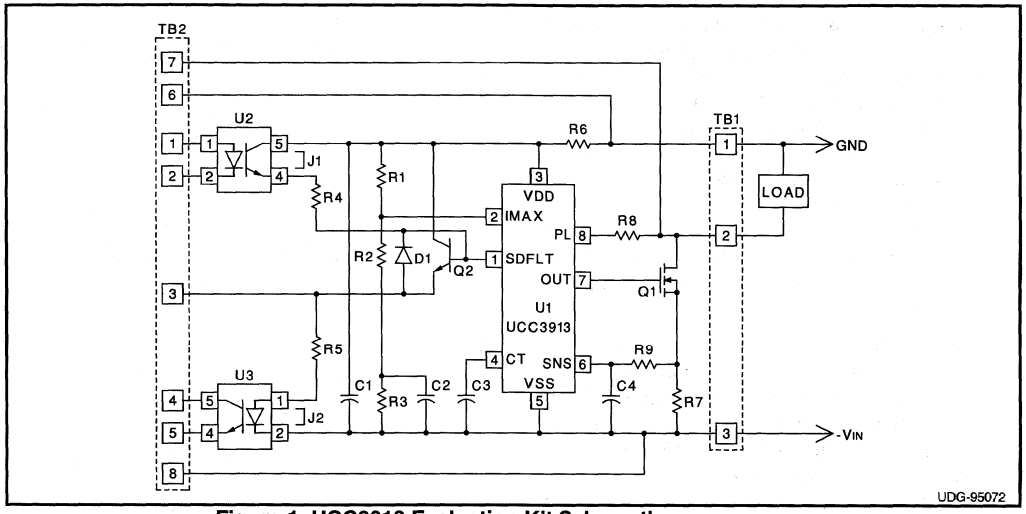

Figure 1. UCC3913 Evaluation Kit Schematic

List of Materials :

C1	1µF/16VDC Ceramic
C2	not used - open circuit
C3	1.5nF/16VDC
C4	not used - open circuit
D1	1N4148 Diode
Q1	IRF630 200V/5A MOSFET
Q2	2N2222 NPN
R1	24k, 1/4W
R2	510 ohms, 1/4W
R3	JUMPER - use AWG 22 wire
R4	47k, 1/4W
R5	1k, 1/4W
R6	3.3k, 1/4W or Qty (4) 13kΩ 1/8W SMT resistors in parallel
R7	50 milliohm shunt
R8	510k, 1/4W
R9	JUMPER - use AWG 22 wire
U1	UCC3913 IC
U2,3	4N29 Optocoupler

Test Equipment :

Power supply : 48VDC / 1.5ADC
Programmable electronic load to sink 1.5A at 48VDC

5/95

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Design Note

Paralleling UCC3912 Electronic Circuit Breaker ICs

By Paul Aloisi and Bill Andreycak

The UCC3912 IC is an integrated 3 Amp electronic circuit breaker which includes programmable overcurrent protection and retry timing following a fault. Other common uses for this function are in higher current (12A) and low "headroom" applications where a lower voltage drop is required. Each of these can be addressed by paralleling UCC3912 devices as shown in Figure 1.

To provide the circuit breaker function, the UCC3912 uses an internal FET switch having a typical on resistance of 0.150 ohms and 3 Amp continuous current rating. The positive temperature characteristics of MOS devices are beneficial in parallel applications to help divide the total load current evenly amongst all of the devices used. The UCC3912 with the lowest on resistance will pass slightly more of the current than the others, but its forward voltage drop will increase accordingly. This causes the load current to steer towards the other devices (in parallel) which were previously passing less current. With this configuration, equilibrium will be reached quickly as the total load current is distributed amongst all of the slaves.

One feature of the UCC3912 is its digitally programmable threshold for overcurrent limiting. When this current level is reached, the UCC3912 control circuitry regulates current to the programmed IMAX amplitude. To facilitate this, the gate drive to its internal MOS pass device is reduced, causing its on resistance and corresponding voltage drop to increase. As in the previous example for paralleled devices, this steers current to the other UCC3912s in parallel, forcing load sharing.

The duration of this allowable overcurrent condition is also programmable by selecting the appropriate timing capacitor value to the IC's fault timing (CT) pin. When the overcurrent condition is detected, two protection functions begin operation. First, the UCC3912 goes into a constant current mode to regulate current to the pro-

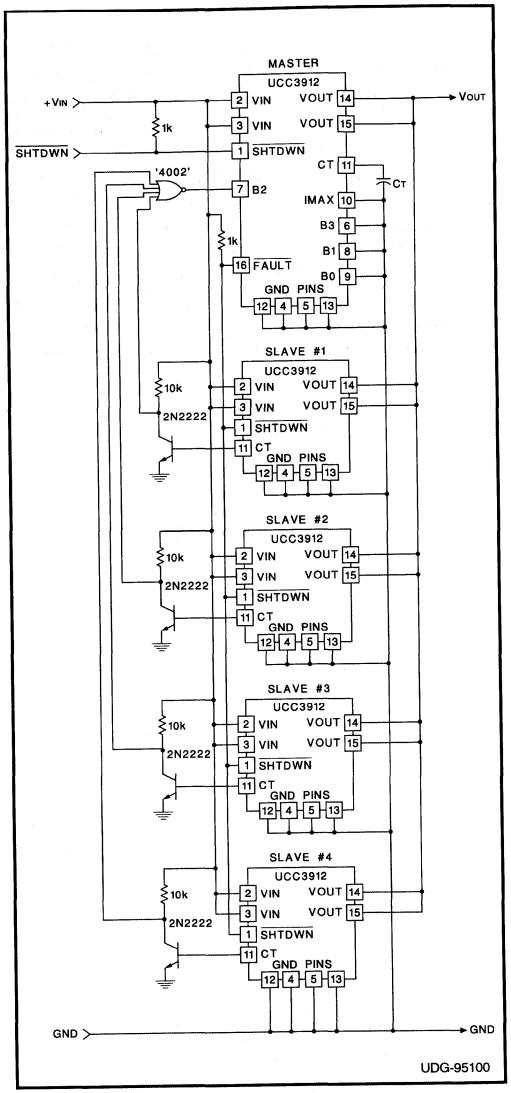

Figure 1. Paralleling UCC3912 Electronic Circuit Breakers

grammed value of IMAX. Simultaneously, the device begins charging the fault timing capacitor and provides a digital indication at the open collector FAULT pin of the IC. The overcurrent duration concludes when the timing capacitor charges to a preset voltage and the MOS pass transistor is turned off. The off time is internally controlled to thirty times the programmed fault duration ($t_{OFF} = 30 \bullet t_{FAULT}$), resulting in an approximate three percent (3%) effective duty cycle to safely limit power dissipation into a short circuit. Note that the UCC3912 also features internal overtemperature shutdown protection should the timer be incorrectly programmed for too long of a fault duration or inadequate heatsinking provided. Consult the UCC3912 datasheet for complete details of the timing and fault protection circuitry operation into single and repetitive overcurrent conditions.

Circuit Operation

In this paralleled application of UCC3912 devices, a master/slave arrangement will be incorporated and the fault timing control will be governed entirely by the master. Slave devices are configured to give a digital representation of the overcurrent condition, and their individual CT outputs are "NOR"ed together as an input to the master. A generic CMOS '4002 digital IC is used for its low current and 3V operational characteristics. Note that each input requires a 2N2222 NPN signal level transistor with a 10k ohm pull up resistor from the input supply (V_{IN}) to its collector to complete the interface. This arrangement is necessary to achieve the proper digital inputs to the NOR gate while clamping the UCC3912 CT pin voltages to just a base-emitter diode drop (V_{BE}) above ground. This will override the internal timing circuits of the individual slaves which are being controlled by the master's fault timer.

In normal operation (prior to any overcurrent condition) the CT pin of each slave UCC3912 is low and the corresponding NPN transistor is off. The 10k ohm collector resistors place a digital high on the NOR gate's four inputs, and the output of this gate is low. When any of the slave UCC3912 devices goes into overcurrent protection its CT pin is pulled high by an internal current source. Normally, this would start charging the fault timing capacitor, but in this paralleled application, it forward biases the base-emitter junction of the respective 2N2222 transistor. This turns on the NPN device and forces a digital low input to the NOR gate. When all four of the NOR inputs go low, the output of the NOR gate goes high. This indicates that all four of the slaves are limiting current to their programmed maximum level and that an overcurrent condition exists.

The output of this NOR gate is used to digitally program one bit (BIT2) of the master UCC3912's overcurrent limit. The master was previously "off", not providing any load current since it's four overcurrent inputs (BITs 0 through 3) were all low. Any digital input below "0100" programs its output current to zero by turning off the power switch. But triggered by the overcurrent conditions of the slaves, the NOR gate output switches BIT2 of the master high. This turns the master on and programs its output current to 0.25A by the "0100" code at BITS 0 through 3. The master now allows 0.25 amps in addition to the slaves 12 amps to the load for a system total of 12.25A. This is the sum of the master (0.25A) and the four slave overcurrent programming thresholds of three amps each (4 • 3.0A). Provided that the demanded load current is in excess of 12.25 amps, as would be the case with a short circuited load, the master then provides two functions. First, it regulates the current through the master to the programmed 0.25 amp level. Additionally, it begins a fault timing sequence, the duration of which is programmed by the value of the fault timing capacitor, CT. This capacitor charges during the overcurrent condition until it reaches the internal 1.5 volt fault threshold. Once triggered, the fault latch turns off the UCC3912's internal MOSFET switch (to provide the circuit breaker function) while also indicating the fault condition by providing a "low" on the IC's FAULT pin. Note that the master's FAULT output is connected to the slaved UCC3912s' SHTDWN pin which turns off all of the slaved devices at the same time that the master turns off.

The duration of the overcurrent event is programmed entirely by the master's CT timing capacitor value according to the UCC3912 datasheet information and design equations. The timing circuitry will deliver a current limited, pulsed mode fault protection and retry with a three percent (3%) duty cycle. While the timing capacitor is charging, each IC regulates and compares its load current to the programmed fault overcurrent level. Providing that the fault condition does exist, all UCC3912 ICs are turned off for the remaining ninety-seven percent (97%) of the programmed fault timing period. The resulting three percent duty cycle fault mode facilitates safe operation into a continuous overload or short circuited condition. It safely limits input power consumption and power dissipation in the circuit breaker switches. Additionally, no costly system downtime or manual replacement of a fuse or resetting of a circuit breaker is required.

Once the abnormal load condition has been removed, the circuit goes back into normal operation. The master's $\overline{\text{FAULT}}$ output returns to a "high" along with each of the slaves' $\overline{\text{SHTDWN}}$ inputs. If the load has not been removed, the master is retriggered by the NOR gate once each slave has detected an overcurrent condition, and the system goes back to the three percent duty cycle protection mode.

Note that the entire system is nominally triggered at 12.25A which is programmed by the four UCC3912 slaves' individual 3A thresholds and the 0.25A contribution of the master. However, this is unlikely to occur in a typical application because of two of the device's other ratings. First, is the maximum specified "trip" current of 3.5A for each slave switch and 0.45A for the master with the programmed overcurrent inputs (Bits 0 - 3). This would raise the highest trigger threshold to 14.45A. However, the more dominant factor is the high current capability of the UCC3912's switch which - is rated at four amps (4A) typical. In fact, each device can safely provide 5.2A (worst case) over all rated temperature and manufacturing conditions. One possible scenario should be reviewed using an instantaneous short circuit on the outputs. Even though all of the slaves properly triggered their internal fault logic at 3.5A (worst case), all four of the slaves could be delivering as much as 5.2 amps maximum (within the device's ratings) to the load. This would correspond to a maximum load current of 21.25 amps. And while unlikely to repetitively occur in a typical application, it does represent the worst case sum of the four slaves'(4 • 5.2A) plus the master's (0.45A) maximum current ratings. However, it's advised to evaluate this figure to that of other fault protection and overcurrent techniques, for example fuses, which can be significantly higher for short durations. More specific details and comparisons can be found in Unitrode Application Note U-151.

Other Applications

This design example utilized the UCC3912 device's rated current capability of 3A, but can be scaled for other applications with higher or lower requirements. Each slave can be individually programmed for a maximum current between 0.25A and 3A in 0.25A increments using the 4 bit digital inputs to the fault circuitry. This is beneficial in many low voltage supply applications which require a low headroom or dropout voltage (the voltage drop between the input and output connections of the circuit breaker) to meet the load's power supply specifications. In these, the UCC3912's could be paralleled to minimize the series voltage drop - and not to obtain the higher current capability of the system. This is one application where it is desirable to program the slave's overcurrent thresholds to a lower value than 3A each.

The 0.25A example of additional load current provided by the master can also be raised to deliver higher total system current to accommodate a transient load condition. Examples of this can be found in many battery powered energy management systems where only the required active circuitry is enabled and all others are switched off. When supplying power to these types of loads, often high inrush currents are needed to quickly charge up any local bypassing and filtering capacitors. This brief condition can be accommodated by programming the master UCC3912's overcurrent bits accordingly.

Although switching of only the master UCC3912's BIT2 is shown, its BIT3 input can also be switched for higher current capability. Additionally, BIT0 and BIT1 are shown grounded in the example circuit but can be programmed or switched with digital "1"s as well. Active digital programming of the master and all slave overcurrent BITs is also possible for the more demanding overcurrent protection applications. Each UCC3912 Electronic Circuit Breaker IC also features internal overtemperature protection with shutdown for complete system protection.

Additional Reference Material:

[1] UCC3912 Data Sheet

[2] Application Note U-151: "UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information"

[3] UCC3912 Evaluation Kit

[4] Design Note DN-58: "UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information"

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Design Note

UCC3981 USB Power Controller IC, Evaluation Board, Schematic, and List of Materials

By Chuck Melchin

Introduction

The UCC3981 Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage as well as four 5V regulated voltages for USB ports. The 3.3V linear regulator is used to provide power to a local USB microcontroller. The 5V outputs are current limited to 500mA and the 3.3V output to 100mA in full compliance with USB specifications.

This demonstration kit provides all the circuitry necessary to evaluate the performance of the UCC3981 in a typical application. Each of the 5V outputs, as well as the 3.3V microcontroller voltage, can be individually enabled for optimal port control. Output enable is accomplished by the use of a five-position dipswitch and overcurrent signals are pulled up to the input voltage through 10KΩ resistors. Both enable and overcurrent signals are available at a 10 position in line SIP for easy scope probe access. The demo kit utilizes an external NMOS switch in a low dropout linear regulator for pre-regulating a rough DC voltage, such as a filament voltage, to provide the 5.5V input to the four 5V linear regulators.

This kit can also provide a valid means of evaluating the UCC39811 in a typical application circuit. The UCC39811 is intended to perform the same tasks as the UCC3981 with the exception of providing the gate drive and control circuitry for the 5.5V preregulator. The preregulator function can be bypassed by providing 5.5V externally at VREG, removing Q1 and replacing C09 with a 0.1μF ceramic capacitor. In this case VFIL and VHUB should also be connected to the 5.5V supply providing DC bias for the 3.3V regulator and the gate drive for the internal 5V regulators.

TESTING PROCEDURE

1. Set all enable switches to the "off" position. SW1 switches 1-4 correspond to outputs ENA-D respectively. Switch 5 controls ENHUB.
2. Supply a minimum of 6V, maximum of 9V, from a 2A minimum supply to the V_{FIL} banana jack. Apply a 5V, 500mA supply to the V_{HUB} banana jack. Connect grounds for both supplies to the demonstration kit ground. Ensure the maximum voltage of 9V is not exceeded on either the V_{FIL} or V_{HUB} pins.
3. Connect a voltmeter to the VREG output. The voltage should read approximately 5.5V.
4. Connect the voltmeter to the V5A output. The output voltage should read approximately 0V.
5. Set the enable switch (ENA) for V5A to the "on" position. The output voltage should read approximately 5V. The corresponding enable pin of the 10 position SIP should transition from a low to a high.
6. Repeat steps 4 and 5 for outputs V5B – V5D and the 3.3V output.
7. Apply variable resistive loads to all outputs. Increase the loads sequentially to approximately 500mA on the 5V outputs, and 100mA on the 3.3V output. The appropriate overcurrent flags on the 10 position SIP should transition from a high to a low as each output reaches its overcurrent condition. Reset each load to its nominal value after observing each output's overcurrent flag to prevent thermal problems with the device. The overcurrent flags would normally signal the USB controller of the overcurrent condition and the controller would shut down the appropriate output in an actual application. The overcurrent flags should return to a logic high once the load is reset to its nominal value.
8. Reset the enable switch for each output. The corresponding output voltages should read approximately 0V.
9. Power down the input supplies.

If the testing procedure is successfully completed the demonstration kit is verified to be functional and is ready for more rigorous and application specific evaluation to be performed.

For more complete information, pin descriptions and specifications for the UCC3981 USB power controller IC, please refer to the UCC3981 data sheet or contact your Unitrode Field Applications Engineer.

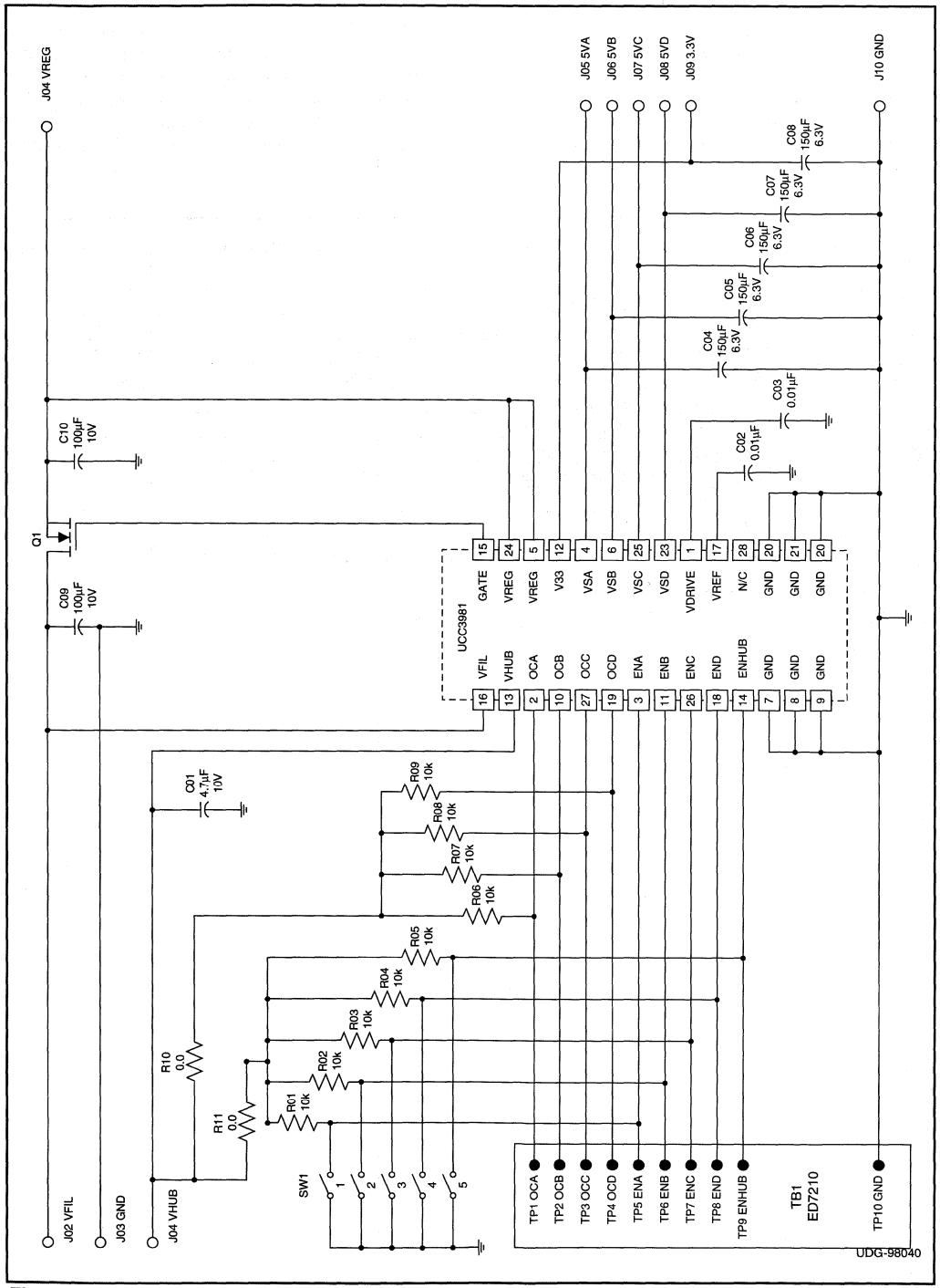

Figure 1. UCC3981 evaluation board schematic.

Notes:

1) *Absolute Maximum voltage for VHUB is 9.0V*
2) *Absolute Maximum voltage for VFIL is 9.0V*
3) *VHUB and VFIL can be connected together*
4) *Pregulator can be bypassed by providing 5.5V at VREG and VFIL, removing Q1 and replacing C09 with a 0.1µF Ceramic capacitor.*
5) *ENABLE and OVERCURRENT signals are pulled up to VHUB. 0Ω jumpers R10 and R11 can be removed to wire pullups to a different voltage*
6) *Capacitors C04 through C10 can be replaced with size "D" Tantalum SMD capacitors.*
7) *Capacitor C01 can be replaced with size "B" Tantalum SMD capacitors.*

Reference Designator	Description	Manufacturer	Part Number
R01–R09	10k, 5%, 1/8W, Metal Film Resistor		
R10, R11	0.0W, 5%, Jumper, Metal Film Resistor		
TB1	Pin Header, 10 position	Mill-Max	ED7210
SW1	DIP Switch, 5 Position, SPST	AMP	A5205
C01	4.7µF, 10V, Tantalum Capacitor		
C02, C03	0.01µF, Z5U, Ceramic Capacitor		
C04–C08	150µF, 6.3V, Electrolytic Capacitor		
C09, C10	100µF, 10V, Electrolytic Capacitor		
J01–J10	Binding Post		
U1	USB Power Controller IC	Unitrode	UCC3981
Q1	60V, 17A, N-Channel MOSFET	International Rectifier	IRFZ24

Table 1. UCC3981 evaluation board list of materials.

Note: UCC3981 is also the UCC3831. UCC39811 was formerly UCC38531.

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Design Note

UCC3918 "Low On-Resistance Hot Swap Power Manager", Evaluation Board, Schematic, and List of Materials

By Dave Olson

INTRODUCTION

The UCC3918 evaluation kit allows the designer to evaluate the performance of the UCC3918 Low On-Resistance Hot Swap Power Manager in a typical application circuit. The schematic for the evaluation kit is shown in Figure 1.

FEATURES

- Integrated 0.06Ω Power MOSFET
- 3V to 6V Operation
- External Analog Control of Fault Current 0A to 4A
- Independent Analog Control of Current Limit up to 5A
- Overload Protection
- 1μA ICC when Disabled
- Programmable On Time
- Programmable Start Delay
- Fixed 3% Duty Cycle During Fault Conditions

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 8V
SOIC Power Dissipation. 2.5W
Fault Output Sink Current. 50mA
Fault Output Voltage . . . . . V_{IN}
Output Current (DC) . . . . . Internally Limited
TTL Input Voltage. . . . . –0.3V to V_{IN}

Functions of SW1, SW2 and SW3

SW1 and SW2 provide the designer with the flexibility of evaluating the performance of the UCC3918 when residing on either the system backplane or on an adapter card. Closing SW1 after SW2 simulates an application where the UCC3918 resides on a plug-in adapter card. Closing SW1 prior to SW2 simulates an application where the UCC3918 resides on the system backplane. SW3 provides a shutdown input to disable the IC.

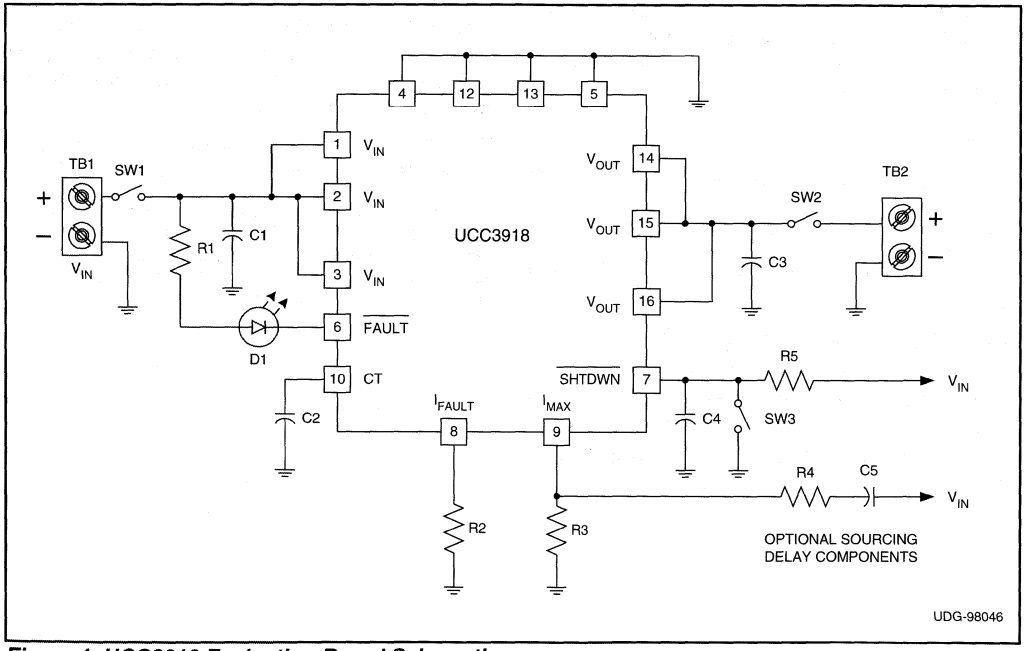

Figure 1. UCC3918 Evaluation Board Schematic

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Calculating Maximum Sourcing Current (I_{MAX})

The maximum sourcing current is programmed by selection of R3, connected from pin 9 (I_{MAX}) to GND. R3 can be calculated as:

$$R3 = \frac{126k}{I_{MAX}}\ \Omega \qquad (1)$$

For the UCC3918 evaluation kit R3 is set to 42.2kΩ for I_{MAX} = 3A typical. Please refer to the UCC3918 data sheet for further discussion of I_{MAX}.

Calculating the Fault Current (I_{FAULT})

The I_{FAULT} pin allows linear programming of the fault level current from 0 to 5A. When operating below the fault current the internal FET will be fully enhanced providing low on resistance. When output currents exceed I_{FAULT} the output remains on but the fault timer starts charging CT. R2 sets the current fault level. R2 can be calculated as:

$$R2 = \frac{105k}{I_{FAULT}}\ \Omega \qquad (2)$$

For the UCC3918 evaluation kit R2 is set to 52.3kΩ for I_{FAULT}= 2A typical.

Calculating the Fault and Shutdown Times

The UCC3918 evaluation kit incorporates a 0.1µF timing capacitor, C2 (CT) to set the fault time. The fault and shutdown times can be found by using the following equations.

$$T_{FAULT} = 27.8k \bullet C2 \qquad (3)$$

$$T_{SHUTDOWN} = 0.833X10^{6} \bullet C2 \qquad (4)$$

Where C2 is in Farads and T is in Seconds.

For the evaluation board T_{FAULT} = 2.78mSec and $T_{SHUTDOWN}$=83.3mSec.

Estimating Maximum Load Capacitance

The maximum load capacitance that can be charged depends on several factors; the nature of the load (constant current or resistive), the maximum sourcing current, and the allowed fault time.

For a constant current load, the maximum capacitance can be estimated from:

$$C_{OUT} = \qquad (5)$$

$$(I_{MAX} - I_{LOAD}) \bullet \left[\frac{27.8X10^{3} \bullet C2}{V_{OUT}}\right] Farads$$

For a resistive load of value RL, C_{OUT} can be estimated from:

$$C_{OUT} = \frac{27.8x10^{3} \bullet C2}{RL \bullet \ell n\left[\dfrac{1}{1 - \dfrac{V_{OUT}}{I_{MAX} \bullet RL}}\right]} Farads \qquad (6)$$

SAFETY RECCOMMENDATIONS

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL or some other safety agency rating is required, a redundant safety device such as a fuse should be placed in series with the power MOSFET device. The UCC3918 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

Note: *Capacitor C1 is located on the component side of the input switch and will contribute to the inrush current.*

For more complete information, pin descriptions and specifications for the UCC3918 Low On-Resistance Hot Swap Power Manager, please refer to the UCC3918 data sheet or contact your Unitrode Field Applications Engineer at (603) 424-2410.

Reference Designator	Description	Manufacturer	Part Number
C1	22µF, 25V Tantalum Capacitor	Sprague	199D226X0025DA1
C2	0.1µF, 50V Ceramic Capacitor		
C3	22µF, 25V Tantalum Capacitor	Sprague	199D226X0025DA1
C4	Not Populated		
C5	Not Populated		
D1	LED		
R1	300Ω, 0.25W Resistor		
R2	52.3kΩ, 0.25W Resistor		
R3	42.2kΩ, 0.25W Resistor		
R4	Not Populated		
R5	10kΩ, 0.25W Resistor		
SW1	Slide Switch		
SW2	Slide Switch		
SW3	Dip Switch		
TB1	Terminal Block		
TB2	Terminal Block		
U1	Low On-Resistance Hot Swap Power Manager	Unitrode	UCC3918

Table 1. UCC3918 Evaluation board list of materials.

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Design Note

UCC3919 Hot Swap Power Manager Evaluation Circuit and List of Materials

By Robert B. Diener

INTRODUCTION

The UCC3919 evaluation board is designed to allow the user to fully test the capabilities of the UCC3919 Hot Swap Power Manager. Overcurrent protection circuitry can be added to either a plug in adapter card that is being hot swapped or to the backplane circuit itself. This circuit can be used to test the capabilities of the UCC3919 Hot Swap Power Manager for either application.

EVALUATION BOARD FEATURES

- 3V to 8V operation
- Fault current threshold of 5A
- Maximum output current of 7A during fault
- Overload shutdown (Electronic Circuit Breaker)
- On-board fault indicator
- On-board N-channel MOSFET with 0.011Ω $R_{DS(on)}$
- On-board 0.01Ω, 1W sense resistor
- Choice of manual or automatic reset modes
- Choice of 3% duty cycle current limiting or average power limiting during fault
- Shutdown function
- Optional provision for soft-start delay

CONTROL SWITCHES

The UCC3919 Hot Swap Power Manager Evaluation Circuit has several switches enabling the user to evaluate its operation in different configurations.

SW1 and SW2 can be used to mimic the connections between a back plane and a plug in adapter card. The order of operation for these switches will determine whether the protection circuitry is located on the plug in adapter card or on the backplane. By closing SW1 prior to SW2, the circuit will

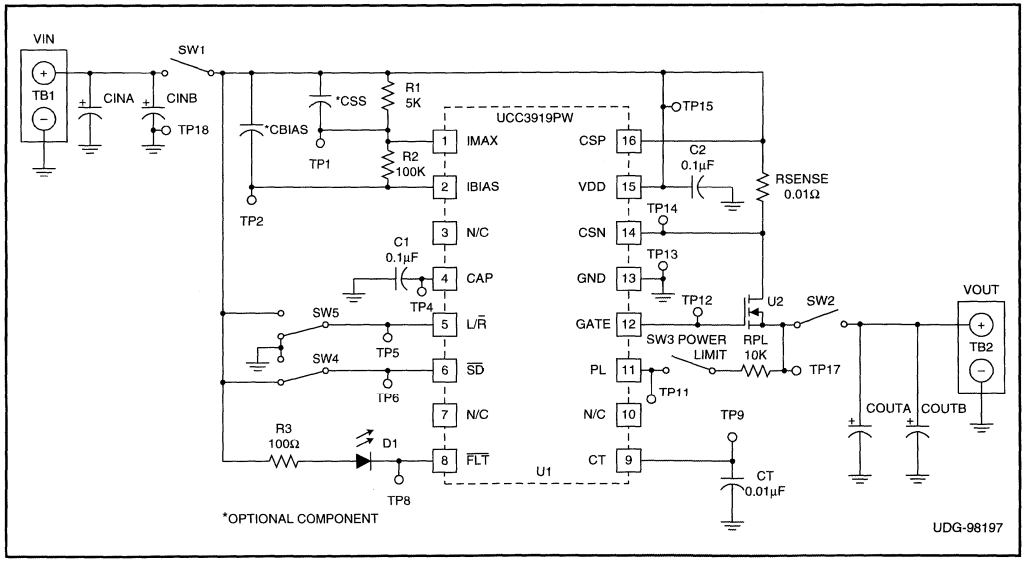

Figure 1. Schematic diagram.

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simulate a situation where the protection circuitry is located on the back plane. Closing SW2 prior to SW1 simulates a situation where the protection circuitry is located on the adapter card that is being hot swapped.

SW3 controls the Power Limit function. In the PLIM position, the PL pin is connected to the output via a 10k resistor. During a fault condition, as the input voltage is increased the duty cycle will decrease and the average power will be held relatively constant. In the HCCP position, a fault condition will cause the output to be limited to a 3% duty cycle independent of input voltage.

SW4 controls the shutdown pin. In the SD position the UCC3919 will be put into a low current standby mode and the external MOSFET will be turned off.

SW5 controls the L/R pin. While in the LATCH position, a detection of a fault condition will cause the external MOSFET to be turned off and remain off until SW5 is set to the RESET position or the power is cycled. With SW5 in the RESET position, a fault condition will cause the circuit to be in hiccup mode until the output current falls below I_{FAULT}.

CURRENT THRESHOLDS

I_{FAULT} is the output current threshold that starts the fault timer. For this circuit, I_{FAULT} has been set to 5A. The fault timer will run until either the output current falls below I_{FAULT} or until it times out. If the fault timer times out, the external MOSFET will turn off and the circuit will enter a fault condition.

I_{MAX} is the maximum output current the circuit will supply. For this circuit I_{MAX} has been set to 7A. During a fault, if SW5 is in RESET mode the output will be duty cycle limited and the current supplied during TON will be limited to I_{MAX}. If I_{MAX} is set below I_{FAULT}, the external MOSFET will be in a high power dissipation mode limiting the output current to I_{MAX} and the circuit will never enter a fault condition.

$I_{OVERLOAD}$ is the threshold that will activate the circuit breaker function. For this circuit $I_{OVERLOAD}$ has been set to 27A. This threshold could be reached if the circuit is already powered up and a heavy load or a direct short is applied to the output. In this case the overload comparator will take over, the external MOSFET will turn off immediately, and the fault timer will be started.

OPERATION

Fault Timer

During normal operation the external MOSFET is fully on and current is supplied to the output. If the output current rises above I_{FAULT}, the fault timer will be started. I_{FAULT} is calculated as:

$$I_{FAULT} = \frac{0.05V}{R_{SENSE}} \quad (1)$$

The fault timer is controlled by the CT capacitor. When the fault timer is started, the CT capacitor will charge up to 1.5V as long as the output current is above I_{FAULT}. If the voltage across CT reaches 1.5V the external MOSFET will turn off and the circuit will enter a fault condition. The time required for CT to charge from 0V to 1.5V is referred to as $T_{ON\ (INIT)}$. With SW3 in the HCCP position, $T_{ON\ (INIT)}$ for this circuit is approximately 430µs. $T_{ON\ (INIT)}$ is calculated as:

$$T_{ON(INIT)}(\text{sec}) = \frac{CT(\mu F) \bullet 1.5}{35\mu A + I_{PL}} \quad (2)$$

If SW5 is in the LATCH position, the output will stay off until switched back to RESET or the power is cycled. If SW5 is in the RESET position the CT capacitor will then discharge to 0.5V at which point the external MOSFET will turn back on. If the output current is above I_{FAULT}, the process will repeat with the external MOSFET on during the charge time of the CT capacitor and the external MOSFET off during the discharge time of the CT capacitor. The charge and discharge times are referred to as T_{ON} and T_{OFF} respectively. With SW3 in the HCCP position, T_{ON} and T_{OFF} are calculated as:

$$T_{ON}(\text{sec}) = \frac{CT(\mu F)}{35\mu A + I_{PL}} \quad (3)$$

$$T_{OFF}(\text{sec}) = \frac{CT(\mu F)}{1.2\mu A} \quad (4)$$

I_{PL} will be zero if SW3 is set to HCCP. If the circuit enters a fault condition with SW3 set to HCCP, the output current will be duty cycle limited to 3%. For this circuit, T_{ON} = 280µs and T_{OFF} = 8.3ms.

If the circuit is in fault and SW3 is set to PLIM the circuit will be in the power limit mode. In this mode I_{PL} is calculated as:

$$I_{PL} = \frac{V_{IN} - V_{OUT} - V_{PL}}{R_{PL}} \quad (5)$$

V_{PL} is measured with respect to the CSP pin as listed in the UCC3919 data sheet.

While in power limit mode, as the input voltage is increased, the duty cycle of the output will decrease, thus keeping the power dissipation relatively constant. For this circuit, with VIN=5V and the output shorted, I_{PL} will be approximately 320µA. The circuit will have T_{ON}=25µs for an average power dissipation of approximately 68mW. If the input voltage is raised to 8v, T_{ON} will decrease to 14µs and the average power dissipation will be approximately 57mW. T_{OFF} will remain the same independent of SW3.

Timing Capacitor

The CT capacitor must be selected to ensure that the UCC3919 will not enter fault mode during the initial start-up or when recovering from a fault in the hiccup mode. The selection of CT is dependent upon the type of load and the size of the load capacitor. If CT is too small or COUT is too large, the CT capacitor will charge up to 1.5V and the circuit will enter a fault mode before COUT is allowed to fully charge. Refer to the UCC3919 data sheet when changing the value of the CT capacitor.

For this circuit, the CT capacitor has been selected to be 0.01µF. When operating in the hiccup mode with a duty cycle of 3%, COUT (MAX) is shown in Equation (6).

where I_{CH}, the charging current of the CT capacitor is approximately 35µA. With VIN=5V and an output current of 3.3A, the maximum value for COUT is approximately 290µF.

When operating in the power limit mode, the maximum value for COUT can be calculated in Equation (7).

With VIN=5V and an output current of 3.3A, the maximum value of COUT is approximately 71µF.

I_{MAX}

Once the output current has risen above I_{FAULT}, the internal linear amplifier will limit this current to a maximum of I_{MAX}. I_{MAX} is determined as:

$$I_{MAX} = \frac{1.5V \bullet R1}{(R1+R2) \bullet R_{SENSE}} \quad (8)$$

If I_{MAX} is set to a level lower than I_{FAULT}, the UCC3919 will limit the output current to a maximum of I_{MAX}, while never entering a fault condition. This leaves the external MOSFET in a high power dissipation region.

$I_{OVERLOAD}$

With the circuit powered up, a heavy load or a direct short suddenly applied to the output will cause the output current to spike. If this current reaches $I_{OVERLOAD}$, the external MOSFET will immediately turn off and the fault timer will start. $I_{OVEROAD}$ is calculated as:

$$I_{OVERLOAD} = I_{MAX} + \frac{0.2V}{R_{SENSE}} \quad (9)$$

This condition occurs only if SW2 is closed after SW1. For cases where SW2 is closed before SW1, an optional capacitor, CSS can be added to the circuit to provide for a soft start. In this case CSS will limit the slew rate of the output current.

If the circuit is operating in a noisy environment, an optional capacitor, CBIAS can be added to bypass the internal 1.5V bias generator. CBIAS should be limited to a maximum of 0.001µF.

$$COUT\,(MAX) = \frac{CT}{I_{CH} \bullet RL \bullet \ell_n\left(1 - \frac{VIN}{I_{MAX} \bullet RL}\right)} \quad (6)$$

$$COUT\,(MAX) = \frac{CT}{\left[\frac{(V_{IN} - V_{PL})^2}{2 \bullet R_{PL} \bullet V_{IN}} + I_{CH}\right] \bullet \left[-RL \bullet \ell n\left(1 - \frac{V_{IN}}{I_{MAX} \bullet RL}\right)\right]} \quad (7)$$

Table I: List of Materials

Designator	Description	Manufacturer/Dist.	Part Number
C1, C2	0.1µF, Ceramic capacitor, 1206 SMD	Digikey	PCC104BCT-ND
CBIAS	*optional		
CINA, CINB	100µF, 16V, Tantalum capacitor, 7343 SMD	AVX	TAJD107M016
COUTA	10µF, 20V, Tantalum capacitor, 3528 SMD	AVX	TAJB106K020
COUTB	*optional		
CSS	*optional		
CT	0.01µF, Ceramic capacitor, 1206 SMD	Digikey	PCC103BCT-ND
D1	LED, red, 1206 SMD	Digikey	LU60351CT-ND
R1	5k, Metal film resistor, 1206 SMD	Digikey	P4.99KFCT-ND
R2	100k, Metal film resistor, 1206 SMD	Digikey	P100KFCT-ND
R3	150Ω, Metal film resistor, 1206 SMD	Digikey	P150FCT-ND
RPL	10k, Metal film resistor, 1206 SMD	Digikey	P10.0KFCT-ND
RSENSE	0.01Ω, 1W, Metal film resistor, 2512 SMD	IRC	LR2512-01-FTR
SW1, SW2	Right. angle, SPDT slide switch	Digikey	CKN5006
SW3, SW4, SW5	Miniature SPDT slide switch	Newark	52F516 switch
TB1, TB2	Terminal block	Mouser	506-2SV-02
U1	Hot Swap Power Manager	Unitrode	UCC3919PW
U2	N-channel MOSFET	International Rectifier	IRF7413

SAFETY RECOMMENDATIONS

The UCC3919 is designed to provide protection against over current situations, but since semiconductors can ultimately fail short, this circuit may require a fuse or electro-mechanical circuit breaker in series as back-up protection.

For complete details about the operation of the UCC3919 Hot Swap Power Manager, please refer to the UCC3919 Data Sheet and UCC3919 Hot Swap Power Manager Application Note.

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Design Note

UCC3917 Positive Floating Hot Swap Power Manager Evaluation Kit, Schematic and List of Materials

By Dave Olson

INTRODUCTION

The UCC3917 evaluation kit allows the designer to evaluate the performance of the UCC3917 Positive Floating Hot Swap Power Manager (HSPM) in a typical application setting. Component selection for the UCC3917 Evaluation Kit is for operation at 28Vdc, 1A. Operation at other voltages/currents may be accomplished by proper component selection and replacement. The schematic for the evaluation kit is shown in Fig. 1. The Bill of Materials with component ratings is specified in Table 1.

UCC3917 Features

- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Precision Fault Threshold
- Internal Charge Pump for Driving External NMOS Device
- Programmable Average Power Limiting
- Fault Output
- Programmable Fault Mode - Latch or Retry
- Programmable Fault Timer
- Shutdown Control
- Undervoltage Lockout
- No maximum voltage limitation

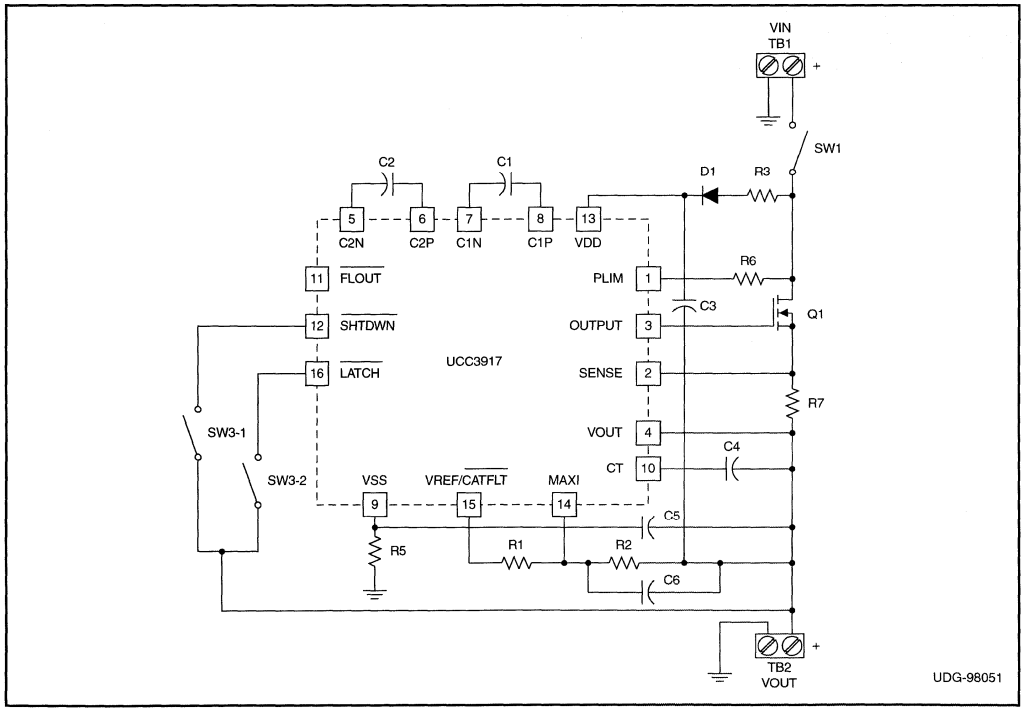

Figure 1. UCC3917 evaluation kit schematic 28V/1A.

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Switch Functions

SW1: Switch SW1 allows the designer to evaluate the performance of the UCC3917 when residing on an adapter card. Closing SW1 after input power is applied to the board simulates hot insertion into a backplane.

SW2: Omitted

SW3: Switch SW3-1 controls the SHTDWN pin of the UCC3917. In the OFF position, the switch pulls the SHTDWN pin to VOUT. In the ON position, the SHTDWN pin is left open. SW3-2 is used to program the fault-handling mode of the UCC3917. In the OFF position, the LATCH pin will be pulled low to VOUT, placing the UCC3917 in the latch mode of operation during a fault. In the ON position, SW3-2 allows LATCH to float high, thus putting the UCC3917 in the hiccup mode during a fault condition.

Programming the Maximum Sourcing Current Pin, MAXI

The maximum sourcing current level, the current level at which the output looks like a constant current source, is equal to the voltage at the MAXI pin divided by the sense resistor R7. MAXI is derived using a voltage divider from the internally regulated voltage VREF/$\overline{\text{CATFLT}}$ to VOUT. If desired, placing a capacitor on MAXI with respect to VOUT can program a controlled current slew rate (soft start). The evaluation kit is designed for a maximum sourcing current of 2A. Please see the Bill of Materials for respective resistor values. There is also a spare footprint for an optional soft start capacitor. The maximum sourcing capability is defined by:

$$I_{MAX} = \frac{V_{MAXI}}{R7} \quad (1)$$

where

I_{MAX} = maximum sourcing current desired (A)

R7 = sense resistor (Ω)

V_{MAXI} = voltage at MAXI with respect to VOUT (V)

The voltage at MAXI with respect to VOUT is defined by:

$$V_{MAXI} = \frac{R2}{R2 + R1} \bullet V_{REF} \quad (2)$$

where

V_{REF} = Regulated voltage at VREF/$\overline{\text{CATFLT}}$ (V)

R1 = Resistance from VREF/$\overline{\text{CATFLT}}$ to MAXI (Ω)

R2 = Resistance from MAXI to VOUT (Ω)

Programming the Fault Timer

The fault timer starts when the load current increases beyond the fault current, I_{FAULT}, threshold. The I_{FAULT} threshold is defined as:

$$I_{FAULT} = \frac{50mV}{R7} \quad (3)$$

where

I_{FAULT} = The fault current threshold (A)

R7 = The sense resistor value (Ω)

The fault current threshold for the UCC3917 evaluation board is set for 1A (R7 = 0.05Ω). Once the load current increases beyond the fault current threshold, the fault timer starts. The fault timer consists of a internal constant current source charging an external cap C4. Once the voltage on C4 reaches the 2.5V, an internal comparator trips and signals a fault condition. The gate drive to the external FET is disabled and the IC either latches off or enters its hiccup mode of operation (refer to the Switch Functions section for more details on programming latch mode versus hiccup mode). The internal current source charges C4 at a nominal rate of 50μA. C4 must be selected to allow enough time for the output capacitance to charge. The fault time, the time required to charge C4 to the fault comparator's threshold, is defined as:

$$T_{FAULT} = \frac{C4 \bullet \Delta V}{I_{CH}} \quad (4)$$

where

T_{FAULT} = time required to charge C4 to the fault threshold (sec)

C4 = the external capacitor on the CT pin (F)

ΔV = the fault comparator threshold (2.5V for latch mode: 2.0V for hiccup mode)

I_{CH} = internal charge current (A)

The rate at which the total output capacitance can be charged is dependent on the maximum output current available and the nature of the load. The fault time, T_{FAULT}, must be greater than the time required to charge any load capacitance. Please refer to the UCC3917 data sheet, *Selecting Minimum Timing Capacitance*, for more detailed information.

Programming the Average Power Dissipation of the External FET, PLIM

During the hiccup mode of operation, mentioned in the previous section on programming the fault timer, it is necessary to limit the average power dissipated in the external MOSFET. The hiccup mode of operation typically retries the output at a 3% duty cycle. The MOSFET will be turned on for the duration of the programmed fault time and if the fault is still present will shut down for an extended period of time. The duty cycle is defined as:

$$DutyCycle = \frac{1.5\mu A}{I_{PL} + 50\mu A} \quad (5)$$

where,

50µA = CT charging current

1.5µA = CT discharge current

I_{PL} = charge current provided by R6 (A)

Under normal operation I_{PL}=0, however, even operation at 3% duty cycle can result in substantial power dissipation in the external MOSFET. The power dissipated in the MOSFET is defined as:

$$P_{DISS} = V_{FET} \bullet I_{MAX} \bullet DutyCycle \ W \quad (6)$$

where

V_{FET} = the voltage across the FET, VINV–OUT, (V)

IMAX = the maximum sourcing current (A)

DutyCycle = operating duty cycle

The average power dissipation in the FET when incorporating the power limit function is defined as:

$$P_{FET(avg)} = I_{MAX} \bullet 1.5\mu A \bullet R6 \ W \quad (7)$$

or solving for R6,

$$R6 = \frac{P_{FET(avg)}}{I_{MAX} \bullet 1.5\mu A} \ \Omega \quad (8)$$

The UCC3917 evaluation board is populated with R6=200K. The average power dissipated in the FET, $P_{FET(avg)}$, during a fault condition should be ~0.3W. Please refer to the UCC3917 for more detailed information on R6 and controlling $P_{FET(avg)}$.

Selection Criteria for Other External Components

Because the UCC3917 derives its own operating voltage through a charge pump supplied by IDD, it is necessary for IDD to provide ~5mA of current to keep the charge pump operating. During startup, this current will be provided by input (V_{IN}) through R3, but once the IC is up and running on its own, IDD is supplied by the output (V_{OUT}). The current is returned through R5. Therefore, R3 and R5 can be determined by:

$$R3 = \frac{V_{IN} - 10V}{5mA} \ \Omega \quad (9)$$

$$R5 = \frac{V_{IN} - 5V}{5mA} \ \Omega \quad (10)$$

For applications that require wide input ranges it may be difficult to size R3 and R5 to provide adequate current over the whole operating range. For the wide input ranges, R3 and R5 can be replaced with constant current regulator diodes (1N5314). ***Please Note: IDD should not be allowed to exceed 10mA.***

External Input Capacitors: Excess source impedance may adversely affect operation of the Linear Current Amplifier control loop, resulting in oscillation when operating at the maximum sourcing current. Decoupling the evaluation board's input from the source impedance using low ESR tantalum or aluminum electrolytic capacitors can eliminate this oscillation. The capacitors should be placed at the input connector of the board.

Table 1. UCC3917 evaluation kit bill of materials.

Designator	Description	Part Value	Manufacturer	Part Number
C1, C2, C3, C5	X7R, Ceramic, 1206	0.1µF	Panasonic/Digi-Key	PCC104BCT-ND
C4	Tantalum, 50V, Case E/1206	1.0µF	Sprague	194D105X0050E2
C6	Case E/1206 Dual Footprint			Provisional
D1	100V, 1A, Rectifier		Digi-Key	DL4002DICT-ND
Q1	IRF530NS		IR/Newark	IRF530NS
R1	0.1W, 1%, 0805	100kΩ	Panasonic/Digi-key	P100KDCT-ND
R2	0.1W, 1%, 0805	2.0kΩ	Panasonic/Digi-key	P2.0KDCT-ND
R3	0.25W, 5%, 1210	3.6kΩ	Panasonic/Digi-key	P3.6KVCT-ND
R5	0.25W, 5%, 1210	4.7kΩ	Panasonic/Digi-key	P4.7KVCT-ND
R6	0.1W, 1%, 0805	200kΩ	Panasonic/Digi-key	P200KDCT-ND
R7	1W, 1%, 2512	0.05Ω	Dale/Newark	01F1551
SW1	Slide Switch	28Vdc, 3A	C&K/Digi-key	CKN5006-ND
SW3	Dip Switch , 2 pos		C&K/Digi-key	CKN3001-ND
TB1,TB2	Terminal Block, 2 pole		AUGAT/RDI /Mouser	506-2SV-02
U1	HSPM, SOIC-16		Unitrode	UCC3917D

Safety Considerations

Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety agency requires a redundant safety device such as a fuse, it should be placed in series with the power MOSFET device. In addition to providing the hot swap benefits of the device, the UCC3917 will prevent the fuse from blowing for virtually all fault conditions increasing system reliability and reducing maintenance cost.

For further information, consult the UCC3917 Data Sheet or contact a local Unitrode Representative or Field Applications Engineer at (603) 424-2410.

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UCC3912 INTEGRATED ELECTRONIC CIRCUIT BREAKER IC FOR HOT-SWAP AND POWER MANAGEMENT APPLICATIONS

by Dave Zendzian
Applications Engineer

ABSTRACT

This application note describes the design and performance characteristics of the UCC3912 Electronic Circuit Breaker. The practical aspects of applying the circuit breaker are discussed as well as its performance compared to existing technologies. The UCC3912 integrates a power MOSFET with all of the necessary control and housekeeping functions including current limiting, short circuit protection, and auto recovery capabilities. The performance of the circuit breaker is compared to PolySwitches® and conventional fuses in both hot swap and short circuit applications.

INTRODUCTION

Today's design engineers are faced with a variety of choices when selecting protection devices to meet their circuit or system's design requirements. Fuses, positive temperature coefficient (PTC) resistors, and electromechanical circuit breakers represent only a sampling of the technologies available to meet their needs. Each of these devices provides a different degree of security, ranging from simple short circuit protection to devices which offer active current limiting and remotely resettable operation.

Fuses, while providing an inexpensive solution, fall short of many of the protection requirements imposed on modern electronic equipment. Figure 1 illustrates the protection capability of two general fuse categories; fast-acting and slow-blow. Although both devices provide gross short circuit protection, even the fastest devices react on the order of milliseconds, passing currents up to 500% of their rated value. In addition, fuses, by their very nature, have to be physically replaced following an overload condition. This increases the equipment's down time along with the chance of an incorrect device being installed, thereby reducing overall system reliability.

PTC resistors, on the other hand, eliminate the need for human intervention by providing resettable overcurrent protection. However, because they are actuated by the heating effect of an overcurrent load, their reaction time is limited to several milliseconds. This results in output currents several times their steady state rating. Figure 2 illustrates typical "time to trip" data for polymeric PTC resistors.

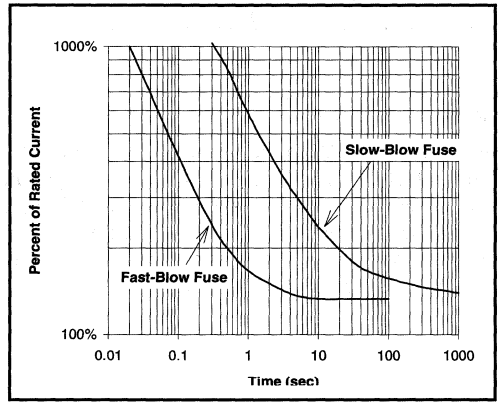

Figure 1. Relation of Percent of Rated Current to Fuse Blowing Time.

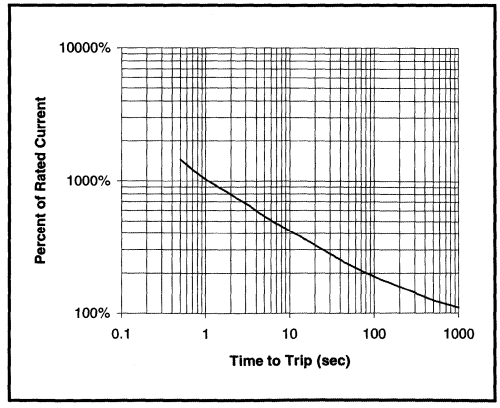

Figure 2. Relation of Percent of Rated Current to Blowing Time.

The UCC3912 Electronic Circuit Breaker offers a new, integrated solution to the problem of circuit protection and power management. Each of the drawbacks associated with existing technologies are addressed in the UCC3912 design. In addition, the UCC3912 provides logic level load control for power management applications. This note describes the features and performance of the UCC3912 as compared to other available protection techniques. In particular, hot swap, power management, and short circuit protection applications are addressed in detail.

HOT SWAPPING

The term hot swap refers to the system requirement that submodules be swapped out upon failure or system modification without removing power to the hardware. Design of modern computer systems, disk arrays, network hubs and communication switches require modules to be hot swapped while maintaining the integrity of the powered and operating system. This requirement allows the hardware to maintain operation, increasing the system's performance and reliability.

Implementing the hot swap requirement imposes several design constraints upon the equipment's power system. In order for the hardware to maintain error free operation during the installation or removal of a submodule, the 5 volt power bus must not drop below a minimum voltage of 4.5V. Voltages below 4.5V can disrupt logic levels, causing an indeterminate number of failures including data corruption and logic lockups. This ultimately reduces system reliability and data integrity.

The potential for glitching the power bus exists whenever an unpowered module is inserted into an operational system. Virtually all modules possess some amount of onboard bus capacitance which serves to filter and maintain power quality once the board becomes operational. However, these very same capacitors require an initial charging current in order to bring their voltage up to the same level as the system's power supply. The only factors limiting the magnitude of this current is the equivalent series resistance (ESR) of the capacitors themselves and the impedance of the interconnect between the module and the rest of the system. Unfortunately, the better the capacitors are at serving their purpose of filtering the bus, the lower their ESR. As a result, the initial inrush current during the hot swap can become excessively high.

Figure 3 illustrates the inrush current and corresponding voltage glitch when a load of 2A and 120µF is switched onto a 5V power bus. The 120µF of load capacitance consisted of a solid tantalum, surface mount style capacitor (Sprague #595D127X9020R2T) with a typical ESR of 0.25Ω at 100kHz. The power bus was bypassed with 240µF of the same style capacitor. As the figure illustrates, the inrush current reaches a maximum value of approximately 27A, resulting in a 1V glitch on the power bus. This exceeds the 4.5V limit by 500mV causing the supply to drop to 4.0V! In addition to causing the voltage glitch, the excessive inrush current can also result in arcing between connector pins and excessive heating of the load capacitance. Each of these effects shortens the life of the component, ultimately reducing system reliability.

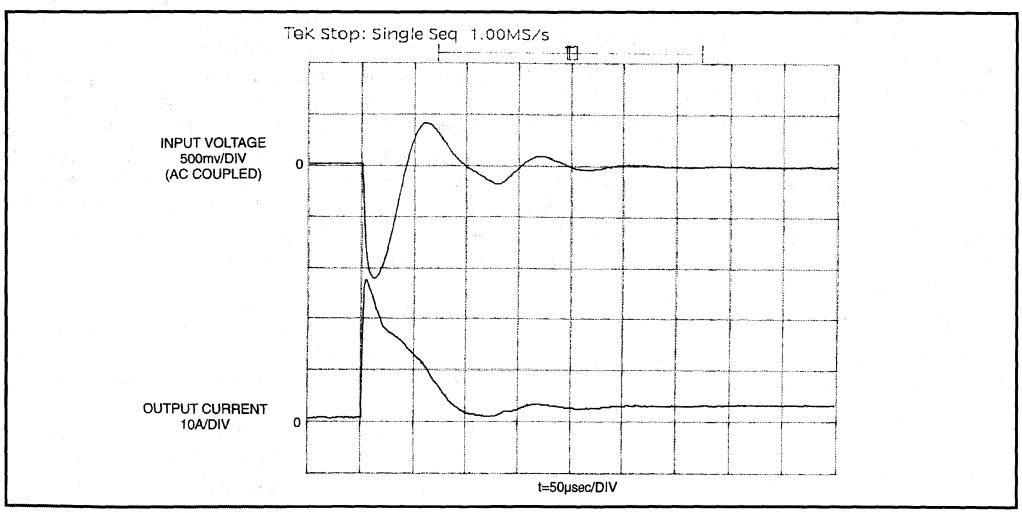

Figure 3. Inrush Current and Corresponding Voltage Glitch for a 2A, 120µF Load.

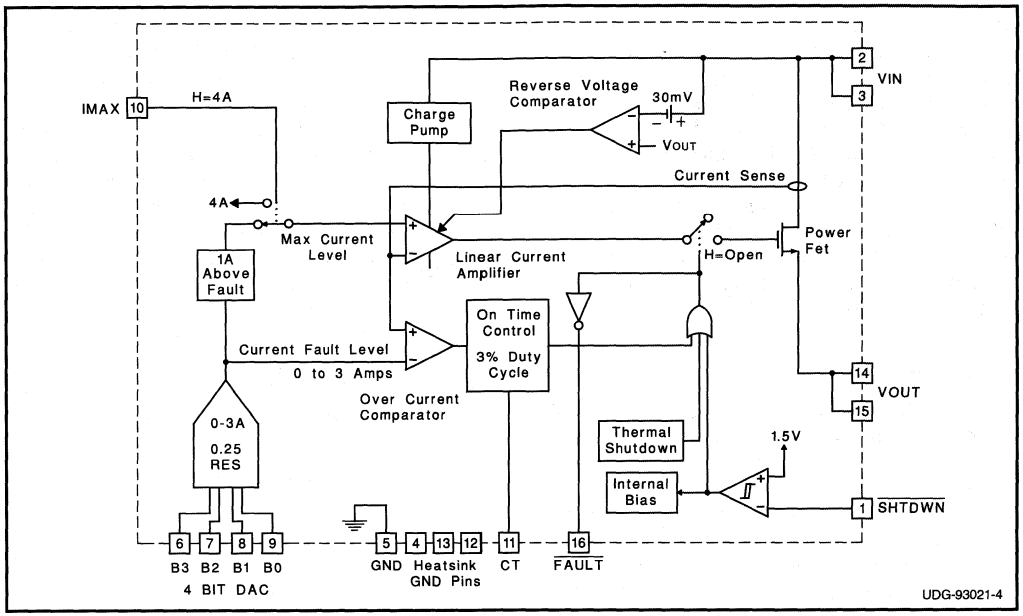

Figure 4. UCC3912 Electronic Circuit Breaker Block Diagram

THE UCC3912 ELECTRONIC CIRCUIT BREAKER

In its most rudimentary form, a circuit breaker, whether electromechanical or electronic, protects a circuit from excessive current flow. Electromechanical devices accomplish this by opening a set of contacts when the current exceeds a specified level. These types of breakers usually latch off during a fault and therefore need to be manually reset once the current falls below a reasonable value. An electronic circuit breaker, on the other hand, provides protection through the use of a power transistor. By monitoring the output current through a current shunt, the transistor can be biased "on" or "off" based upon whether or not a predetermined trip current has been exceeded.

The UCC3912 is an electronic circuit breaker IC designed to provide power management and hot swap capability in addition to its basic circuit breaker function. Performance features of the UCC3912 include:

- Integrated 0.15Ω power MOSFET
- Switchmode short circuit protection
- Automatic short circuit recovery
- Digitally programmable 4-bit maximum current limit
- Unidirectional current flow
- SMT power package
- Fault indicator output
- Low power "sleep" mode
- Thermal shutdown
- Low part count implementation

The block diagram of the UCC3912 is shown in Figure 4. Under normal operating conditions the integrated N-channel MOSFET is biased "on" using the internal charge pump to drive the gate. Output current is sensed using a mirrored MOSFET and is compared to an adjustable trip level set by the 4-bit DAC input. When the output current exceeds the trip level, the fault timer begins to charge the timing capacitor, CT, with a current of 36μA. If the output current does not fall below the trip level by the time the capacitor charges to 1.5V, the output is switched off and the capacitor is discharged with a current of 1.2μA. Once the capacitor's voltage has reached 500mV, the circuit breaker attempts to return power to the load. At this point the timer cycle will repeat as long as the fault is present, resulting in an output duty cycle of 3%.

Figure 5 illustrates the cyclical retry of the UCC3912 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that the capacitor is completely discharged and must initially charge to the reset threshold of 0.5V. If at any time the output current reaches IMAX, the MOSFET transitions into linear mode, providing constant output current until the fault time expires. The discrete IMAX input is used to set the maximum output current to either a fixed

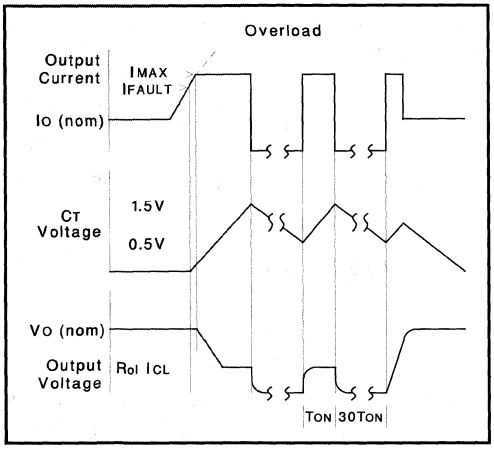

Figure 5. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3912 under Fault Conditions.

value of 4A, (logic level high), or to a value 1A above the trip current as set by the DAC inputs, (logic level low). The 4 bit DAC allows the fault current level to be programmed from 0 to 3A in 250mA increments.

Fault time duration is controlled by the value of the timing capacitor, CT, according to the following equation:

$$(1)\quad t_{FAULT} = CT \bullet \frac{\delta v}{I} = CT \bullet \frac{1.5 - 0.5}{36E - 6}$$
$$= 27.8E3 \bullet CT$$

Figure 6 provides a plot of fault time vs timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. *The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault.* If not, the charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle

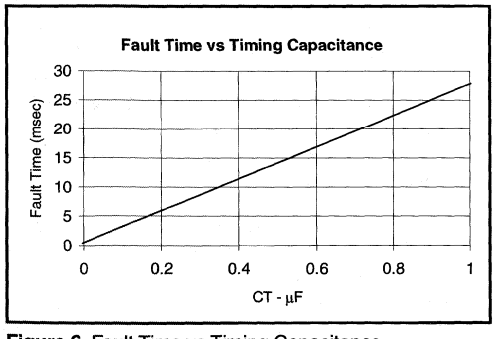

Figure 6. Fault Time vs Timing Capacitance

will then repeat, preventing the output from turning on.

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and ITRIP values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$(2)\quad t_{FAULTmin} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}}$$

The minimum timing capacitor can be calculated by substituting equation (1) for tFAULT in equation (2) and solving for CT.

$$(3)\quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

In addition to the IMAX and DAC inputs, the UCC3912 provides a fault indicator output and shutdown command. The $\overline{\text{FAULT}}$ signal is an open drain output which is active low under any condition which turns the output MOSFET "off". These conditions include under voltage lockout (UVLO), over current faults, thermal shutdown, and active shutdown as commanded by the $\overline{\text{SHTDWN}}$ input. Note that $\overline{\text{FAULT}}$ is asserted (low) during power up while the UCC3912 is in a UVLO state.

The $\overline{\text{SHTDWN}}$ command is an active low input which turns the MOSFET "off" and puts the IC into sleep mode, reducing the quiescent current to less than 5µA. The shutdown command can be used to extend the life of battery powered systems by powering down subsystems when not in use.

Unidirectional current flow is another attractive feature of UCC3912. The reverse voltage comparator senses the output voltage and turns the MOSFET "off" whenever the output voltage is less than 30mV below the input. Under light loads, the UCC3912 regulates the voltage drop until

$$(4)\quad (I_{OUT}) \bullet (R_{DSon}) \geq 30mV,$$

thus preventing false shutdowns. This effectively prevents current flow from output to input, eliminating the need for series diode protection and the associated voltage drop and power losses incurred with its use.

PRACTICAL CONSIDERATIONS

The UCC3912 is supplied in 16-pin power surface mount packages. Four ground leads are provided in order to effectively transfer heat out of the package. These pins should always be terminated to as large an area of copper as possible. Although the 3% duty cycle switchmode protection drastically minimizes power dissipation, thermal analysis

should still be performed in order to insure reliable circuit operation.

When interfacing with larger values of load capacitance, the UCC3912 fault time must be increased accordingly. While the average power remains low due to the 3% duty cycle, the power dissipation during the fault time will result in a junction temperature rise based on the thermal time constant of the system. A simplified thermal model of the system is comprised of the die, leadframe and PC board. However, for fault times less than 30msec, the effect of the leadframe and PC board can be considered negligible as their thermal time constants are on the order of 2 and 300sec respectively. A rough estimate of the transient junction temperature can then be calculated based on the following equation:

$$(5)\quad Tj(t) = P_{DISS}\left[\Theta_{DIE}\left(1 - e^{-t/\tau}\right)\right] + T_L$$

Where P_{DISS} = transient power dissipation
Θ_{DIE} = thermal resistivity between die and leadframe ≈ 4°/W
t = fault time
τ = thermal time constant of the die ≈ 30msec
T_L = steady state lead temperature

As the fault time is increased beyond 30msec, a more thorough transient thermal analysis is required. For additional information regarding thermal analysis and transient response, the reader is directed to reference (1).

In applications requiring minimum voltage losses, it is important to take the effects of PCB trace resistance into account. When passing two to three amps of current, minimum trace widths can result in enough I • R voltage drop to effect system performance. By increasing either the trace width or copper weight, these effects can be made negligible. Table I provides resistance/inch values for various trace widths of 1, 1.5, and 2 oz. copper.

Table I
PCB Trace Resistance (mΩ/inch)

Copper Wt.	Trace Width (inches)					
	0.01	0.02	0.03	0.05	0.07	0.1
1.0 oz.	48.5	24.23	16.2	9.7	6.9	4.9
1.5 oz.	38.8	19.4	12.9	7.8	5.5	3.9
2.0 oz.	24	12	8	4.8	3.4	2.4

A TYPICAL APPLICATION

In order to evaluate the performance of the UCC3912, consider a typical application consisting of a 2A maximum load current in parallel with 120µF of load capacitance. The 2A output current is accommodated by setting the UCC3912 trip current to 2.25A, using the DAC inputs. Bits B0 and B1 are grounded while bits B2 and B3 are tied to VIN. The maximum output current is configured to 1A above the trip current (3.25A) by grounding the IMAX input. The timing capacitor value must then be selected to accommodate the 120µF load capacitance:

$$(6)\quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

$$= \frac{120E-6 \bullet 5}{27.8E3 \bullet (3.25 - 2.25)} = 21.6nF$$

A 47nF capacitor was chosen in order to provide adequate margin for component and parameter tolerances. Lastly, the $\overline{SHTDWN}$ input to the UCC3912 is connected to VIN since it is not used in this example.

In actual hot swap applications, the circuit breaker function may reside on the system's backplane servicing one or more submodules, or be distributed throughout the individual submodules depending on system requirements. In order to test both of these application scenarios, a MOSFET was used to simulate a hot swap on the input and output of the UCC3912. A test load was constructed using a 120µF low ESR tantalum capacitor in parallel with a carbon power resistor, while 240µF was used to simulate the system's input bus capacitance. Output current was monitored using a noninductive 10mΩ current shunt in series with the load. Figure 7 illustrates the test setup including the UCC3912 circuit configuration.

HOT SWAP PERFORMANCE

Figure 8 illustrates the load current and input voltage waveforms, measured at points A and B in Figure 7, with and without the UCC3912. In Figure 8(a), transistor Q2 was used to perform the hot swap on the output of the UCC3912, simulating an application with the circuit breaker resident on the system backplane. In this situation the UCC3912 limits the load current to approximately 4A as compared to the 24A peak seen without the breaker! Consequently, the voltage glitch seen at the input bus capacitor is reduced from approximately 1V to less than 150mV!

Figure 8(b) illustrates the results when Q2 is used to simulate the hot swap on the input of the UCC3912. Again, the output current is controlled as both the circuit breaker and submodule receive power, providing very similar results to those of Figure 8(a).

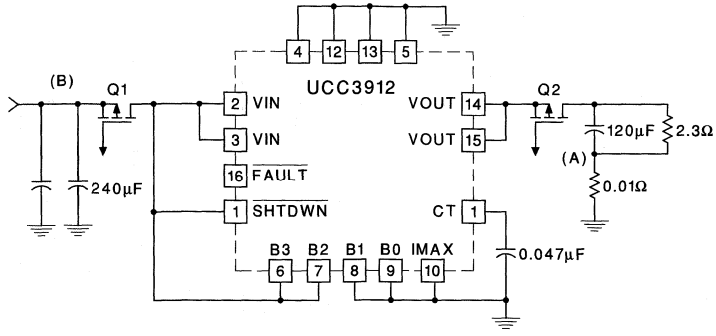

Figure 7. Typical UCC3912 Configuration and Hot Swap Test Circuit Setup.

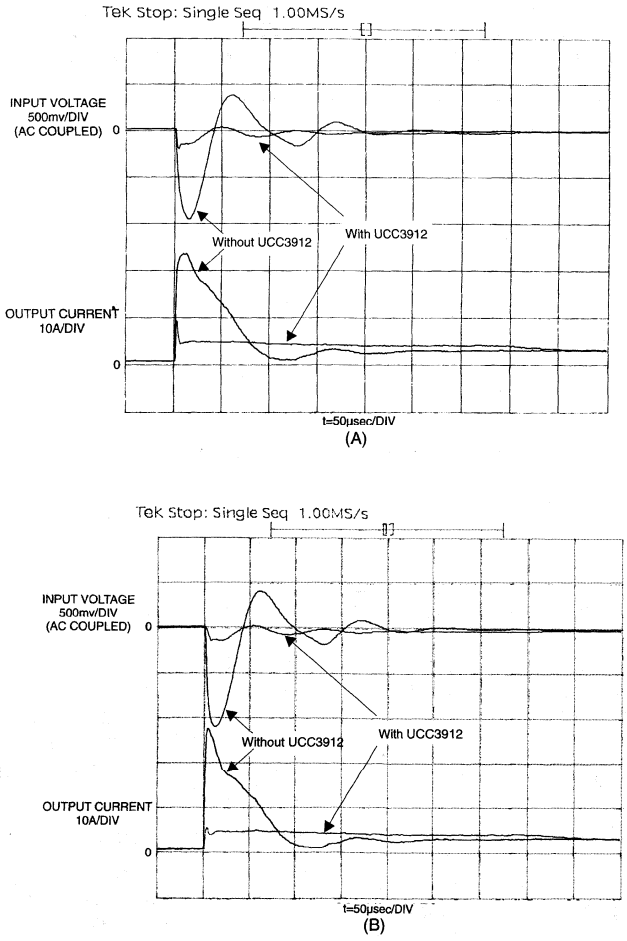

Figure 8. Hot Swap Results With and Without the UCC3912 Circuit Breaker. A) Hot Swap Performed on UCC3912 Output. B) Hot Swap Performed on UCC3912 Input.

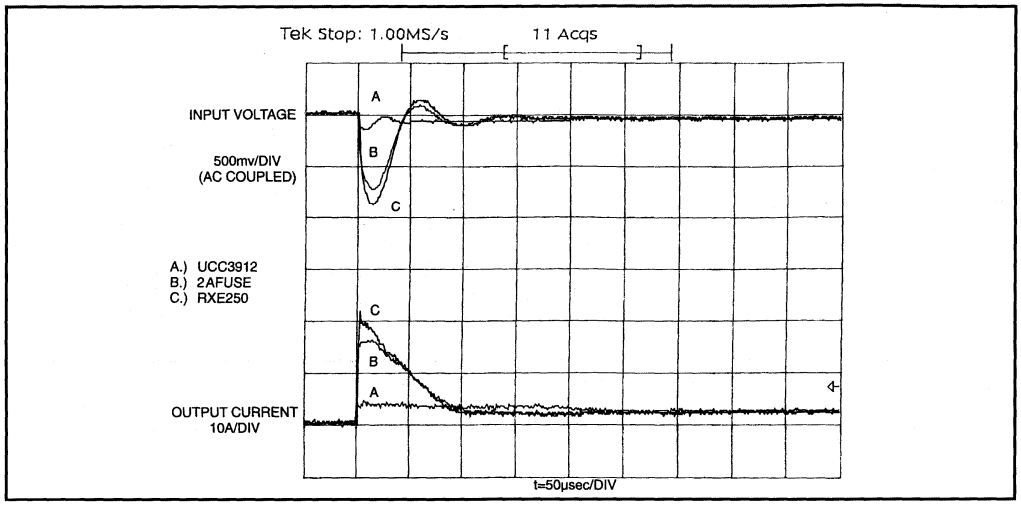

Figure 9. Hot Swap Performance Comparison Between a Fuse, PolySwitch® and the UCC3912.

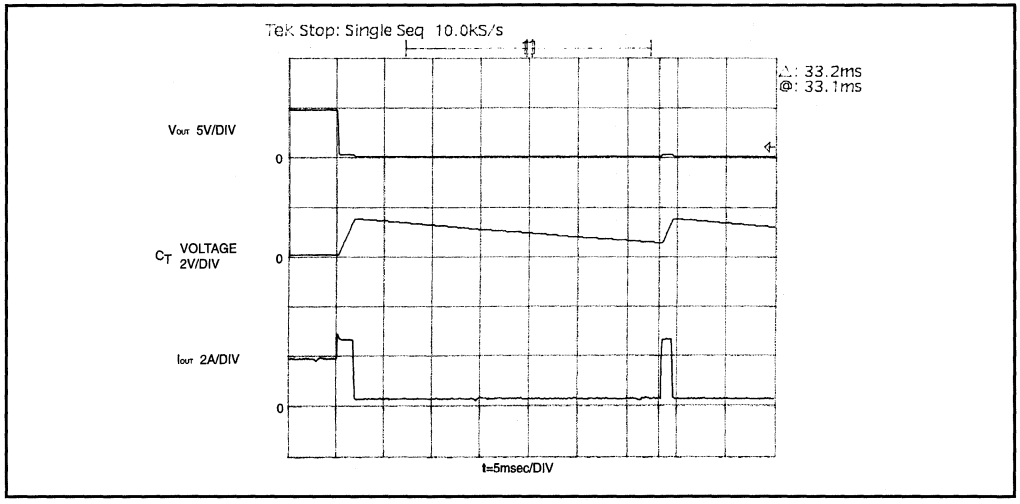

Figure 10. Short Circuit Performance of the UCC3912 Illustrating the 3% Duty Cycle Protection Technique.

Not shown in this figure is a delay of approximately 100µsec as the internal charge pump builds up gate charge for the MOSFET.

The hot swap performance of the UCC3912 was also compared to that of a fuse and PolySwitch®, two industry standard protection devices. A 2.5A PolySwitch® (RXE250) and a 2A slow-blow fuse (Littelfuse 313.002) were each substituted for the UCC3912 during a hot swap test. Figure 9 illustrates the results using the three different protection devices. Comparing the results of Figures 8 and 9, it is evident that both the fuse and PolySwitch® offer virtually no protection for transients of this speed; the current magnitudes are very close to those seen without any protection device at all. The circuit breaker, on the other hand, provides a fast transient response, keeping the current and the associated voltage transient within specification.

SHORT CIRCUIT PROTECTION

As previously described, the UCC3912 provides overcurrent and short circuit protection by modulating the output at a 3% duty cycle. During the "on" time, output current is limited to the value set by the IMAX and DAC inputs. Figure 10 illustrates the performance of the UCC3912 test circuit when a

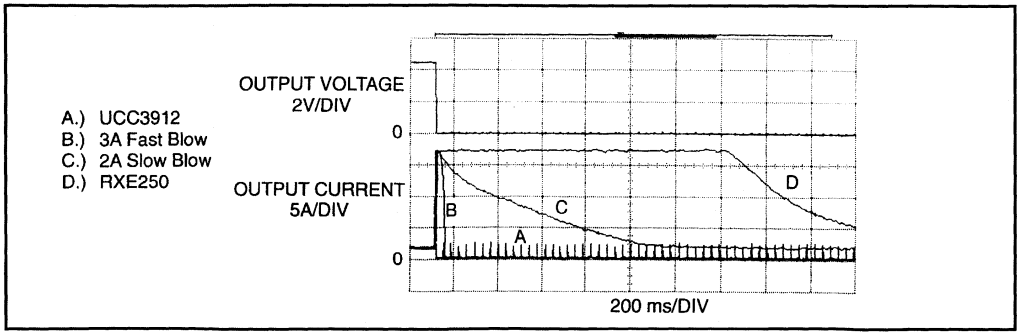

Figure 11. Short Circuit Performance Comparison of a Fuse, PolySwitch® and the UCC3912.

short-circuit is applied in place of the load. The bottom trace is the output current, modulated at a 3% duty cycle, while the center trace is the voltage across the timing capacitor. Note that the first current pulse is approximately 50% longer than subsequent pulses due to the timing capacitor initially charging from 0V.

The short circuit test was also conducted on the 2.5A PolySwitch®, 2A slow-blow fuse, and a 3A fast-acting fuse (Littelfuse 312.003). Figure 11 compares the performance of the 4 different protection techniques. The peak currents incurred with each of the fuses and the PolySwitch® reach approximately 17.5A and are limited only by the output capability of the 5V power supply. The PolySwitch® takes approximately 1.25sec before it begins to limit the current and eventually latches into high impedance mode. At this point it will remain in a high impedance state due to a sustained self heating current and will only reset after it has cooled and the fault condition has been corrected. As a result, the device requires that the input voltage be removed from the system in order to insure a circuit reset. The fuses on the other hand, respond faster than the PolySwitch®, but once blown require manual replacement before the hardware can resume operation. Table II compares the I • T and peak current characteristics of the four techniques.

Table II

Protection Device	Peak Current (Amps)	I • T (Amp-sec)
PolySwitch® RXE250	17.5	17.5
Fuse 312.003	17.5	9.75
Fuse 313.002	17.5	0.875
UCC3912	3.25	0.098

Note: 1) Peak currents are limited by power supply.
2) I • T estimated for first second of short circuit.

When compared to any of the other commonly used technologies, the performance of the UCC3912 is superior. The electronic circuit breaker responds almost immediately to a short circuit, limiting the current to 3.25A before turning off the output. The breaker then attempts to reapply power at a 3% duty cycle until the fault has been corrected. The low duty cycle, coupled with the current limiting feature keeps the power dissipation at a reasonable level, eliminating the need for extensive heating sinking. In this example the UCC3912 dissipates only 5V • 3.25A • 3% = 488mW of power during the short circuit.

POWER MANAGEMENT APPLICATIONS

In an effort to save energy, the federal government is working to impose regulations that will require electronic equipment and appliances to operate more efficiently. As an example, consider the personal computer (PC). PCs typically dissipate 100 to 200W, with an additional 150 to 350W consumed by the monitor. In order to limit the power dissipation to a recommended 30W during periods of nonusage, circuitry must be added to shutdown key components such as the monitor, high powered cache circuits and bus interfaces. The UCC3912 offers a simple solution to these types of power management applications.

The UCC3912 can be configured as a low current (<5µA) standby power switch, as shown in Figure 12. The shutdown input, $\overline{\text{SHTDWN}}$, is utilized to turn off the internal MOSFET, removing power from the load and reducing the UCC3912 quiescent current to <5µA. When reactivated by the logic command, the current limiting features of the UCC3912 allow the load circuits to resume operation without disrupting the rest of the system.

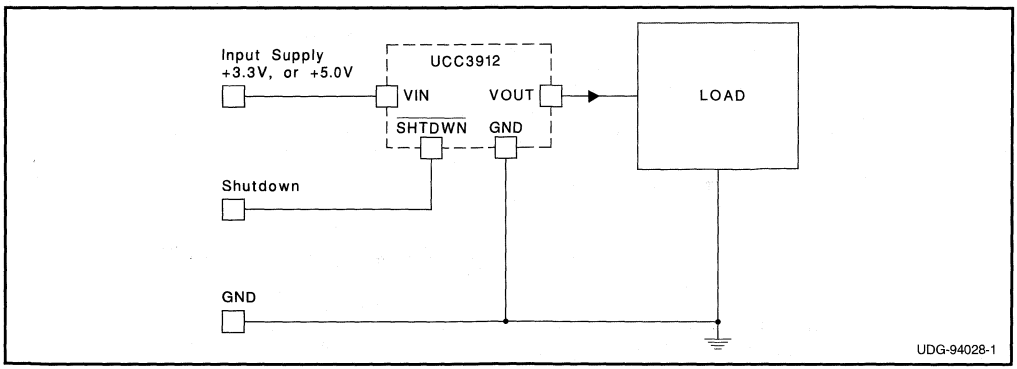

Figure 12. Low Current Standby Power Switch

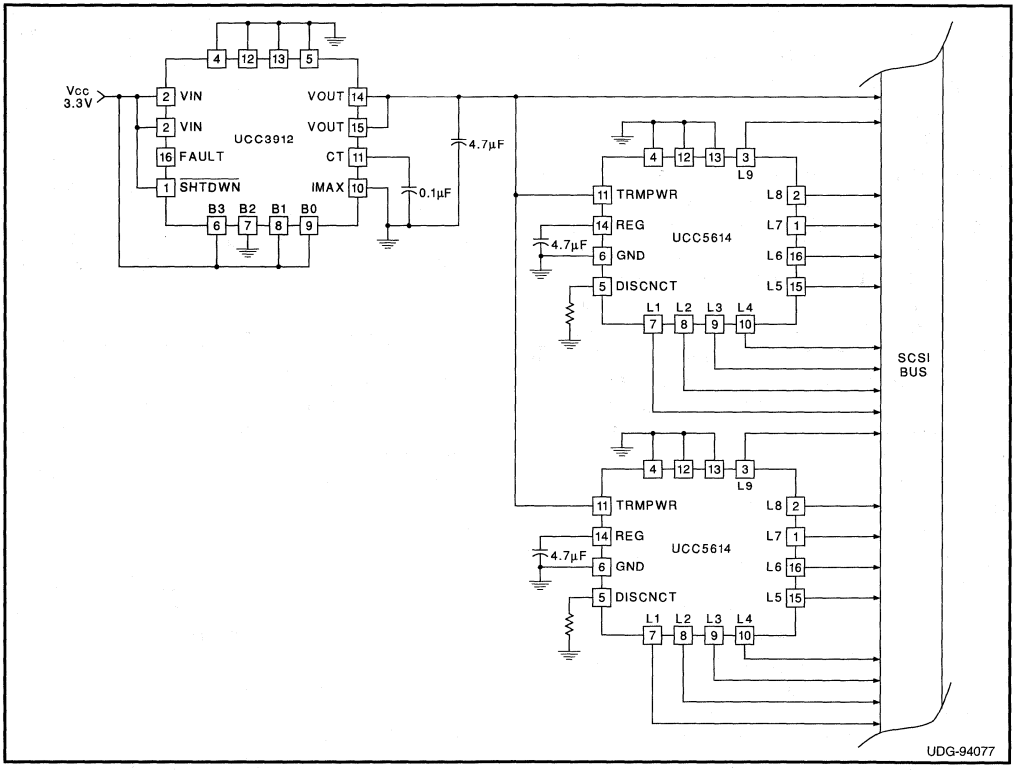

Figure 13. Typical 3.3V SCSI Application

APPLICATION CIRCUITS

The 3.3V power bus has quickly become the standard for laptop computers and other battery operated equipment. Unfortunately, SCSI standards specify an active termination voltage of 2.7V. In addition, standards require that the Termpwr source be fused and provide for unidirectional current flow. These requirements have typically forced designers to include a 5V supply in 3.3V systems - a 5%, 3.3V bus leaves only 130mV of headroom for a diode, fuse, and regulator overhead. Replacing the diode and fuse with the UCC3912 limits the voltage drop to less than 60mV while still meeting SCSI requirements. Combining the UCC3912 with a low dropout active terminator such as the UCC5614 results in a complete design. Figure 13 illustrates a typical 3.3V SCSI application.

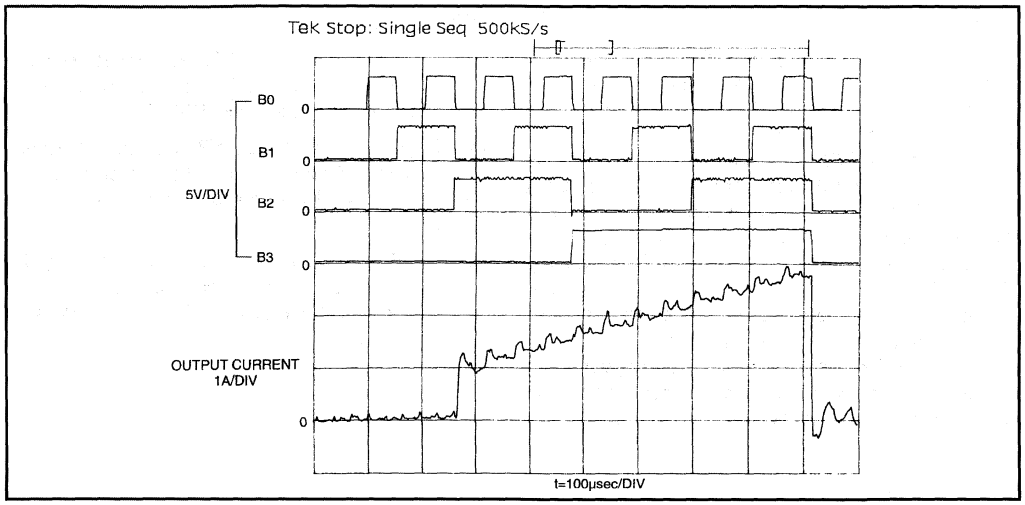

Figure 14. Controlled Current Slew Rate Using the UCC3912 4-Bit DAC.

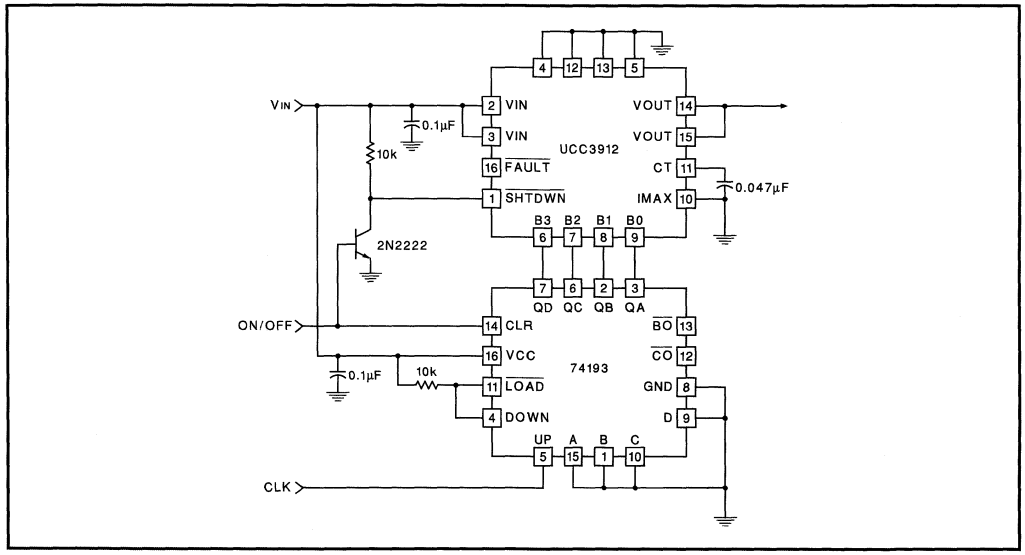

Figure 15. UCC3912 Current Control Circuit Implementation.

The UCC3912 lends itself well to more sophisticated current limiting schemes through the use of the DAC inputs. Greater control of output current slew rate can be obtained by stepping the DAC through a series of its input codes. Figure 14 illustrates the output current as the DAC inputs are controlled using the output of a 4-bit counter as shown in Figure 15. Similarly, loads such as motors often require inrush currents several times their normal running value. By using the counter in Figure 15 to count down rather than up, the motor can be quickly accelerated to speed using maximum current and then closely protected against overload.

The duty cycle protection capability of the UCC3912 can be disabled by grounding the timing capacitor input, CT. This causes the UCC3912 to remain in constant current mode during a fault condition. When operating in this manner the UCC3912 is in linear mode and will dissipate power as function of the maximum output current and differential input/output voltage. It is extremely important that adequate heatsinking is provided when operating in this configuration.

SUMMARY

As demonstrated throughout this application note, the UCC3912 provides a level of protection far superior to that offered by existing technologies. Integrating a high speed, programmable current amplifier, power MOSFET, and charge pump allows for precise control of both inrush and short circuit currents. Fast, accurate transient control helps to maintain power supply tolerance, enabling reliable hot swap implementation. In addition, preventing destructive current transients during connector mating prolongs the life of the hardware. By integrating each of these features, the UCC3912 electronic circuit breaker offers a new and complete solution to power management, hot swap, and short circuit requirements.

REFERENCES

[1] J. O'Connor, "Thermal Characteristics of Surface Mount Packages", Unitrode Product and Applications Handbook, 1993-94.

[2] Raychem, PolySwitch® R-Line Circuit Protectors, RXE Product Family, Manufacturers Data Sheet, Raychem Corporation, Menlo Park, CA, 1993.

[3] Littelfuse, Electromechanical Devices and Circuit Protection Components, Manufacturers Catalog No. 20, Littelfuse Tracor, Des Plaines, IL, 1985.

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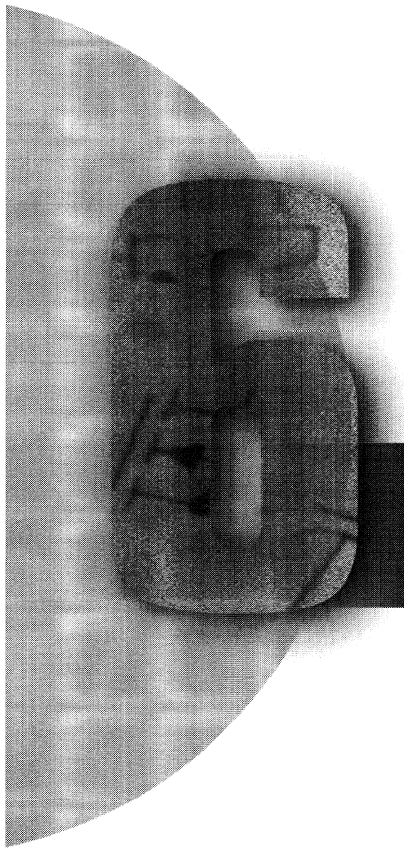

Drivers/Receivers Transceivers

Drivers / Receivers / Transceivers

Interface Drivers, Receivers	UNITRODE PART NUMBER				
	UC5170C	UC5171	UC5172	UC5180C	UC5181C
Drivers	8	8	8		
Receivers				8	8
Power	±10V	±10V	±10V	+5V	+5V
EIA232 / V.28	Y	Y	Y	Y	Y
EIA423 / V.10	Y	Y	Y	Y	Y
EIA422 / V.11	N	N	N	Y	Y
V.35	N	N	N	Y	Y
Appletalk	N	N	N	N	Y
Page Number	IF/6-3	IF/6-7	IF/6-11	IF/6-15	IF/6-18

Interface Transceivers	UNITRODE PART NUMBER				
	UC5350	UC5351+			
Drivers	1	1			
Receivers	1	1			
Power	+5V	+5V to 24V			
Control Area Network	Y	Y			
Device Net	Y	Y			
SDS	Y	Y			
Page Number	IF/6-21	IF/6-27			

+ New Product


UNITRODE

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Octal Line Driver

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards EIA232E/V.28, EIA423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection

DESCRIPTION

The UC5170C is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all eight drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is easily accomplished by taking the select pins (MS+ and MS-) to ground for low output mode (EIA232E/V.28 and EIA423A/V.10) or to their respective supplies for high mode (EIA232E/V.28). High mode should only by used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . -15V
PLCC Power Dissipation, T_A = 25°C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) . . . . . 1250 mW
Input Voltage . . . . . -1.5V to +7V
Output Voltage . . . . . -12V to +12V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . -65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of packages.

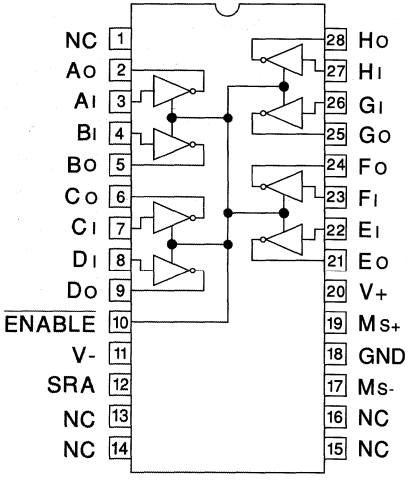
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
		HIGH	LOW
$\overline{EN}$	DATA	EIA-232E[2]	EIA423A+EIA232E
0	0	(V+)-3V	5V to 6V
0	1	(V-)-3V	-5V to -6V
1	X	High Z	High Z

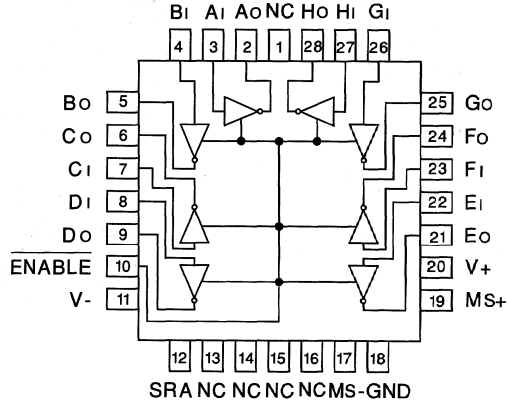
Note 2: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



6

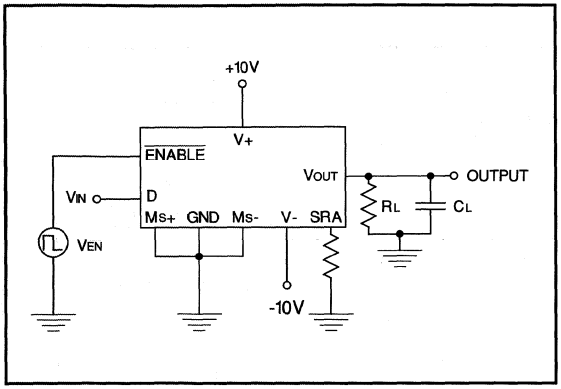
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $R_{SRA} = +10k$, $T_A = T_J$.

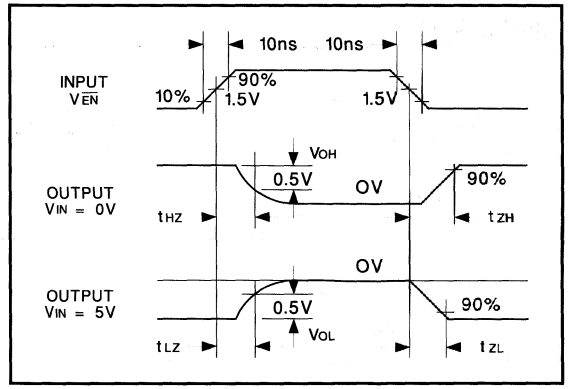
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			9		15	V
V- Range			-9		-15	V
V+ Supply Current	I_+	R_L = Infinite $\overline{En}$ = 0V		25	42	mA
V- Supply Current	I_-	R_L = Infinite $\overline{En}$ = 0V		-23	-42	mA
INPUTS						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA		-1.1	-1.8	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	-200	-8.0		µA
OUTPUTS						
High Level (Low Mode) Output Voltage	V_{OH}	V_{IN} = 0.8V R_L = Inf.	5.0	5.3	6.0	V
(EIA423A/V.10, EIA232E/V.28)		$\overline{En}$ = 0.8V R_L = 3k	5.0	5.3	6.0	V
		R_L = 450	4.5	5.2	6.0	V
Low Level (Low Mode) Output Voltage	V_{OL}	V_{IN} = 2.0V R_L = Inf.	-5.0	-5.3	-6.0	V
(EIA423A/V.10,EIA232E/V.28)		$\overline{En}$ = 0.8V R_L = 3k	-5.0	-5.3	-6.0	V
		R_L = 450	-4.5	-5.2	-6.0	V
Output Balance (EIA423A/V.10)	V_{BAL}	R_L = 450 $V_{OH} - V_{OL} = V_{BAL}$		0.2	0.4	V
High Level (High Mode) Output Voltage	V_{OH}	V_{IN} = 0.8V R_L = Inf., M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
(EIA232E/V.28)		$\overline{En}$ = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
Low Level (High Mode) Output Voltage	V_{OL}	V_{IN} = 2.0V R_L = Inf., M_{S+} = V+, M_{S-} =V-	-7.0	-7.7	-10	V
(EIA232E, V.28)		En = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	-7.0	-7.7	-10	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, V+ = 15V, V- = -15V	-100		100	µA
Short-Circuit Current	I_{OS}	V_{IN} = 0V, $\overline{En}$ = 0V	25	50		mA
		V_{IN} = 5V, $\overline{En}$ = 0V	25	40		mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $T_A = T_J$.

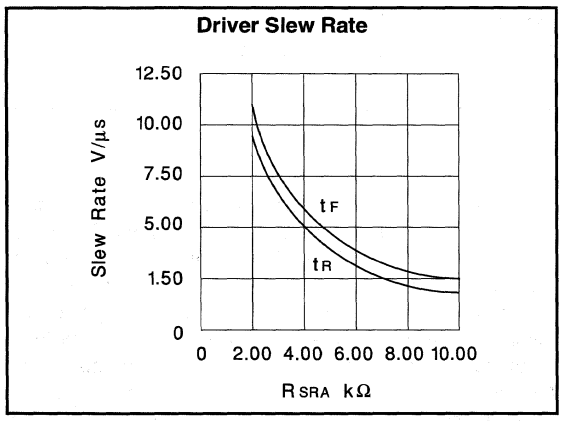
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
High Impedance	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
Output	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

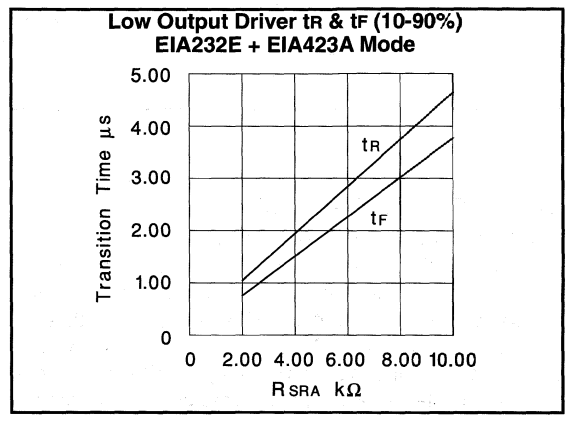
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATION INFORMATION

Slew Rate Programming

Slew rate for the UC5170C is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \ (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10k which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA423A +V.10. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

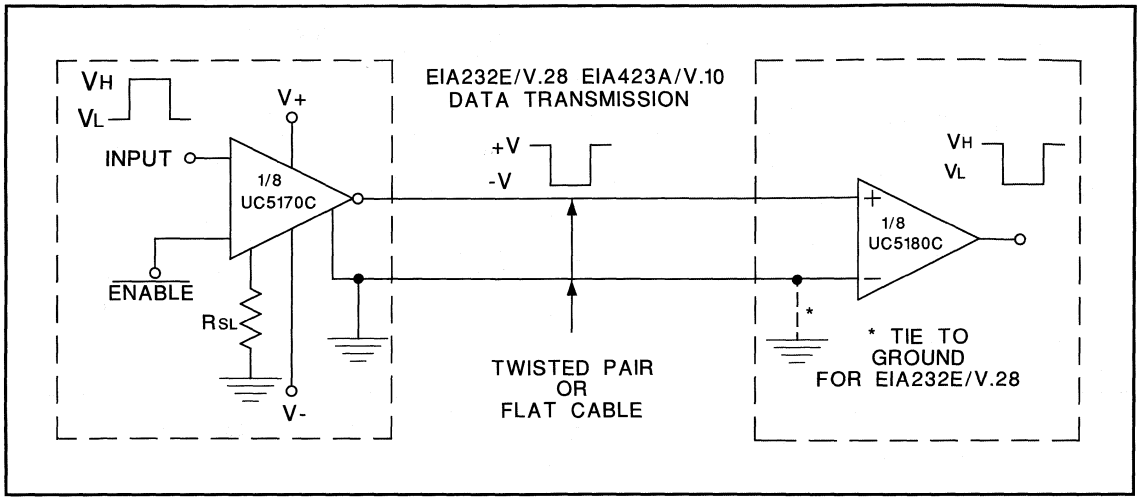
Output Voltage Programming

The UC5170C has two programmable output modes, either a low voltage mode which meets EIA423A, EIA232E/V.28/V.10 specifications, or the high output mode which meets the EIA232E, V.28 specifications.

The high output mode provides greater output swings, minimum of 3V below and supply rails for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supplies, MS+ to V+ and MS- to V-.

The low output mode provides a controlled output swing and is accomplished by connecting both mode select pins to ground.

APPLICATIONS



SPECIFIC LAYOUT NOTES

The UC5170C layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5170C on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5170C can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,00 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5170C is P6KEIOCA.

*Transzorb is a trademark of General Semiconductor Industries.

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Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Digital Selection of High Mode EIA232E/CCITT V.28 only, and Low Mode EIA232E/V.28 & EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins

DESCRIPTION

The UC5171 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is accomplished by the select pin Ms logic "low" for low output mode (EIA232E/V.28 & EIA423A/V.10) or pin Ms logic "high" for high mode (EIA232E/V.28). High mode should only be used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) ..... -15V
PLCC Power Dissipation, T_A = 25°C (Note 2) ..... 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) ..... 1250 mW
Input Voltage ..... -1.5V to +7V
Output Voltage ..... -12V to +12V
Slew Rate Resistor ..... 2k to 10kΩ
Storage Temperature ..... -65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

FUNCTIONAL TABLE

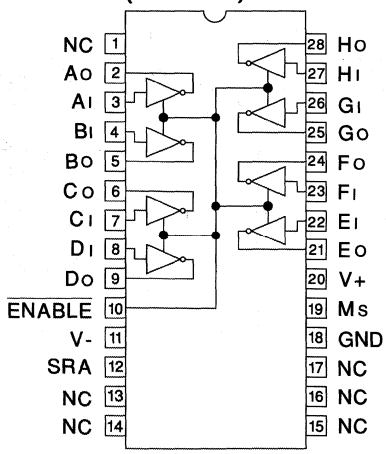
INPUTS		OUTPUTS	
$\overline{EN}$	DATA	EIA-232E(3)	EIA-232E/EIA-423A
0	0	(V+)-3V	5V to 6V
0	1	(V-)+3V	-5V to -6V
1	X	High Z	High Z

Note 3: Minimum output swings.

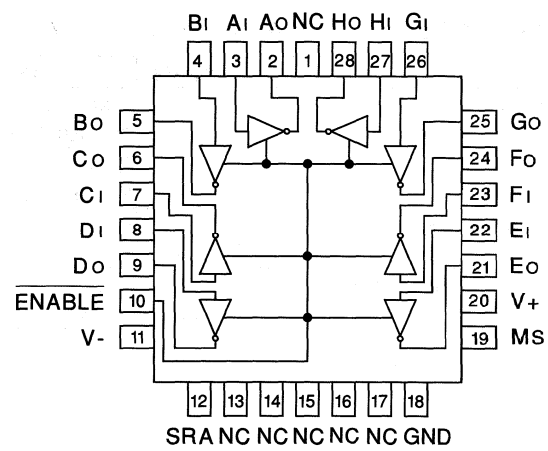
6

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS:

Unless otherwise stated these specifications hold for $|V+| = |V-| = +10V$, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $R_{SRA} = +10k$, $T_A = T_J$.

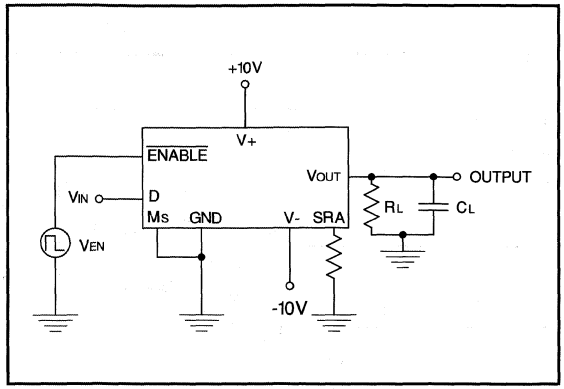
PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-15		-9	V
V+ Supply Current	I+	R_L = Infinite $\overline{En}$ = 0V			25	42	mA
V- Supply Current	I-	R_L = Infinite $\overline{En}$ = 0V		-42	-23		mA
INPUTS							
High Level Input Voltage	V_{IH}			2.0			V
Low Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA		-1.8	-1.1		V
High Level Input Current	I_{IH}	V_{IH} = 2.4V			0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-200	-8.0		µA
OUTPUTS							
High Level	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA423A)			R_L = 450	4.5	5.2	6.0	V
Low Level	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-6.0	-5.3	-5.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-6.0	-5.3	-5.0	V
(EIA423A)			R_L = 450	-6.0	-5.2	-4.5	V
Output Balance (EIA423A)	V_{BAL}	R_L = 450	$V_{OH} + V_{OL} = V_{BAL}$		0.2	0.4	V
High Level	V_{OH}	V_{IN} = 0.8V, M_S = 2.0V	R_L = Inf.	7.0	7.6	10	V
Output Voltage (EIA232E)		$\overline{En}$ = 0.8V	R_L = 3k	7.0	7.6	10	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V, M_S = 2.0V	R_L = Inf.	-10	-7.7	-7.0	V
(EIA232E)		En = 0.8V	R_L = 3k	-10	-7.7	-7.0	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, M_S = 2.0V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	50		mA
			V_{IN} = 5V	25	40		mA

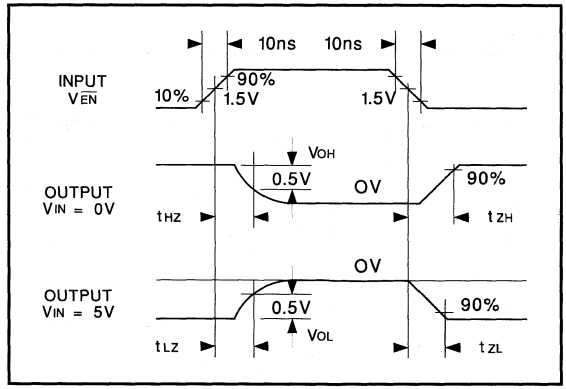
AC ELECTRICAL CHARACTERISTICS:

at $|V+| = |V-|$ = +10V, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $T_A = T_J$.

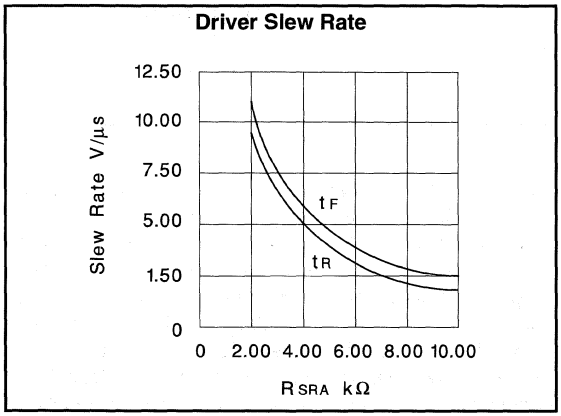
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
High Impedance	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
Output	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

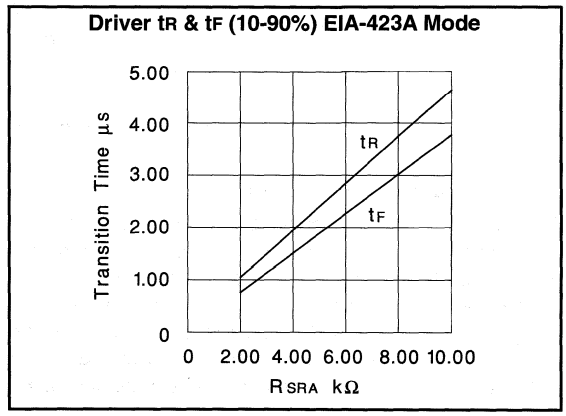
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5171 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \; (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate=300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet)=100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

Output Voltage Programming

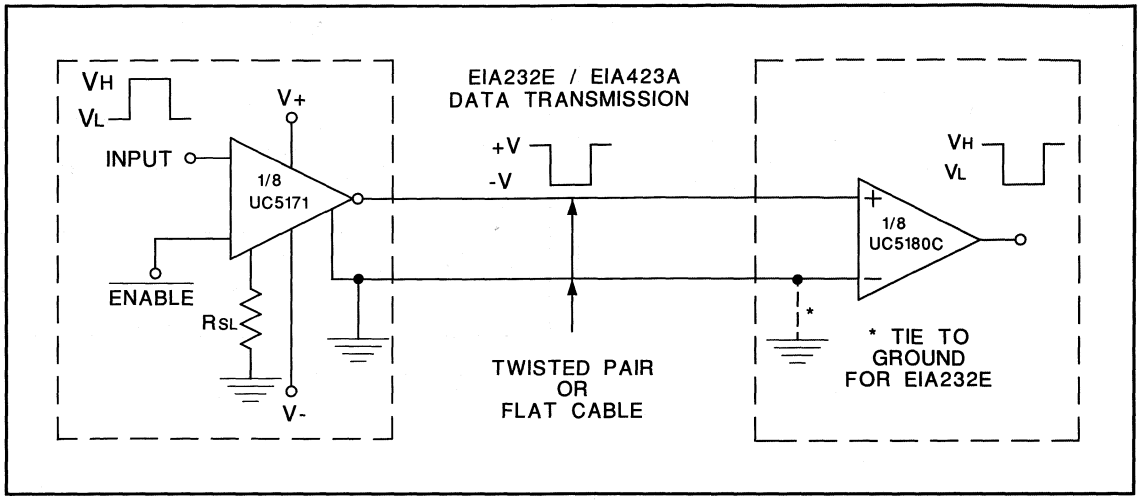
The UC5171 has two programmable output modes, either a low voltage mode which meets EIA-423A operational specifications, or the high output voltage mode which meets the EIA-232E specifications.

The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the modes select pin, (MS), to a TTL "high" level. The low output mode provides a controlled output swing and is accomplished by connecting the mode select pin, (MS), to a TTL "low level."

EIA Standards

The UC5171 meets or exceeds the EIA Standards for EIA-232E and EIA-423A modes of operation except under power down conditions. When powered down with the output attached to an active buss, the UC5171 has the potential to load the bus under transient conditions.

APPLICATIONS



UC5171 Specific Layout Notes

The UC5171 layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5171 on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5171 can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal-to-metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5171 is P6KEIOCA

*Transzorb is a trademark of General Semiconductor Industries.

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UNITRODE

Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Meets Standards EIA232E/CCITT V.28, and EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins
- EOS on all Output Pins 35V under all Output Conditions
- High Current Output for Long Line Drive, Exceeds Standards

DESCRIPTION

The UC5172 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels are independent of the power variations.

The UC5172 has high output current, and current balance for long line drive applications. EOS - Output parasitic SCRs powered on and off are 35V, well above signal levels, allowing protection devices to work.

Inputs are compatible TTL+MOS logic families and are diode protected against negative transients.

FUNCTIONAL TABLE

INPUTS		OUTPUT
$\overline{EN}$	DATA	EIA232E/EIA423A
0	0	5V to 6V
0	1	-5V to -6V
1	X	High Z

Note 2: Minimum output swings.

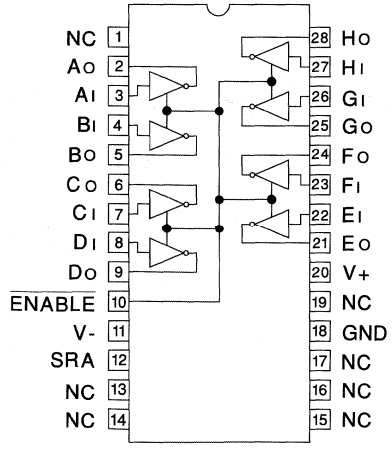
ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . -15V
PLCC Power Dissipation, T_A=25°C (Note 3) . . . . . 1000 mW
DIP Power Dissipation, T_A=25°C (Note 3) . . . . . 1250 mW
Input Voltage . . . . . -1.5V to +7V
Output Voltage . . . . . -6V to +6V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . -65°C to +150°C

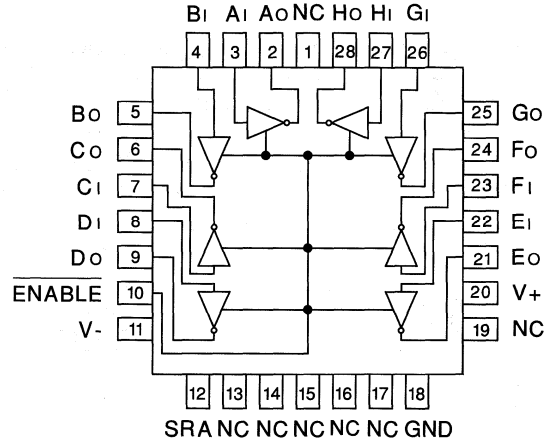
Note 1: All voltages are with respect to ground, pin 18.
Note 3: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



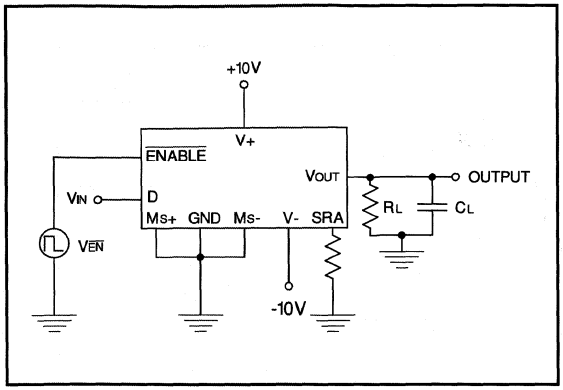
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0°C < T_A < +70°C$, $R_{SRA} = +10k$, $T_A = T_J$.

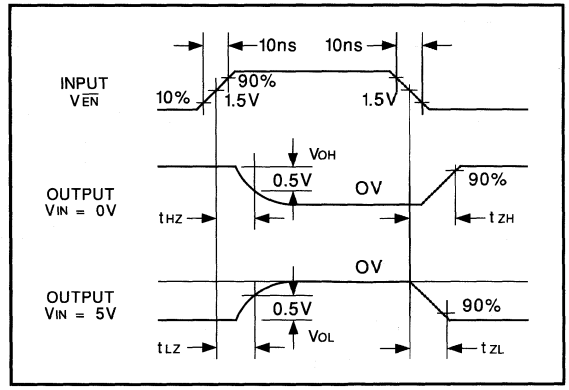
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-9		-15	V
V+ Supply Current	I+	R_L = Infinite $\overline{En}$ = 0V			15	25	mA
V- Supply Current	I-	R_L = Infinite $\overline{En}$ = 0V			-17	-25	mA
INPUTS							
High-Level Input Voltage	V_{IH}			2.0			V
Low-Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA			-1.1	-18	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		-2	0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-200	-8.0		µA
OUTPUTS							
High Level Output Voltage	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA-423A)			R_L = 450	4.5	5.2	6.0	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-5.0	-5.3	-6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-5.0	-5.6	-6.0	V
(EIA-423A)			R_L = 450	-4.5	-5.4	-6.0	V
Output Balance (EIA-423A)	V_{BAL}	R_L = 450, $V_{OH} - V_{OL} = V_{BAL}$			0.2	0.4	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, $V_O = \pm 6V$, V+ = 15V, V– = -15V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	65		mA
			V_{IN} = 5V	25	70		mA
Power Off Output Current	I_{PO}	$V_O = \pm 6V$, V+ = V– = 0V		-100		100	mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-| = +10V$, $0°C < T_A < +70°C$, $T_A = T_J$.

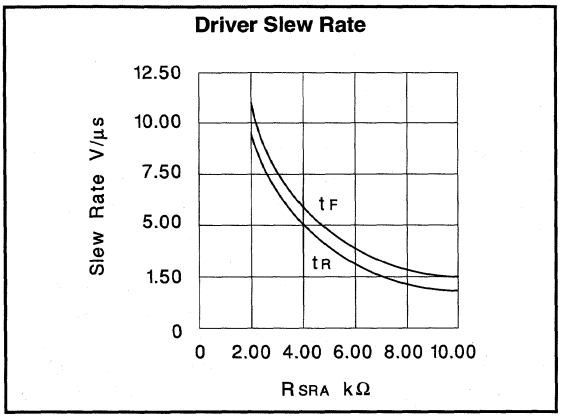
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	7.6	8.5	9.4	V/µs
	t_F	R_L = 450, C_L = 50pF	7.6	8.5	9.4	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.5	1.7	1.9	Vµs
	t_F	R_L = 450, C_L = 50pF	1.5	1.7	1.9	V/µs
Propagation Output to High Impedance	t_{HZ}	R_{SRA} = 10k		0.8	2.0	µs
	t_{LZ}	R_L = 450, C_L = 50pF		0.5	2.0	µs
Propagation High Impedance to Output	t_{ZH}	R_{SRA} = 10k		2.0	7.0	ms
	t_{ZL}	R_L = 450, C_L = 50pF		1.0	7.0	µs

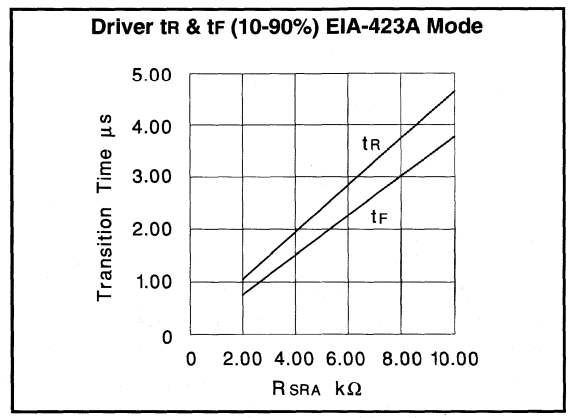
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATIONS

Slew Rate Programming

Slew rate for the UC5172 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \text{ (RSRA in k}\Omega\text{)}$$

The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

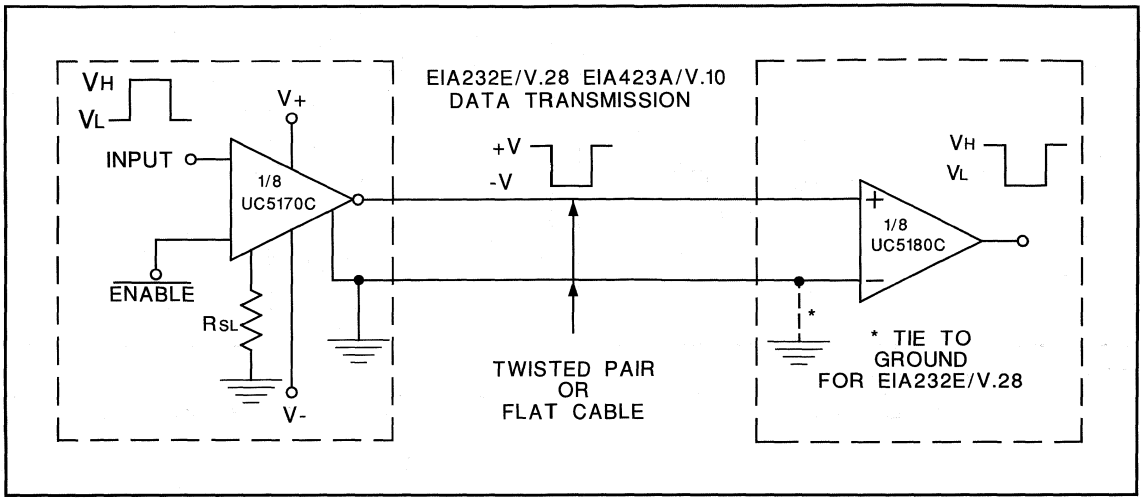
Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)
Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

The UC5172 has been used in applications up to 460KBPS.

APPLICATIONS



Specific Layout Notes

The UC5172 layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5172 on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5172 can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5172 is P6KEIOCA.

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UNITRODE

Octal Line Receiver

FEATURES

- Meets EIA 232E/423A/422A and CCITT V.10,V.11, V.28, X.26, X.27
- Single +5V Supply--TTL Compatible Outputs
- Differential Inputs Withstand ± 25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current--35 mA Max
- Input Noise Filter
- Internal Hysteresis

DESCRIPTION

The UC5180C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA423A, EIA422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180C includes an input noise filter and is intended for applications employing data rates up to 200 KBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

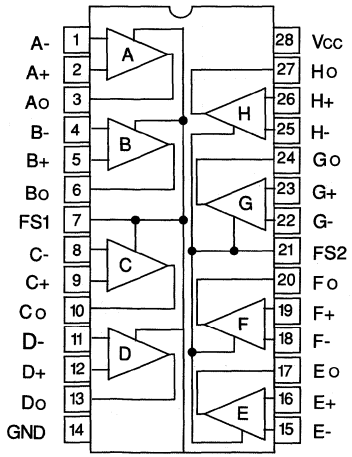
Supply Voltage, V_{CC}	7V
Output Sink Current	50 mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to V_{CC}
PLCC Power Dissipation, T_A = 25°C (Note 2)	1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2)	1200 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	-300°C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive into, negative out of the specified terminal

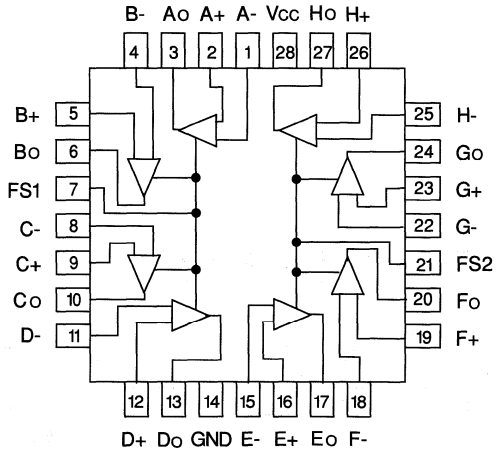
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, Input Common Mode Range ± 7V, T_A = T_J

PARAMETERS	SYMBOL	TEST CONDITIONS		UC5180C MIN	UC5180C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ | V_{IN} | ≤ 25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0 ≤ I_{OUT} ≤ 8mA, $V_{FAILSAFE}$ = 0V		0.45	V
			0 ≥ I_{OUT} ≥ - 400 µA, $V_{FAILSAFE}$ = V_{CC}	2.7		
Differential Input High Threshold	V_{TH}	V_{OUT} = 2.7V, I_{OUT} = 440 µA (See Figure 1)	R_S = 0 (Note 2)	50	200	mV
			R_S = 500 (Note 2)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 440 mA (See Figure 1)	R_S = 0 (Note 2)	-200	-50	mV
			R_S = 500 (Note 2)	-400		
Hysteresis	V_H	F_S = 0V or V_{CC} (See Figure 1)		50	140	mV
Open Circuit Input Voltage	V_{ICC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{CH}	V_{ID} = 1V, I_{OUT} = - 440µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 3)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 4		20	100	mA
Supply Current	I_{CC}	4.75V ≤ V_{CC} ≤ 5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IN} = -10V	-3.25		

Note 2: Rs is a resistor in series with each input.
Note 3: Measured after 100ms warm up (at 0°C)
Note 4: Only 1 output may be shorted at one time and then only for a maximum of 1 sec.

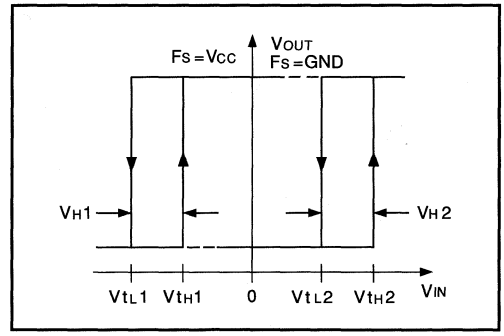


Figure 1. VtL, VtH, VH Definition

AC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C, Figure 2, T_A = T_J.

PARAMETERS	SYMBOL	TEST CONDITIONS	UC5180C MIN	UC5180C MAX	UNITS
Propagation Delay - Low to High	t_{PLH}	C_L = 50pF, V_{IN} = ± 500mV		550	ns
Propagation Delay - High to Low	t_{PHL}	C_L = 50pF, V_{IN} = ± 500mV		550	ns
Acceptance Input Frequency	f_A	Unused Input Grounded, V_{IN} = ± 200mV		0.1	MHz
Rejectable Input Frequency	f_R	Unused Input Grounded, V_{IN} = ± 500mV	5.5		MHz

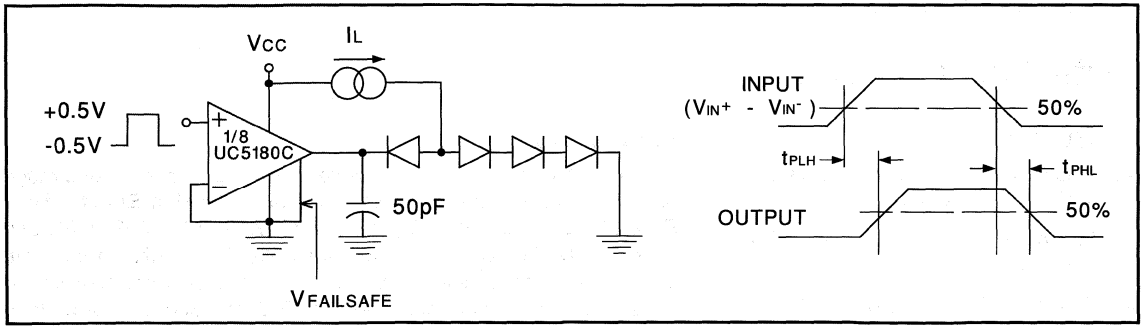


Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

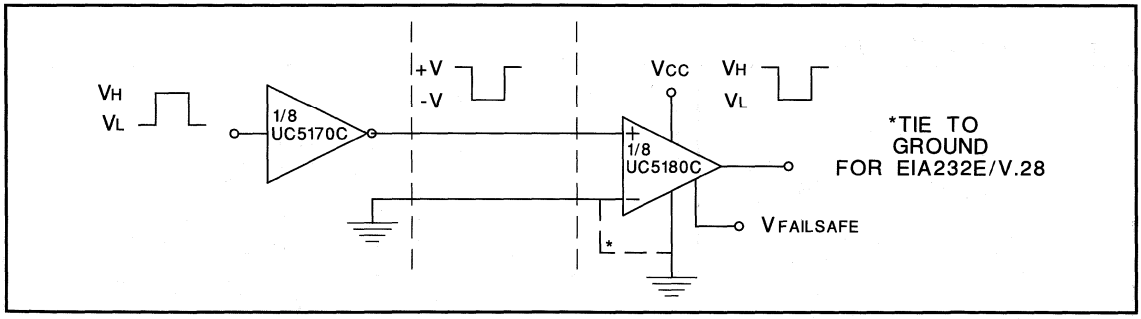
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) drive in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to VCC or ground. A connection to VCC provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (FS1 and FS2) on the UC5180C where each provides common failsafe control for four receivers.

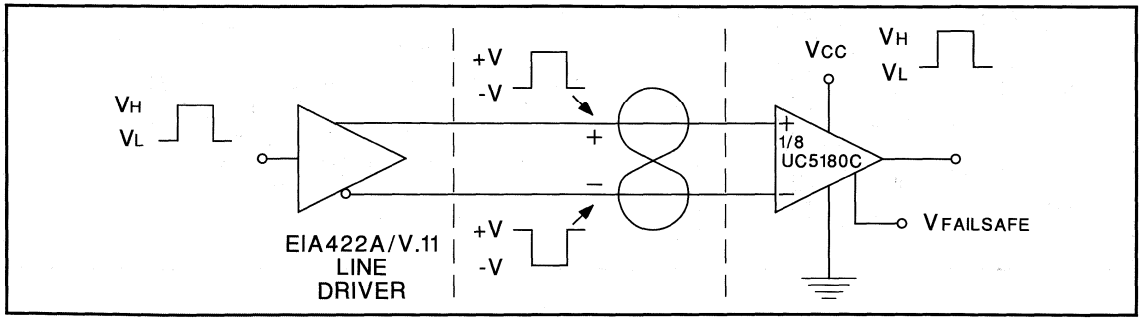
Input Filtering (UC5180C)

The UC5180C has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



UNITRODE CORPORATION
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UNITRODE

Octal Line Receiver

FEATURES

- Meets EIA232E/423A/422A and CCITT V.10, V.11, V.28, X.26, X.27
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35mA Max
- Internal Hysteresis

DESCRIPTION

The UC5181C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA422A, EIA423A and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5181C is similar to the UC5180C, but without the input filtering. Thus, it covers the entire range of data rates up to 10MBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

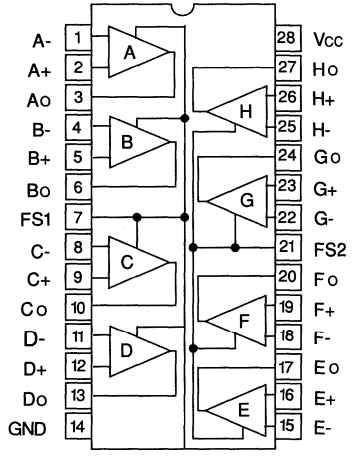
Supply Voltage, V_{CC}	7V
Output Sink Current	50mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to V_{CC}
PLCC Power Dissipation, T_A=25° C (Note 2)	1000 mW
DIP Power Dissipation, T_A=25° C (Note 2)	1200 mW
Storage Temperature Range	-65° C to +150° C
Lead Temperature (Soldering, 10 seconds)	-300° C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive in, negative out of the specified terminal.

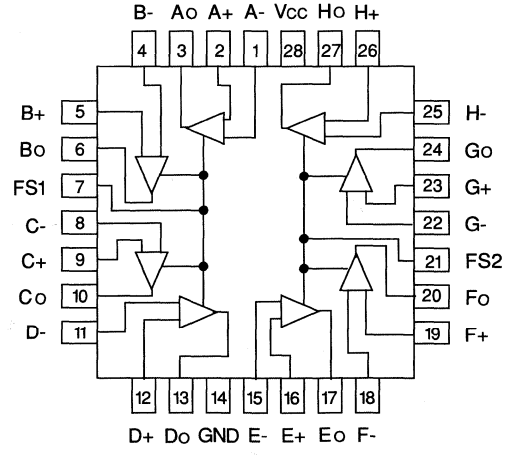
Note 2: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V, T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS		UC5181C MIN	UC5181C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ |V_{IN}|≤25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0≥I_{OUT}≤8mA $V_{FAILSAFE}$=0V		0.45	V
			0≥I_{OUT}≥-400µA, $V_{FAILSAFE}$=V_{CC}	2.7		
Differential Input High Threshold	V_{TL}	V_{OUT}= 0.45V, I_{OUT} = -440µA (See Figure 1)	R_S = 0 (Note3)	50	200	mV
			R_S = 500 (Note 3)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 3)	-200	-50	mV
			R_S = 500 (Note 3)	-400		
Hysteresis	V_H	F_S=0V or V_{CC} (See Figure 1)		45	140	mV
Open Circuit Input Voltage	V_{IOC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, I_{OUT} = -440 µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 4)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 5		20	100	mA
Supply current	I_{CC}	4.75V ≤V_{CC}≤5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IH} = -10V	-3.25		

Note 3: Rs is a resistor in series with each input.
Note 4: Measure after 100 ms warm up (at 0°C).
Note 5: Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
Note 6: The delays, either t_{PLH} or t_{PHL}, shall not vary from receiver to receiver by more than 35ns.

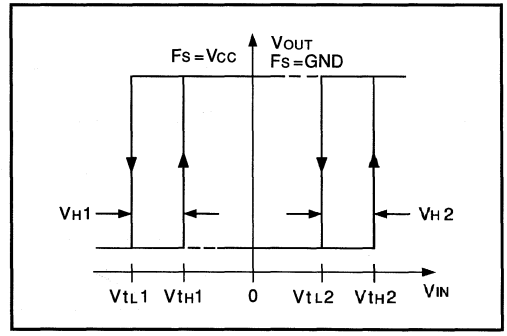


Figure 1. VTL, VTH,VH Definition

AC ELECTRICAL CHARACTERISTICS: V_{CC}=5V ±5%. T_A=0°C to +70°C, Figure 2 T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS	UC5181C MIN	UC5181C MAX	UNITS
Propagation Delay–Low to High	t_{PLH}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Propagation Delay–High to Low	t_{PHL}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Acceptable Input frequency	f_A	Unused Input Grounded, V_{IN}= ±200 mV		5.0	MHz

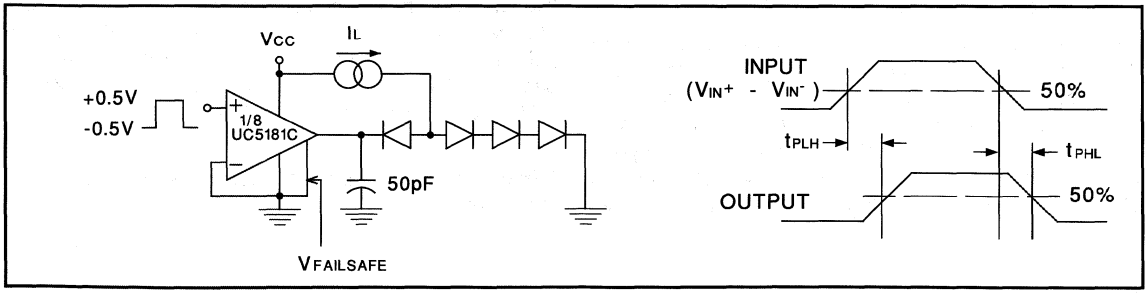


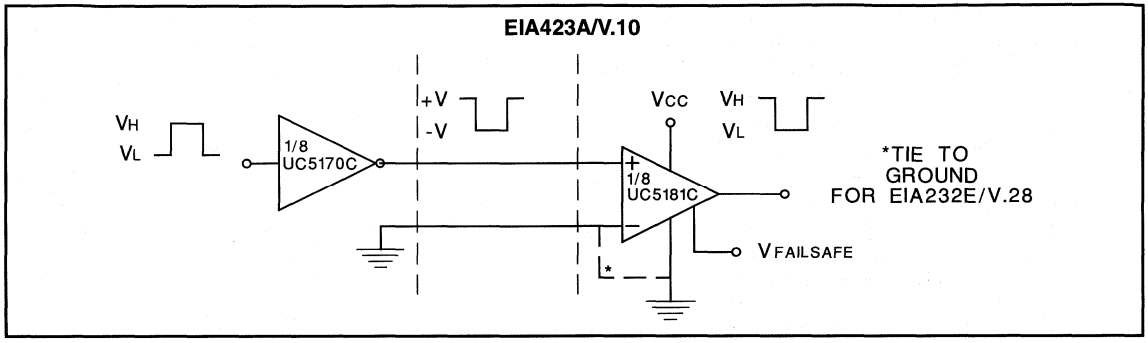
Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

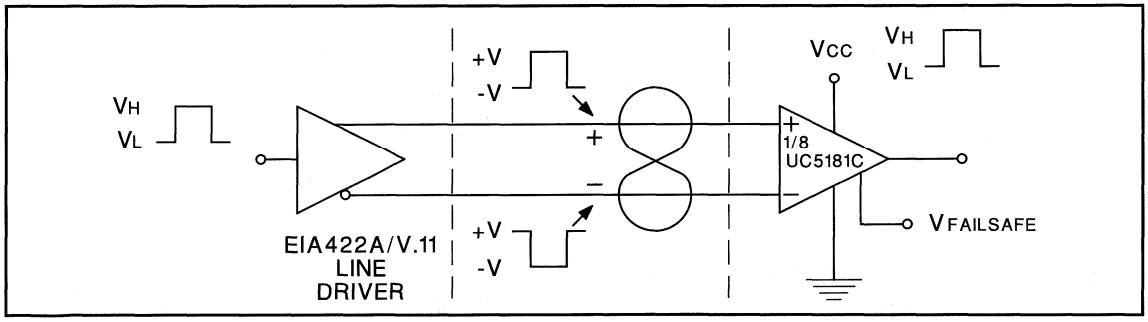
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to VCC or ground. A connection to VCC provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (FS1 and FS2) on the UC5181C where each provides common failsafe control for four receivers.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, and protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5180C and the UC5181C is P6KE22CA.

* Transzorb is a trademark of General Semiconductor Industries.

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CAN Transceiver

FEATURES

- Pin Compatible with PCA82C250 and DeviceNet, SDS, ISO11898 Compatible
- High Speed, up to 1Mbps
- Differential Transmit to the Bus and Receive from the Bus to the CAN Controller
- At Least 110 Nodes Can Be Connected
- 100V Transient Protection on the Transmit Output
- 24V Supply Cross Wire Protection on CANH and CANL
- No Bus Loading When Powered Down
- Operates over –40°C to +125°C
- Unitrode DeviceNet ID#107

DESCRIPTION

The UC5350 Control Area Network Transceiver is designed for industrial applications employing the CAN serial communications physical layer per ISO 11898 standard. The device is a high speed transceiver designed for use up to 1Mbps. Especially designed for hostile environments, this device features cross wire, loss of ground, over voltage, and over temperature protections well as a wide common mode range.

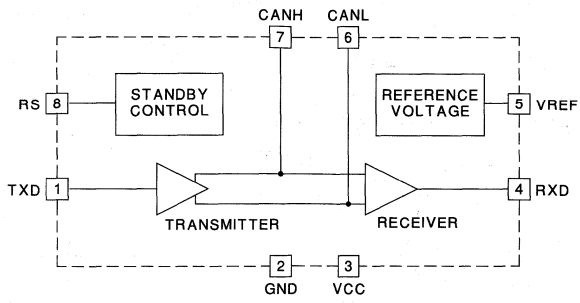
The transceiver interfaces the single ended CAN controller with the differential CAN bus found in industrial and automotive applications. It operates over the –7V to +12V common mode range of the bus and will withstand common mode transients of –25V to +18V as well as Schaffner tests. Performance features include high differential input impedance, a symmetrical differential signal driver and very low propogation delay that improves bus bandwidth and length by reducing reflection and distortion.

The transceiver operates over a wide temperature range, –40°C to +125°C and is available in 8-pin SOIC and Dual-in-Line packages.

FUNCTIONAL TABLE (VCC = 4.5V to 5.5V)

Inputs		System Mode	Output Mode	Outputs	
TXD	RS			$V_{CANH} - V_{CANL}$	RXD
0	0	High Speed	Dominant	1.5V to 3V	0
1	0	High Speed	Recessive	–120mV to +12mV	1
High Z	0	High Speed	Recessive	–120mV to +12mV	1
X	1	Standby		High Z	0 at Bus = Dominant 1 at Bus = Recessive

BLOCK DIAGRAM



UDG-96202

3/98

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . –0.3V to 9V
TXD, RXD, VREF, RS . . . . . –0.3V to VCC + 0.3V
CANL, CANH
0V < VCC < 5.5V. . . . . –8V to +36V
Non-Destructive, Non-Operative. . . . . –8V to +32V
Transient, Schaffner Test (Fig. 1) . . . . . –150 to +100V
Operating Temperature . . . . . –40°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.). . . . . +300°C
Crosswire Protection Maximum VBUS 30V
Bus Differential Voltage* 30V
Cross Wire Protection TA. . . . . –40°C to 125°C

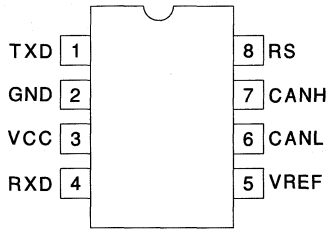
Currents are positive into, negative out of the specified terminal.

Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

**Refers to Figures 9, 10, 11, 12 and 13.*

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N, D Package



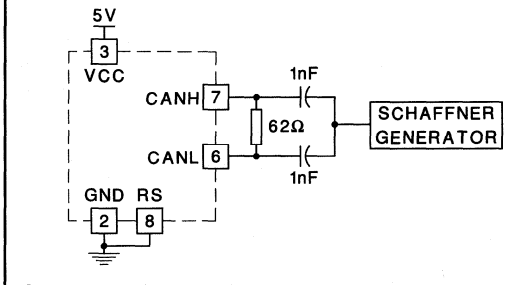


Figure 1. Schaffner Test

ELECTRICAL CHARACTERISTICS (Total Device)

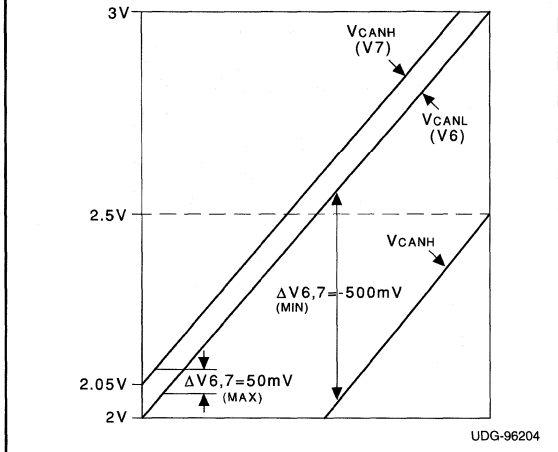
Unless otherwise stated, the device is disconnected from the bus line; VCC = 4.5V to 5.5V; 60Ω in parallel with 100pF load between CANH and CANL; TA = –40°C to +125°C, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		5.5	V
Supply Current	Dominant, TXD = 1V			70	mA
	Recessive, TXD = 4V		9	13	mA
	Standby, RS = 4V		1	1.5	mA
RS Input Current		–10		5	µA
RS Voltage Input = Logic 1	Standby	0.75VCC			V
RS Voltage Input = Logic 0	High Speed			0.3VCC	V
Transmitter Voltage Input = Logic 1	Transmitter Output Recessive	0.7VCC			V
Transmitter Voltage Input = Logic 0	Transmitter Output Dominant			0.3VCC	V
Transmitter Current Input at Logic 1	TXD = 4V			30	µA
Transmitter Current Input at Logic 0	TXD = 1V	–30		30	µA
Receiver Voltage Output = Logic 1	RXD = –100µA, TXD = 4V	VCC –1.0			V
Receiver Voltage Output = Logic 0	RXD = 1mA, TXD = 1V		0.75	1.0	V
	RXD = 10mA, TXD = 1V		1.2	1.5	V
CANH, CANL Input Resistance	No Load, TXD = 4V	30	43	54	kΩ
Differential Input Resistance	No Load, TXD = 4V	60	86	108	kΩ
CANH, CANL Input Capacitance	(Note 1)			20	pF
Differential Input Capacitance	(Note 1)			10	pF
Reference Output Voltage	VREF = ±50µA	0.45VCC		0.55VCC	V

Note 1: Guaranteed by design. Not 100% tested in production.

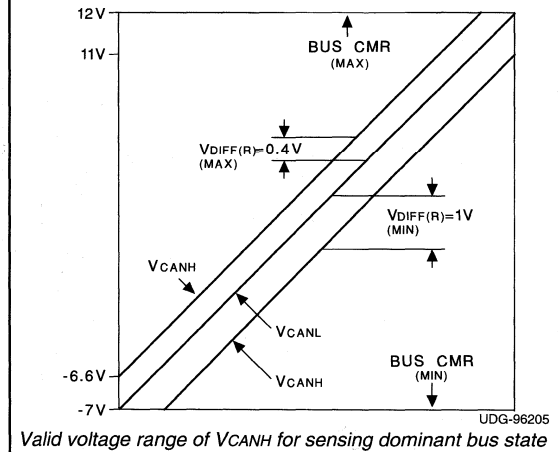
ELECTRICAL CHARACTERISTICS (DC Parameters For Recessive State) Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CANH}, V_{CANL}	No Load, TXD = 4V (Figure 2)	2	2.5	3	V
Differential Output Transmitter (V_{CANH} – V_{CANL})	No Load, TXD = 4V (Figure 2)	–500	0	50	mV
Differential Input Receiver	Common Mode Range = –7V to +12V, TXD = 4V, CANH, CANL Externally Driven (Figure 3)	–1		0.40	V
Differential Input Resistance	No Load	60			kΩ
CANH, CANL Input Resistance		15		50	kΩ



Valid output of CANH, CANL during recessive state transmission. TXD = LOGIC 1

Figure 2. Recessive State Voltage Diagram

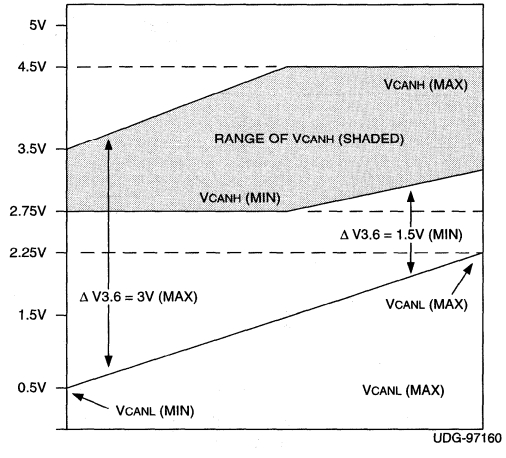


Valid voltage range of V_{CANH} for sensing dominant bus state as V_{CANL} varies over bus common range mode. TXD = LOGIC1

Figure 3. Recessive State Voltage Diagram

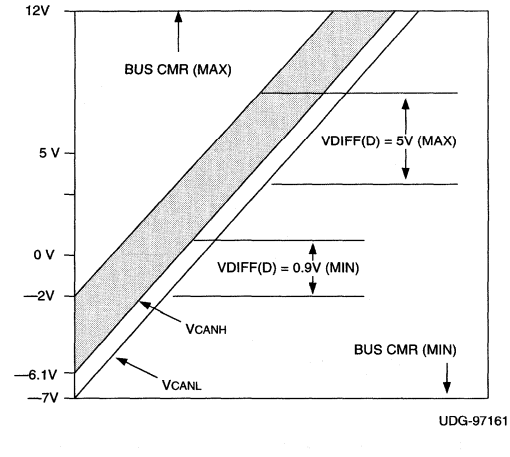
ELECTRICAL CHARACTERISTICS (DC Parameters For Dominant State) Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL. VCC = 4.75V to 5.5V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CANH Output Voltage (V_{CANH})	TXD = 1V (Figure 4)	2.75		4.5	V
CANL Output Voltage (V_{CANL})	TXD = 1V (Figure 4)	0.50	1.1	2.25	V
Differential Output Transmitter (V_{CANH} - V_{CANL})	TXD = 1V (Figure 4)	1.5	2	3	V
Differential Input Receiver ($V_{DIFF(D)}$)	Common Mode Range = –2 to +7V, TXD = 4V, CANH, CANL Externally Driven (Figure 5)	0.9		5	V
	Common Mode Range = –7 to +12V, TXD = 4V, CANH, CANL Externally Driven (Figure 5)	1.0		5	V



Valid voltage range of V_{CANH} for sensing recessive bus state as V_{CANL} varies over bus common mode range. TXD = LOGIC 1

Figure 4. Dominant State Voltage Diagram



Valid voltage range of V_{CANH} for sensing dominant bus state as V_{CANL} varies over bus common range mode. TDX = LOGIC 0

Figure 5. Dominant State Voltage Diagram

TRANSMITTER CHARACTERISTICS

Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Transmitter (V_{CANH} - V_{CANL})	Dominant Mode	1.5	2	3	V
	Recessive Mode	–500		50	mV
Delay From TXD to Bus Active T_{ON} (TXD)	(Figure 6)		45	65	ns
Delay From TXD to Bus Inactive T_{OFF} (TXD)	60Ω Across CANH and CANL (Figure 6)		40	80	ns

RECEIVER CHARACTERISTICS

Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Receiver (V_{CANH} - V_{CANL})	Dominant Mode, TXD = 4V	0.9			V
	Recessive Mode, TXD = 4V			0.4	V
Differential Input Hysteresis	TXD = 4V		150		mV
Delay From Bus to RXD (T_{ON})	Inactive to Active Bus (Figure 6)			55	ns
Delay From Bus to RXD (T_{OFF})	Active to Inactive Bus, 60Ω Across CANH and CANL (Figure 6)			145	ns
Delay From Bus to RXD (T_{OFF})	T_A = –25°C to 85°C Active to Inactive Bus, 60Ω Across CANH and CANL (Figure 6)			75	ns

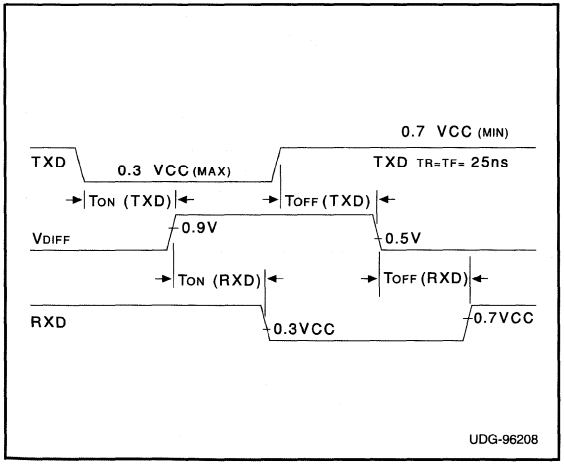


Figure 6. Transceiver AC Response

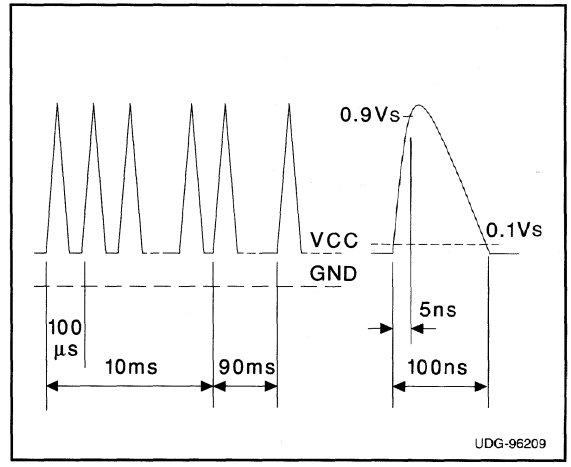


Figure 7. Timing Diagram for Schaffner Tests

Magnitude Specifications for Vs

ISO	DIN 40839-1	Schaffner
DP7637/1	(Draft)	NSG500C/506C
Up to 150V	Up to 150V	40V to 200V

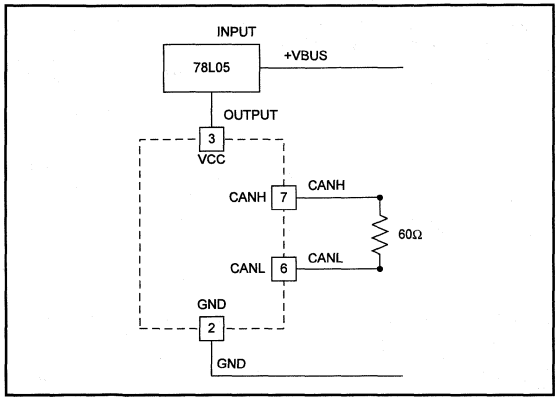


Figure 8. Normal Connection

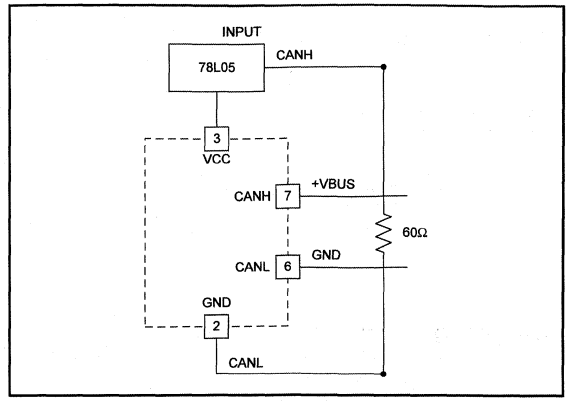


Figure 9. Crosswire No. 1

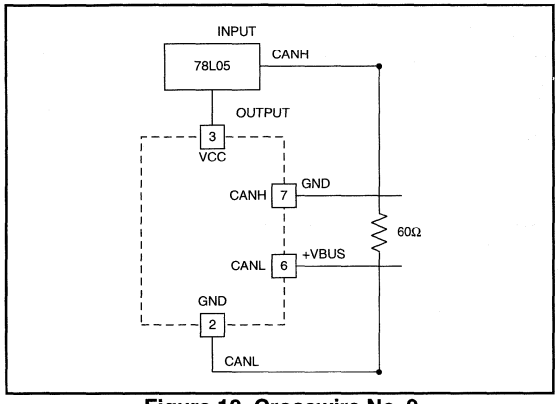


Figure 10. Crosswire No. 2

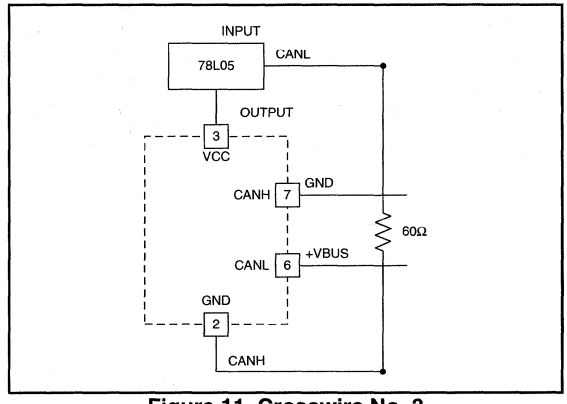


Figure 11. Crosswire No. 3

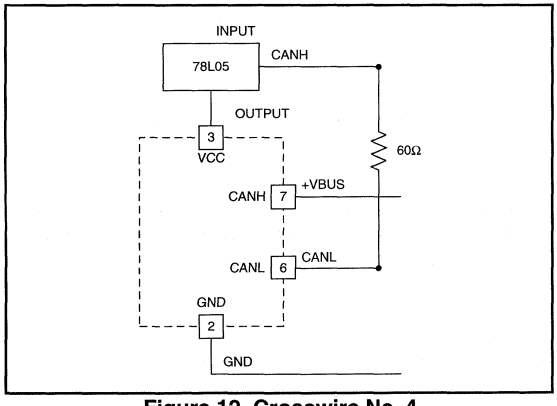


Figure 12. Crosswire No. 4

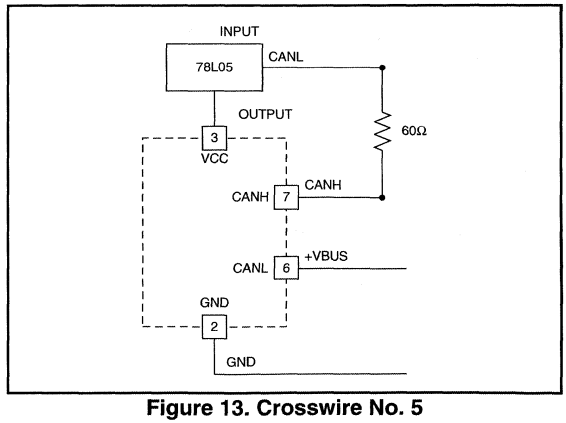


Figure 13. Crosswire No. 5

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UNITRODE

ADVANCE INFORMATION

CAN Transceiver with Voltage Regulator

FEATURES

- DeviceNet, SDS, ISO 11898 Compatible
- High Speed, up to 1Mbps
- Differential Transmitter and Receiver bus interface
- – 25V to +18V Protection on CANH and CANL
- Loss of Ground Protection
- High Differential Input Impedance
- Supports 110 nodes or more
- Operates over -25°C to +85°C
- Unitrode DeviceNet ID#107

DESCRIPTION

The UC5351 Control Area Network (CAN) Transceiver is designed for industrial applications employing the CAN serial communications physical layer per the ISO 11898 standard. The device is a high speed transceiver plus voltage regulator designed for use up to 1Mbps. Especially designed for hostile environments, this device features cross-wire and over voltage protection, thermal shutdown, a wide common mode range, and loss of ground protection.

The UC5351 CAN Transceiver interfaces the single ended CAN Controller with the differential CAN Bus found in industrial and automotive applications. Performance features include high input impedance, a symmetrical differential signal driver, and low propagation delay that improve bus bandwidth and length, while reducing reflection and distortion. Reduced reflection and distortion results in increases of effective bus length and bandwidth.

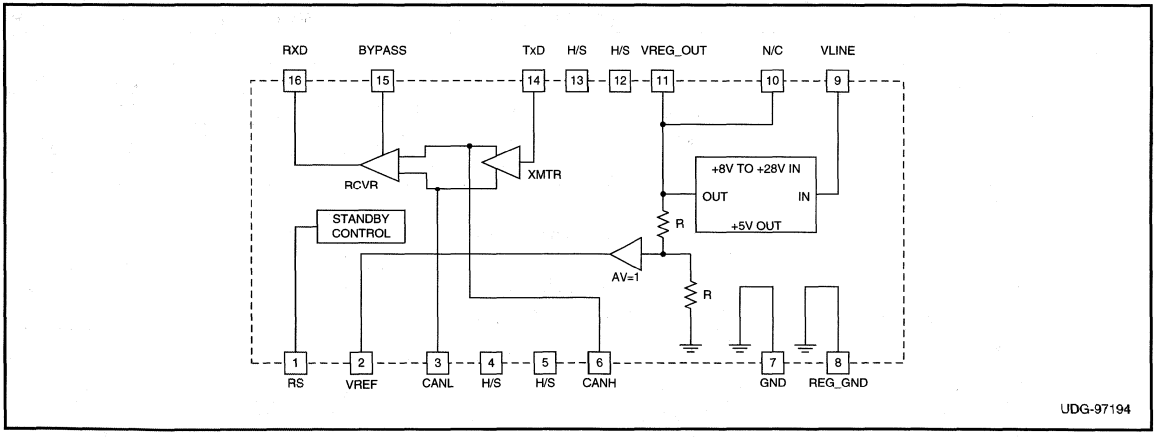
The on-board regulator permits direct connection to a +8V to 24V power bus and supply power to the transceiver with 40mA of reserve ouput current to power external components.

The transceiver operates over a wide temperature range, –25°C to 85°C, and is available in a16-pin power SOIC package.

FUNCTIONAL TABLE (VLINE = 8V TO 28V)

Inputs		Sytem Mode	Output Mode	Outputs	
TxD	Rs			$V_{CANH} - V_{CANL}$	RxD
0	0	High Speed	Dominant	1.5V to 3V	0
1	0	High Speed	Recessive	–120mV to +12mV	1
High Z	0	High Speed	Recessive	–120mV to +12mV	1
X	1	Standby		high Z	A & "0" @ Bus = Dominant
					A & "0" @ Bus = Recessive

BLOCK DIAGRAM

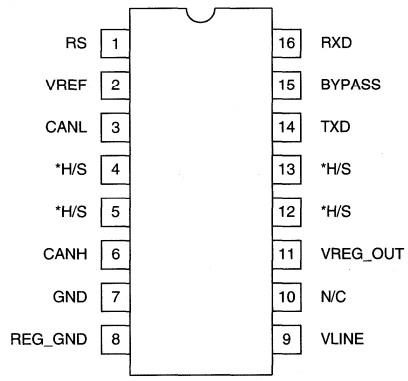


ABSOLUTE MAXIMUM RATINGS

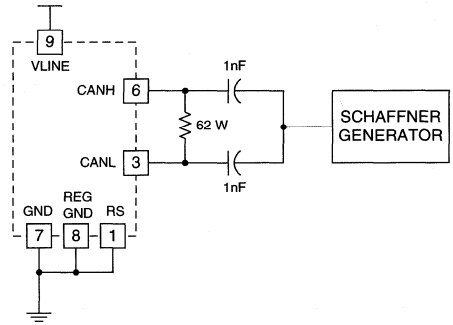
Supply Voltage . . . . . –0.3V to +36V
TXD, RXD, VREF, RS . . . . . –0.3V to VCC +0.3V
CANL, CANH 8V < VLINE< 28V . . . . . –8V to +36V
Non-Destructive, Non-Operative . . . . . –8V to +32V
Transient, Schaffner Test (Figure 1) . . . . . –150V to +100V
Operating Temperature . . . . . –25°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and consideration of packages.

CONNECTION DIAGRAM

SOIC–16 (TOP VIEW)
DP Package



Warning: H/S pins are connected to the substrate which must float, attach all four pins to at least 0.5 square inch of etch.* ***DO NOT ATTACH TO GROUND!*



See Figure 7 for pulse timing.

ELECTRICAL CHARACTERISTICS (Total Device) Unless otherwise stated, the device is disconnected from the bus line; VLINE = 10V; Io(VREG_OUT) = –40mA; C_{VLINE}=0.33µF; C_{VREG_OUT} = 0.1µF; C_{BYPASS} = 0.1µF; 60Ω in parallel with 100pF between CANH and CANL; T_J =–25°C to +150°C. VR = VREG_OUT Voltage.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Section					
Supply Voltage (VLINE)		8		28	V
Supply Current (VLINE)	Dominant, TXD = 1V; Io(VREG_OUT) = 0			75	mA
	Recessive, TXD = 4V; Io (VREG_OUT) = 0		12	17	mA
	Standby, RS = 4V; Io (VREG_OUT) = 0		6.5	9	mA
Output Voltage (VREG_OUT)	T_J = 25°C	4.8	5	5.2	V
	1mA < Io (VREG_OUT) < 40mA; 8V < VLINE < 28V	4.75		5.25	V
Line Regulation (VREG_OUT)	T_J = 25°C, 8V < VLINE < 28V			90	mV
Load Regulation (VREG_OUT)	T_J = 25°C, 1mA < Io (VREG_OUT) < 40mA			60	mV
Ripple Rejection (VREG_OUT)	f=120Hz, 8V < VLINE < 16V	47			dB
RS Input Current		–5		5	µA
RS Input Voltage = Logic 1	Standby	(0.75)•VR			V
RS Input Voltage = Logic 0	High Speed			(0.3)•VR	V

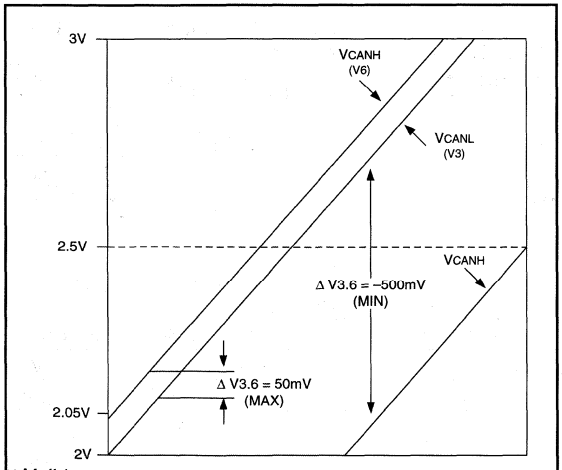
ELECTRICAL CHARACTERISTICS (Total Device) Unless otherwise stated, the device is disconnected from the bus line; VLINE = 10V; $I_{O(VREG\_OUT)}$ = –40mA; C_{VLINE}=0.33µF; C_{VREG_OUT} = 0.1µF; C_{BYPASS} = 0.1µF; 60Ω in parallel with 100pF between CANH and CANL; T_J =–25°C to +150°C. VR = VREG_OUT Voltage.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Voltage Input = Logic 1	Transmitter Output Recessive	(0.7)•VR			V
Transmitter Voltage Input = Logic 0	Transmitter Output Dominant			0.3	V
Transmitter Current Input at Logic 1	TXD = 4V			30	µA
Transmitter Current Input at Logic 0	TXD = 1V	–30		30	µA
Receiver Voltage Output = Logic 1	RXD = –100µA	(0.8)•VR			V
Receiver Voltage Output = Logic 0	RXD = 1mA			(0.2)•VR	V
	RXD = 10mA			1.5	V
CANH, CANL Input Resistance	No Load	34	43	54	kΩ
Differential Input Resistance	No Load	68	86	108	kΩ
CANH, CANL Input Capacitance	(Note 1)			20	pF
Differential Input Capacitance	(Note 1)			10	pF
Reference Output Voltage	I (VREF) = ±50µA	(0.45)•VR		(0.55)•VR	V

Note: Guaranteed by design. Not 100% tested in production.

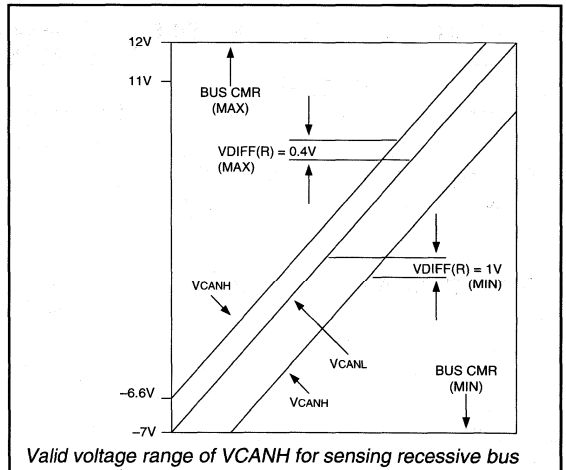
ELECTRICAL CHARACTERISTICS (DC Parameters for Recessive State) Unless otherwise stated, the device is disconnected form the bus line; 60Ω in parallel with 100pF load between CANH nad CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CANH}, V_{CANL}	No Load, TXD = 4V (Figure 2)	2	2.5	3	V
Differential Output Transmitter (V_{CANH}, V_{CANL})	No Load, TXD = 4V (Figure 2)	–500	0	50	mV
Differential Input Receiver		–1		0.4	V
Differential Input Resistance	No Load	68		108	kΩ
Differential Input Receiver	Common Mode Range = –7 V to +12V, TXD = 4V, CANH, CANL Externally Driven (Figure 3)	–1		0.40	V
Differential Input Resistance	No Load	68		108	kΩ



Valid output of CANH, CANL during recessive state transmission. TXD = LOGIC 1

Figure 2. Recessive State Voltage Diagram



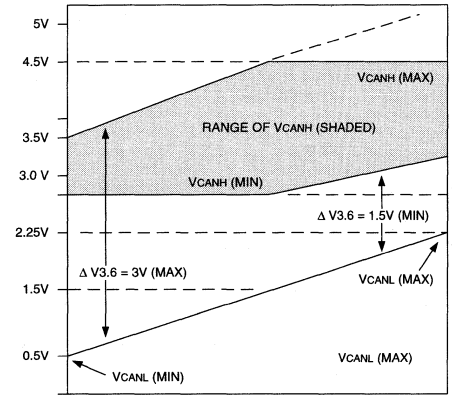
Valid voltage range of VCANH for sensing recessive bus state as VCANL varies over bus common mode range. TXD = LOGIC 1

Figure 3. Recessive State Voltage Diagram

ELECTRICAL CHARACTERISTICS (DC Parameters for Dominant State)

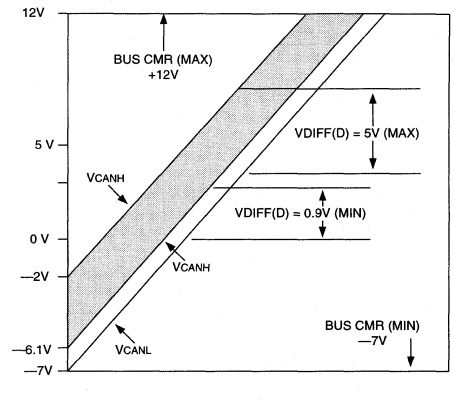
Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CANH Output Voltage (V_{CANH})	TXD = 1V (Figure 4)	2.75	3.5	4.5	V
CANL Output Voltage (V_{CANL})	TXD = 1V (Figure 4)	0.5	1.5	2.25	V
Differential Output Transmitter ($V_{CANH} - V_{CANL}$)	TXD = 1V (Figure 4)	1.5	2	3	V
Differential Input Transmitter ($V_{DIFF(D)}$)	Common Mode Range = –7V to +12V; TXD = 4V, CANH, CANL Externally Driven (Figure 5)	0.9		5	V



Valid output of CANH, CANL during dominant state transmission as CANL is varied over its minimum to maximum range. TXD = LOGIC0.

Figure 4. Dominant State Voltage Diagram



Valid voltage range of VCANH for sensing recessive bus state as VCANL varies over bus common mode range. TXD = LOGIC0.

Figure 5. Dominant State Voltage Diagram

TRANSMITTER CHARACTERISTICS

Unless otherwise stated, the device is disconnected form the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Transmitter ($V_{CANH} - V_{CANL}$)	Dominant Mode	1.5	2	3	V
	Recessive Mode	– 500		50	mV
Delay From TXD to Bus Active T_{ON} (TXD)	(Figure 6)			75	nS
Delay From TXD to Bus Active T_{OFF} (TXD)	60Ω Across CANH and CANL (Figure 6)			75	nS

RECEIVER CHARACTERISTICS

Unless otherwise stated, the device is disconnected form the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Transmitter ($V_{CANH} - V_{CANL}$)	Dominant Mode, TXD = 4V	0.9			V
	Recessive Mode, TXD = 4V		150		mV
Differential Input Hysteresis	TXD = 4V		150		mV
Delay from Bus to RXD (T_{ON})	Inactive to Active Bus (Figure 6)			150	nS
Delay from Bus to RXD (T_{OFF})	Active to Inactive Bus; 60Ω Across CANH and CANL (Figure 6)			150	nS

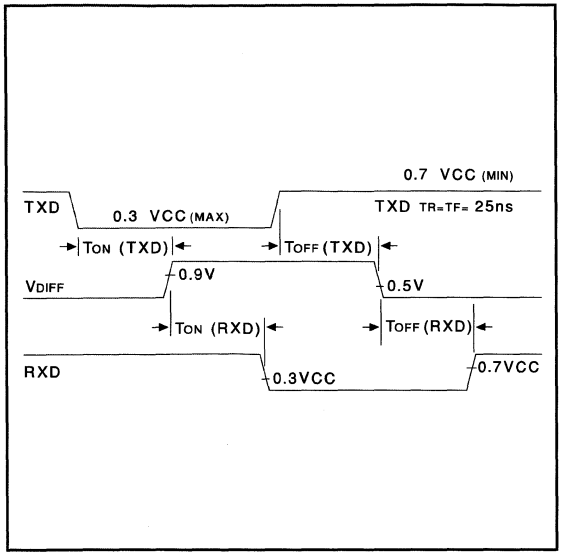


Figure 6. Tranceiver AC Response

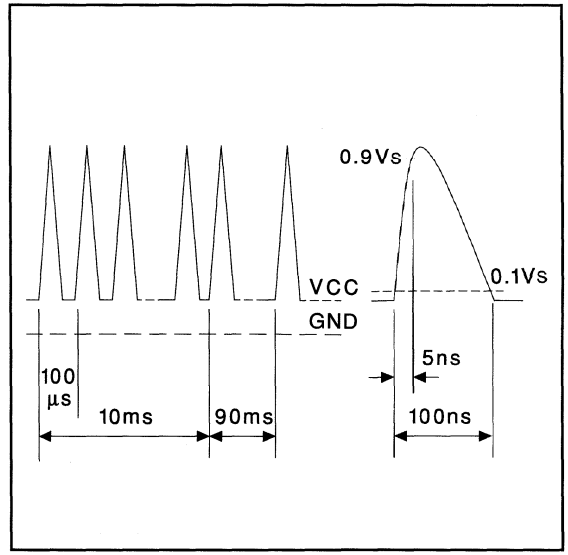


Figure 7. Timing Diagram for Schaffner Tests

Magnitude Specifications for Vs		
ISO	DIN-40839-1	Schaffner
DP7637/1	(Draft)	NSG500C/506C
Up to 150V	Up to 150V	40V to 200V

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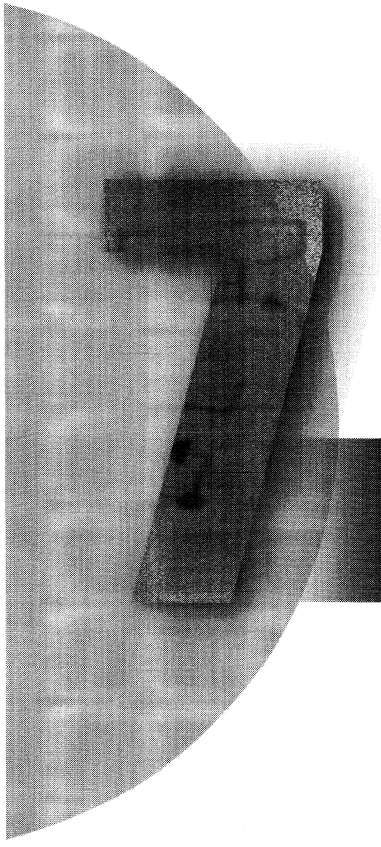


Unitrode Product Portfolio

Interface Products

Nonvolatile Products

Portable Power Products

Power Supply Control Products

SCSI

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5628+	UCC5630	UCC5632	UCC5638+	UCC5639+
Channels	14	9	9	15	15
Channel Capacitance	4	4	4	4	4
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD / SE	LVD / SE
Page Number	IF/3-78	IF/3-83	IF/3-93	IF/3-94	IF/3-99

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5640+	UCC5641+	UCC5646		
Channels	9	9	27		
Channel Capacitance	3	3	3		
Termination Impedance	Differential 105, Common Mode 150	Differential 105, Common Mode 150	Differential 105, Common Mode 150		
Disconnect High or Low	H	L	H		
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type LVD or SE / LVD	LVD	LVD	LVD		
Page Number	IF/3-104	IF/3-108	IF/3-112		

+ New Product

SCSI (cont.)

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5510+	UCC5630A	UCC5672+	UCC5680	
Channels	9	9	9	9	
Channel Capacitance	4	4	4	4	
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	
Diff B input filter	N	N	Y	Y	
Disconnect High or Low	N/A	H	H	H	
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	
Supports Active Negation	Y	Y	Y	Y	
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD	
Page Number	IF/3-5	IF/3-87	IF/3-120	IF/3-121	

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5601	UC5602	UC5603	UC5604	UC5605
Channels	18	18	9	9	9
Channel Capacitance	10	11	6	9	4
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	N	N	Y	N	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-9	IF/3-13	IF/3-18	IF/3-22	IF/3-26

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5606	UC5607	UC5608	UC5609	UC5612
Channels	9	18	18	18	9
Channel Capacitance	1.8	8	6	6	4
Termination Impedance	110 & 2500	110	110	110	110
Disconnect High or Low	L	2L	H	L	H
Termpwr Voltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-30	IF/3-34	IF/3-37	IF/3-40	IF/3-43

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5613	UCC5614	UCC5617	UCC5618	UCC5619
Channels	9	9	18	18	27
Channel Capacitance	3	1.8	2.5	2.5	3
Termination Impedance	110	110 & 2500	110	110	110
Disconnect High or Low	H	H	L	H	L
Termpwr Voltage Range	4 - 5.25	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-47	IF/3-51	IF/3-55	IF/3-59	IF/3-63

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5620	UCC5621	UCC5622		
Channels	27	27	27		
Channel Capacitance	3	3	3		
Termination Impedance	110	110	110		
Disconnect High or Low	H	Split Low	Split High		
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25		
Supports Active Negation	Y	Y	Y		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type SE, LVD or SE / LVD	SE	SE	SE		
Page Number	IF/3-66	IF/3-70	IF/3-74		

Special Functions Circuit	UNITRODE PART NUMBER		
	UCC5661		
Part Name	Ethernet Coaxial Impedance Monitor		
Description	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT		
Page Number	IF/3-112		

+ New Product

Bus Bias Generators

Special Functions	UNITRODE PART NUMBER				
	UC382	UC385	UC560	UCC561+	UC563+
Bus Standard	GTL / BTL	GTL / BTL	SCSI-1,2,3	SPI-2,3	VME / VME64
Sink / Source Current	Pgm / 3A	Pgm / 5A	300mA / –750mA	200mA / –200mA	475mA / –575mA
Page Number	PS/4-2	PS/4-8	IF/4-3	IF/4-7	IF/4-10

+ New Product

Hot Swap Power Managers

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3912	UCC3913	UC3914	UCC3915	UCC39151
Voltage Range	3V to 8V	−10.5V to External Limitation	5V to 35V	7V to 15V	7V to 15V
Current Range	0A to 3A	Externally Limited	Externally Limited	0A to 3A	0A to 3A
Integrated Power FET	Y	N	N	Y	Y
RDSon	150mΩ	N/A	N/A	150mΩ	150mΩ
Programmable Fault Threshold	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	N	Y	Y	N	N
Average Power Limiting	N/A	Y	Y	N/A	N/A
Application / Design Note	DN-58, DN-68, U-151	DN-67		DN-58, DN-68, U-151	DN-58, DN-68, U-151
Available Package	TSSOP, SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-9	IF/5-15	IF/5-23	IF/5-37	IF/5-42

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3916	UCC39161	UCC3917+	UCC3918	UCC3919
Voltage Range	4V to 6V	4V to 6V	10V to External Limitation	3V to 6V	3V to 8V
Current Range	−1.8A to −1.5A	−1A to −0.7A	Externally Limited	0A to 4A	Externally Limited
Integrated Power FET	Y	Y	N	Y	N
RDSon	220mΩ	220mΩ	N/A	60mΩ	N/A
Programmable Fault Threshold	N	N	Y	Y	Y
Programmable Time Delays	Y	Y	Y	Y	Y
Latched Fault Mode	N	N	Y	N	Y
Average Power Limiting	N/A	N/A	Y	N/A	Y
Application / Design Note			DN-98	DN-87	DN-95
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP
Page Number	IF/5-47	IF/5-50	IF/5-53	IF/5-61	IF/5-68

+ New Product

Hot Swap Power Managers (cont.)

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3921	UCC3995+	UCC3996+		
Voltage Range	–10.5V to External Limitation	2.75V to 5.5V	2.75V to 13.6V Two Supplies Sequenced		
Current Range	Externally Limited	Externally Limited	Externally Limited		
Integrated Power FET	N	N	N		
RDSon	N/A	N/A	N/A		
Programmable Fault Threshold	Y	Y	Y		
Programmable Time Delay	Y	Y	Y		
Latched Fault Mode	Y	N	Y		
Average Power Limiting	Y	Y	Y		
Application / Design Note					
Available Package	SOIC or PDIP	TSSOP or SOIC	TSSOP, SOIC or PDIP		
Page Number	IF/5-78	IF/5-98	IF/5-100		

Special Functions	UNITRODE PART NUMBER				
	UCC3831	UCC38531	UCC3981+	UCC39811+	UCC3985+
Part Name	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	CompactPCI Hot Swap Power Manager
Description	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Fully CompactPCI Compliant. Four Channels for Individual Control of Four Supplies 12V, –12V, 5V, and 3.3V
Application / Design Note					
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-3	IF/5-6	IF/5-88	IF/5-91	IF/5-94

+ New Product

Drivers / Receivers Transceivers

Interface Drivers, Receivers	UNITRODE PART NUMBER				
	UC5170C	UC5171	UC5172	UC5180C	UC5181C
Drivers	8	8	8		
Receivers				8	8
Power	±10V	±10V	±10V	+5V	+5V
EIA232 / V.28	Y	Y	Y	Y	Y
EIA423 / V.10	Y	Y	Y	Y	Y
EIA422 / V.11	N	N	N	Y	Y
V.35	N	N	N	Y	Y
Appletalk	N	N	N	N	Y
Page Number	IF/6-3	IF/6-7	IF/6-11	IF/6-15	IF/6-18

+ New Product

Interface Transceivers	UNITRODE PART NUMBER				
	UC5350	UC5351+			
Drivers	1	1			
Receivers	1	1			
Power	+5V	+5V to 24V			
Control Area Network	Y	Y			
Device Net	Y	Y			
SDS	Y	Y			
Page Number	IF/6-21	IF/6-27			

+ New Product

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- 5V V_{CC} operation
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from V_{CC} to first backup battery and from first backup battery to second backup battery
- Battery internally isolated until power is first supplied
- Industrial temperature range available

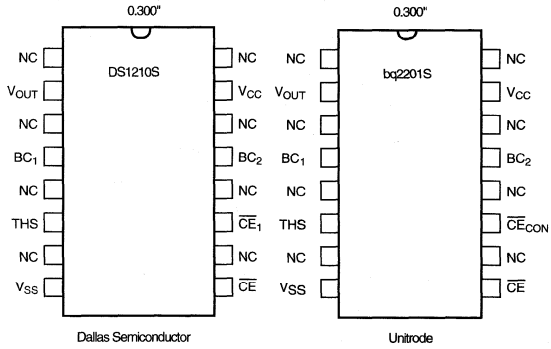
Static-RAM Nonvolatile Controller Selection Guide

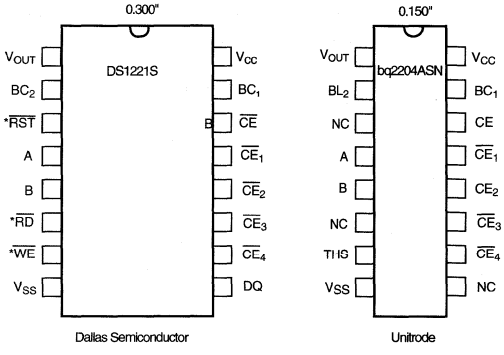
SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8 / NDIP, NSOIC 16 / NSOIC	bq2201	NV/3-3
2		✓	160 mA	16 / NDIP, NSOIC	bq2202	NV/3-11
2	✓	✓	160 mA	16 / NDIP, NSOIC	bq2203A	NV/3-19
4			160 mA	16 / NDIP, NSOIC	bq2204A	NV/3-27
2		✓	160 mA	12 / DIP module	bq2502	NV/3-35

Static-RAM Nonvolatile Controller Cross-Reference	
Dallas Semiconductor	**Unitrode**
DS1210	bq2201PN [1, 2]
DS1210S	bq2201S [1, 2]
DS1218	bq2201PN [1, 2]
DS1218S	bq2201SN [1, 2]
DS1221	bq2204APN [1, 3]
DS1221S	bq2204ASN [1, 3, 4]

Notes:

1. Unitrode's bq2201 and bq2204A do not incorporate a "check battery status" function.
2. Unitrode's bq2201 pins THS and BC_2 should be tied to V_{SS}.
3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.
4. Unitrode's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.





*These pairs must be connected to ground if the security option is not used.

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's NVSRAMs integrate extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell in either a single DIP package or a two-piece LIFETIME LITHIUM SMT module. The NVSRAMs combine secure long-term nonvolatility (more than 10 years without power) with standard SRAM pinouts and fast, unlimited read/write operation.

- ➤ Data retention without power
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10 or 5 years minimum data retention in the absence of power
- ➤ Battery internally isolated until power is first supplied
- ➤ Industrial temperature range available

Nonvolatile Static RAM Selection Guide

Density	Configuration	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64Kb	8Kb x 8	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/Y	NV/5-3
256Kb	32Kb x 8	70[2], 100, 150[2], 200	10 years	28 / DIP	bq4011/Y	NV/5-13
1Mb	128Kb x 8	70[2], 85[2], 120	10 years	32 / DIP 32 / SMT	bq4013/Y	NV/5-23
2Mb	256Kb x 8	85, 120	10 years	32 / DIP	bq4014/Y	NV/5-33
4Mb	512Kb x 8	70, 85, 120	10 years	32 / DIP 32 / SMT	bq4015/Y	NV/5-42
8Mb	1024Kb x 8	70	10 years	36 / DIP	bq4016Y	NV/5-52
16Mb	2048Kb x 8	70	5 years	36 / DIP	bq4017Y	NV/5-61
64Kb	8kB x 8	70	10 years	28 / SNAPHAT	bq4310/Y+	NV/5-70
256Kb	32kB x 8	70[3], 100[5]	10 years	28 / SNAPHAT	bq4311Y/L[4]+	NV/5-81

Notes:
1. "Y" version denotes 10% V_{CC} tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. "Y" version only.
4. "L" version denotes 3.2V typical Vcc operation.
5. "L" version only.

+ New Product

Nonvolatile Static RAM Cross-Reference			
Density	Dallas Semiconductor	STMicroelectronics	Unitrode
64Kb	DS1225AB	M48Z08	bq4010
	DS1225AD	M48Z18	bq4010Y
	-	M48Z58	bq4010/4823Y
	DS1225Y	M48Z58Y	bq4010Y
256Kb	DS1230AB	M48Z35	bq4011
	DS1230Y	M48Z35Y	bq4011Y/4833Y
1M	DS1245AB	M48Z128	bq4013
	DS1245Y	M48128Y	bq4013Y
2M	DS1258AB	-	bq4014
	DS1258Y	-	bq4014Y
4M	DS1250AB	M48Z512A	bq4015
	DS1250Y	M48Z512AY	bq4015Y
8M	DS1265AB	-	bq4016
	DS1265Y	-	bq4016Y
16M	DS1270AB	M48Z2M1	bq4017
	DS1270Y	M48Z2M1Y	bq4017Y

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each *module* is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for data and configuration storage in computers, portable equipment, office machines, and other applications.

- ➤ Clock/calendar counts seconds through years with daylight savings and leap-year adjustments
- ➤ IBM PC AT-compatible clocks include:
  - — 5- or 3-Volt operation
  - — 114, 240, or 242 bytes of user nonvolatile RAM storage
- ➤ 32kHz output for power management
- ➤ Nonvolatile control for an external SRAM
- ➤ SRAM-based clocks feature:
  - — SRAM interface
  - — Up to 512 kilobytes of NVSRAM
  - — CPU supervisor
- ➤ One minute per month clock accuracy in modules
- ➤ IC versions require only a crystal and battery

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Supervisor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 / DIP, SOIC	bq3285	NV/4-3
242		Muxed	5V	✓		24 / DIP, SOIC, SSOP	bq3285E	NV/4-22
242		Muxed	5V	✓		24 / SSOP	bq3285EC/ED	NV/4-46, NV/4-69
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	NV/4-22
242		Muxed	3V	✓		24 / SSOP	bq3285LC/LD	NV/4-46, NV/4-69
240		Muxed	3V			24 / SSOP	bq3285LF+	NV/4-92
114		Muxed	5V			24 / DIP module	bq3287/A	NV/4-111
242		Muxed	5V	✓		24 / DIP module	bq3287E/EA	NV/4-115
242		Muxed	3V			24 / DIP Module	bq3287LD+	NV/4-119
114	✓	Muxed	5V			24 / DIP, SOIC	bq4285	NV/4-123
114	✓	Muxed	5V	✓		24 / DIP, SOIC, SSOP,	bq4285E	NV/4-143
114	✓	Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq4285L	NV/4-143
114	✓	Muxed	5V			24 / DIP module	bq4287	NV/4-168
0		SRAM	3V		✓	28 / DIP, SOIC 28 / SNAPHAT	bq4802+	NV/4-174
8K	✓	SRAM	5V		✓	28 / DIP module	bq4822Y	NV/4-176
8K		SRAM	5V			28 / SNAPHAT	bq4823Y+	NV/4-191

+ New Product

Real-Time Clock Selection Guide (Continued)

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	CPU Supervisor	Pins / Package	Part Number	Page Number
32K		SRAM	5V		28 / DIP module	bq4830Y	NV/4-205
32K		SRAM	5V	✓	32 / DIP module	bq4832Y	NV/4-218
32K		SRAM	5V		28 / SNAPHAT	bq4833Y+	NV/4-233
128K		SRAM	5V	✓	32 / DIP module	bq4842Y	NV/4-247
0	✓	SRAM	5V	✓	28 / DIP, SOIC	bq4845/Y	NV/4-262
0	✓	SRAM	5V	✓	28 / DIP module	bq4847/Y	NV/4-279
512K		SRAM	5V	✓	32 / DIP module	bq4850Y	NV/4-282
512K		SRAM	5V	✓	36 / DIP module	bq4852Y	NV/4-295

+ New Product

Real-Time Clock Cross-Reference

Dallas Semiconductor	STMicroelectronics	Unitrode
DS1285/885	-	bq3285P
DS1285S/885S	-	bq3285S
DS1287/887	-	bq3287MT
DS1287A/887A	M48T86	bq3287A
DS14285	-	bq4285
DS14285	-	bq4285P
DS14285S	-	bq4285S
DS14287	-	bq4287
DS1643	M48T08/T18 M48T58Y/59Y	bq4822Y
DS1644	M48T35	bq4830Y[1]
DS1646	-	bq4842Y[2]

Notes:
1. Memory upgrade.
2. Additional bq4842 features: microprocessor reset, watchdog monitor, clock alarm, and periodic interrupt.

Portable Power (PP) Selection Guides

Unitrode battery charge-management ICs provide full-function, safe charge control for all types of rechargeable chemistries. Functions include pre-charge qualification and conditioning, charge regulation, and termination.

- Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- Flexible charge regulation support:
  - Linear
  - Switch-mode
  - Gating control (external regulator)
- Easily integrated into systems or as a stand-alone charger
- Direct LED outputs display battery and charge status
- Fast, safe, and reliable chemistry-specific charge-termination methods, including rate of temperature rise ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), peak voltage detect (PVD), minimum current, maximum temperature, maximum voltage, and maximum time
- Optional top-off and maintenance charging
- Discharge-before-charge option for NiCd
- Complete set of development tools available for quick product-desig

Battery Charge-Management Selection Guide

Battery Technology	Key Features	Fast-Charge Termination Method	Pins / Package	Part Number	Page Number
Multi-Chemistry	Complete change management with integrated switching controller	PVD, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000+	PP/3-7
		$\Delta T/\Delta$, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000T+	PP/3-20
NiMH, NiCd	Gating control of an external regulator	$-\Delta V$, PVD, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002/C/E/F/G	PP/3-3
		$\Delta T/\Delta t$, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002D/T	PP/3-3
	PWM Controller	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.300" SOIC	bq2003	PP/3-73
	PWM controller, enhanced display mode	$-\Delta V$, PVD, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2004/E/H	PP/3-5
	Dual sequential charge-controller for 2-bay chargers	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	20/0.300" DIP, 20/0.300" SOIC	bq2005	PP/3-119
Lithium Ion	PWM controller	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2054	PP/3-6
	Low-dropout linear with AutoComp™ feature	-	8/0.150" SOIC	bq2056/T/V	PP/3-186
	PWM controller, enhanced display mode	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2954+	PP/3-6
	PWM controller, differential current sense	Minimum current, maximum time	20/0.300" DIP, 20/0.300" SOIC	UCC3956	PP/3-6

+ New Product

Continued on next page

Battery Charge-Management Selection Guide (Continued)

Battery Technology	Key Features	Fast-Charge Termination Method	Pins/ Package	Part Number	Page Number
Lead Acid	PWM controller, 3 charge algorithms	Maximum voltage, $-\Delta^2V$, minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2031	PP/3-154
	Linear controller	Maximum voltage, minimum current	16/0.300" DIP 16/0.300"SOIC	UC3906	PP/3-237
	PWM controller, differential current sense	Maximum voltage, minimum current	20/0.300" DIP 20/0.300"SOIC	UC3909	PP/3-244
Rechargeable Alkaline	2-cell charging	Maximum voltage	8/0.300"DIP, 8/0.150" SOIC	bq2902	PP/3-194
	3- or 4-cell charging	Maximum voltage	14/0.300" DIP, 14/0.150" SOIC	bq2903	PP/3-204

The bq2002 fast-charge control ICs are low-cost CMOS battery charge-control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply or by replacement of the battery. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input. In some versions, this input may be used to synchronize voltage sampling. A low-power standby mode reduces system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Direct LED output displays charge status
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- Top-off and pulse-trickle charge rates available
- Synchronized voltage sampling available
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC packaging

bq2002 Family Selection Guide

	Part Number						
	$-\Delta V$ or PVD Termination					$\Delta T/\Delta t$ Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Fast charge time limit options (minutes)	160/80/40	160/100/40	160/80/40	200/80/40	160/80/40	320/80/40	440/110/55
Hold-off period options (seconds)	600/300/10	600/300/10	300/150/75	300/150/75	300/150/75	none	none
Top-off options	C/32,C/16,0	C/32,C/16,0	none	C/16,0	C/16,0	C/64,C/16,0	none
Top-off period	4.6ms	4.6ms	n/a	1.17s	1.17s	4.6ms	n/a
Pulse-trickle options	C/64,C/32	C/64,C/32	C/32	C/32	C/32	C/256,C/128	none
Pulse-trickle period	9 or 18ms	9 or 18ms	1.17s	1.17s	1.17s	18 or 73ms	n/a
Synchronized voltage sampling	no	no	yes	yes	yes	no	no
Minimum voltage pre-charge qualification	no	no	yes	yes	yes	no	no

Continued on next page

bq2002 Family Selection Guide (Continued)

	Part Number						
	-ΔV or PVD Termination					ΔT/Δt Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Hysteresis on high-temperature cut-off	no	no	no	no	no	yes	yes
LED in "charge pending" phase	n/a	n/a	flashes	flashes	flashes	on	off
Page number	PP/3-35	PP/3-35	PP/3-43	PP/3-61	PP/3-61	PP/3-51	PP/3-51

The bq2004 fast-charge control ICs are low-cost CMOS battery charge control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Integration of PWM current control circuitry allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2004 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply, replacement of the battery, or a logic-level pulse. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input, which also puts the IC into a low-power standby mode, reducing system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Integrated PWM closed-loop current control
- Configurable, direct LED output displays charge status
- Low-power mode
- Top-off and pulse-trickle charging available
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- 16-pin 300-mil DIP or 150-mil SOIC packaging

bq2004 Family Selection Guide

Feature	Part Number bq2004	bq2004E	bq2004H
Maximum time-out selections (minutes)	360/180/90/45/23	325/154/77/39/19	650/325/154/77/39
Hold-off period selections (seconds)	137/820/410/200/100	137/546/273/137/68	273/546/546/273/137
Charge rate during hold-off period	full fast-charge rate	1/8*fast-charge rate	1/8*fast-charge rate
Top-off options	C/2,C/4,C/8,C/16,0	C/2,C/4,C/8,C/16,0	C/4,C/8,C/16,C/32,0
Top-off pulse width/period (seconds)	260/2080	260/2080	260/2080
Top-off duration	MTO	0.235*MTO	0.235*MTO
Pulse-trickle selections	C/32,C/64,0	C/512,0	C/512,0
Pulse-trickle period (ms)	4.17/8.3/16.7/33.3/66.7	66.7/133/267/532	33.3/66.7/133/267
Pulse-trickle pulse width (seconds)	260	260	260
DSEL floating disables pulse-trickle	no	yes	yes
VSEL high disables low-temperature fault threshold	yes	no	no
High-temperature fault threshold	1/4LTF + 3/4 TCO	1/3LTF + 2/3 TCO	1/3LTF + 2/3 TCO
Page number	PP/3-91	PP/3-105	PP/3-105

Li-Ion PWM Charge IC Selection Guide

Feature	Part Number bq2054	bq2954	UCC3956
Charge algorithm	During pre-qualification, the bq2054 charges using a low trickle current if the battery voltage is low. Then it charges using constant current followed by constant volatge. After fast-charge termination, charge is re-initiated by resetting the power to the IC or by inserting a new battery.	Performs similar to the bq2054, but the bq2954 also re-initiates a recharge if the battery voltage falls below a threshold level. This allows the bq2954 to maintain a full charge in the battery at all times.	Uses a 4-step charge algorithm: low-current trickle charge (when the cell voltage is below a user- programmable level); high- current bulk charge; constant-voltage overcharge; optional top-off with user-programmable timer
Current-sensing technique	Low-side current sensing	Low-side and high-side current sensing	Fully differential high-side current sensing can be used up to 20V common mode without the need for external level shifting.
Charge initiation	Application of power or detection of battery insertion	Application of power or detection of battery insertion	One-shot charge initiates charging, or a simple comparator initiates charging on battery insertion.
Detection of deeply discharged (bad) cells	Minimum cell voltage required for fast charge: 2V/cell Trickle-charge period: 1 * MTO	Minimum cell voltage required for fast charge: 3V/cell Trickle-charge period: 0.25 * MTO (for faster detection of bad cells)	User-programmable threshold limits charge current when battery cells are deeply discharged and provides short-circuit protection.
Charge termination based on minimum current	User-programmable minimum current is a ratio of the charging current: 1/10, 1/20, 1/30. A safety charge timer is also available.	User-programmable minimum current is a ratio of the charging current: 1/10, 1/15, 1/20. A safety charge timer is also available.	User-programmable minimum current or user-programmable overcharge timer
Temperature monitoring	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	No
Status display	3 LEDs for state of charge	2 LEDs or one bi-color LED optimize state of charge	2 LEDs for state of charge including end of charge
Full-charge indication	LEDs indicate full charge after charge termination	LEDs indicate full charge just before charge termination	LEDs indicate full charge on charge termination
Input voltage range	4.5V to 5.5V	4.5V to 5.5V	6.5V to 20V
Typical supply current	2mA	2mA	5mA
Voltage regulation accuracy	±1% at 25°C	±1% at 25°C	±1% at 25°C
Wakeup feature for battery pack protectors	No	Yes	No
Integrated PWM controller	Yes	Yes	Yes
Pins/package	16-pin narrow PDIP or SOIC	16-pin narrow PDIP or SOIC	20-pin SOIC or DIP
Page number	PP/3-170	PP/3-217	PP/3-253

Portable Power (PP) Selection Guides

Unitrode's Gas Gauge ICs measure the available charge, calculate self-discharge, and communicate the available charge of a battery pack over a serial port or by directly driving an LED display.

- ➤ Accurate measurement of available charge for nickel cadmium, nickel metal-hydride, lithium ion, lead-acid batteries, and primary lithium
- ➤ Designed for battery-pack integration
- ➤ 150µA or less typical operating current
- ➤ Serial port or direct LED display for remaining battery capacity indication
- ➤ Available capacity is compensated for charge/discharge rate and temperature
- ➤ Accurately measures across a wide range of currents

Battery Capacity-Monitoring ICs Selection Guide

Battery Technology	Approximate Pack Capacity (mAh)	Communication Interface	Additional Key Features	Pins / Package	Part Number	Page Number
NiCd/NiMH	800-5000	1-wire DQ	5 or 6 LED outputs	16 /SOIC	bq2010	PP/4-3
			Slow-charge control	16 /SOIC	bq2012	PP/4-81
			External charge-control support	16 /SOIC	bq2014	PP/4-123
		1-wire HDQ	Register-compatible with bq2050H	16 /SOIC	bq2014H+	PP/4-149
NiCd	800-2000	1-wire DQ	See bq2011 Family Selection Guide	16 /SOIC	bq2011 bq2011J bq2011K	PP/4-24, PP/4-45, PP/4-63
NiCd/NiMH/ Lead Acid	2000-10,000	1-wire HDQ	Programmable offset and load compensation	16 /SOIC	bq2013H	PP/4-103
Li-Ion	800-5000	1-wire DQ	Remaining power (Wh) indication	16 /SOIC	bq2050	PP/4-215
		1-wire HDQ	Register-compatible with bq2014H	16 /SOIC	bq2050H	PP/4-237
Primary Lithium	800-15,000	1-wire HDQ	Programmable discharge efficiency compensation	16 /SOIC	bq2052+	PP/4-259
NiCd/NiMH Lead Acid/ Li-Ion	800-10,000	2-wire SMBus	SBS rev. 1.0-compliant	16 /SOIC	bq2040	PP/4-185
			SBS rev. 0.95-compliant	16 / SOIC	bq2092	PP/4-314
			SBS rev. 1.0-compliant with 5 LEDs	16 /SOIC	bq2945	PP/4-340
		2-wire SMBus or 1-wire HDQ16	SBS rev. 1.1-compliant	28 / SSOP	bq2060+	PP/4-276
Any	Any	1-wire HDQ	Analog peripheral for µC	8 / SOIC or TSSOP	bq2018	PP/4-170

+ New Product

The bq2011 Gas Gauge ICs provide accurate capacity monitoring of rechargeable batteries in high discharge rate environments. The ICs can monitor a wide range of charge/discharge currents using the onboard V-to-F converter and a low-value sense resistor. The ICs track remaining capacity (NAC) and compensate it for battery self-discharge, charge/discharge rate, and temperature. Five LEDs can communicate remaining capacity in 20% increments. A serial port allows a host microcontroller to access the nonvolatile memory registers containing battery capacity, voltage, temperature, and other critical parameters.

- Accurate measurement of available charge in rechargeable batteries
- Designed for NiCd high discharge rate applications
- Drives 5 LEDs for capacity indication
- Automatic charge self-discharge and discharge compensation
- Low operating current
- 16-pin narrow SOIC

bq2011 Family Selection Guide

Feature	Part Number bq2011	bq2011J	bq2011K
Display	Relative or absolute	Absolute	Absolute
Programmed Full Count (PFC) range	4.5–10.5mVh	2.21–3.81mVh	2.21–3.81mVh
Nominal Available Capacity (NAC) on reset	NAC = 0	NAC = PFC or 0	NAC = PFC or 0
Self-discharge rate	NAC/80	NAC/80 or disabled	NAC/80 or disabled
Charge compensation	75–95% based on rate and temperature	65–95% based on rate and temperature	70–95% based on rate and temperature
Discharge compensation	75–100% plus temperature compensation	75–100% plus temperature compensation	100%
End-of-discharge voltage	0.9V/cell	0.9V/cell	0.96–1.16V/cell
Page number	PP/4-24	PP/4-45	PP/4-63

Portable Power (PP) Selection Guides

Unitrode's battery management module products provide true turn-key solutions for capacity monitoring and charge control of NiCd, NiMH, Li-Ion, or Rechargeable Alkaline battery packs. Designed for battery pack integration, the small boards contain all necessary components to easily implement intelligent or smart battery packs in a portable system. The wide selection of boards offers battery monitoring, capacity tracking, charge control, and remaining capacity communication to the host system or user. The boards are fully tested and provide direct cell connections for simple battery packs.

- ➤ Turnkey solutions for intelligent or smart batteries for portable equipment
  - — Computers, cellular phones, and camcorders
  - — Handheld terminals
  - — Communication radios
  - — Medical and test equipment
  - — Power tools
- ➤ Capacity monitoring and charge control
- ➤ Pushbutton-activated LED capacity indication
- ➤ Designed for battery pack integration
  - — Small size
  - — Low power
  - — Direct cell connections

Battery-Management Modules Selection Guide

Battery Technology	Key Features	Part Number	Page Number
NiCd/NiMH	Capacity monitoring, LED indication, serial communications port	bq2110	PP/5-2
	Capacity monitoring, slow-charge control, LED indication, serial communications port	bq2112	PP/5-14
	Capacity monitoring, charge control output, LED indication, serial communications port	bq2114	PP/5-24
	Capacity monitoring and fast charge control	bq2164	PP/5-71
NiCd	Capacity monitoring for high discharge rates, LED indication	bq2111L	PP/5-8
NiCd/NiMH, Lead Acid	Capacity monitoring, LED indication, single-wire serial communications port	bq2113H+	PP/5-20
Li-Ion	Capacity monitoring, Smart Battery data set and interface, LED indication, pack supervision, 4-segment LED indication	bq2148	PP/5-40
	Capacity monitoring, LED indication, serial communications port	bq2150 bq2150/H	PP/5-47 PP/5-53
	Pack supervision: overvoltage, undervoltage, and overcurrent control	bq2158 bq2158T	PP/5-57 PP/5-64
	Capacity monitoring, 3- or 4-cell pack supervision, and LED indication	bq2167+ bq2168+	PP/5-77 PP/5-85
NiCd/NiMH/ Lead Acid/ Li-Ion	Capacity monitoring, Smart Battery data set and interface, 5-segment LED indication	bq2145	PP/5-34
	Capacity monitoring, Smart Battery data set and interface, 4-segment LED indication	bq219XL	PP/5-93
Any	Charge and discharge counting, serial communication port, single-wire interface	bq2118	PP/5-30

+ New Product

Unitrode Lithium Ion Pack-Protection ICs provide reversible overvoltage, undervoltage, and overcurrent protection for lithium ion battery packs.

- ➤ Protects one to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- ➤ User-selectable thresholds mask-programmable by Unitrode
- ➤ Designed for battery-pack integration
  - — Small outline package, minimal external components and space, and low cost

Pack-Protection and Supervisory ICs Selection Guide

Battery Technology	Number of Cells Protected	Protection Types	Key Features	Pins / Package	Part Number	Page Number
Lithium Ion	3 or 4	Overvoltage, overcurrent, and undervoltage	Very low power	16/0.150" SOIC	bq2058	PP/6-2
	2				bq2058T	PP/6-14
		Overcharge, overdischarge, overcurrent	Internal MOSFET (80mΩ total)		UCC3911	PP/6-26
	1		Internal MOSFET (50mΩ total)	16/0.150" TSSOP	UCC3952+	PP/6-32
	3 or 4	Overvoltage, undervoltage, overcurrent	Smart-discharge circuitry	16/0.150" SSOP	UCC3957	PP/6-37
	1	Overcharge, overdischarge, overcurrent	Internal MOSFETS (50mΩ total)	16/0.150" SOIC	UCC3958	PP/6-44

+ New Product

Power-Management ICs Selection Guide

Features	Part Number: UCC3581	UCC3809 -1/2	UCC3800/ 1/2/3/4/5	UCC3813- 0/1/2/3/4/5
Topology	Forward, flyback	Forward, flyback, buck, boost	Forward, flyback, buck, boost	Forward, flyback, buck, boost
Input voltage	Off-line AC	Off-line AC	Off-line AC, battery	Off-line AC, battery
Output voltage	NA	NA	NA	NA
Operating mode	Fixed/variable frequency	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)
Output	1A FET drives	0.8A FET drives	1A FET drives	1A FET drives
Output power	N / A	N / A	N / A	N / A
Supply current	300µA	500µA	500µA	500µA
Power limit	Yes	No	Yes	Yes
Application/design note	DN-48, DN-65	DN-65, DN-89, U-165, U-168	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97
Pin count ❖	14	8	8	8
Page number	PS/8-128	PS/8-192	PS/8-169	PS/8-206

❖The smallest available pin count for thru-hole and surface-mount packages.

Power-Management ICs Selection Guide (Continued)

Features	Part Number: UCC39401	UCC3941 -3/-5/-ADJ	UCC39411 /2/3+	UCC39421/2+	UCC3946	UCC3954
Topology	Boost / battery charger	Boost	Boost	Boost/SEPIC/ flyback	Watchdog/ reset	Flyback
Input voltage	0.8V to (V_{OUT} + 0.5V)	0.8V to (V_{OUT} + 0.5V)	1.1V to (V_{OUT} + 0.5V)	1.8V–8V	2.1V–5.5V	2.5V–4.2V
Output voltage	ADJ to 5.0V	3.3V, 5V, ADJ	3.3V, 5V, ADJ	ADJ	V_{IN}–0.3V	3.3V
Operating mode	Variable frequency	Variable frequency	Variable	Fixed/variable frequency	Watchdog/ reset	Fixed frequency (200kHz)
Output	Internal power FETs	Internal power FETs	Internal power FETs	FET Drives	NA	Internal power FETs
Output power	200mW	500mW (1 cell) 1W (2 cells)	200mW	NA	NA	2W
Supply current	55µA	80µA	48µA	635µA	10µA	1mA
Power limit	Yes	Yes	Yes	Yes	NA	Yes
Application/ design note	-	DN-73	DN-97	-	-	DN-86
Pin count ❖	20	8	8	16/20	8	8
Page number	PP/7-34	PP/7-48	PP/7-58	PP/7-66	PP/7-88	PP/7-93

+ New Product
❖The smallest available pin count for thru-hole and surface-mount packages.

Linear Controller ICs Selection Guide

Features	Part Number UC3832	UC3833	UC3834	UC3835	UC3836	UCC3837
Type of output	Positive adjustable	Positive adjustable	Positive/ negative adjustable	5V fixed	Positive adjustable	Positive adjustable
Maximum input voltage	36V	36V	40V	40V	40V	12V
Minimum output voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V	1.5V
Output drive	300mA	300mA	350mA	500mA	500mA	1.5mA
Type of short circuit limit	Duty cycle	Duty cycle	Foldback	Foldback	Foldback	Duty cycle
Reference voltage accuracy	2%	2%	3% / 4%	2%	2%	2%
Special features	Multiple pins accessible	-	-	Built-in Rsense	Built-in Rsense	Internal charge pump; Direct N-FET drive
Application/ design note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95			-
Pin count ❖	14, 16	8, 16	16	8, 16	8, 16	8
Page number	PS/3-11	PS/3-11	PS/3-18	PS/3-24	PS/3-24	PS/3-28

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide

Features	Part Number UCC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V/ adjustable
Dropout voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output voltage accuracy	2.5%	1%	1%	1%	1%
Maximum input voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown current	10µA	-	-	-	-
Operating current	400µA	-	-	-	-
Line regulation	0.01% / V	-	-	-	-
Load regulation	0.1%, I_{OUT} = 0 to 1A	-	-	-	-
Special features	Power limit	Fast transient response	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	8	5	5	5	5
Page number	PP/7-5	PS/3-5	PS/3-5	PS/3-5	PS/3-5

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UCC383	UCC384	UC385-1	UC385-2	UC385-3
Output voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output voltage accuracy	2.5%	2.5%	1%	1%	1%
Maximum input voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown current	40µA	17µA	-		
Operating current	400µA	240µA	-		
Line regulation	0.01% / V	0.01% / V	-		
Load regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA	-		
Special features	Power limit	Power limit	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	3	8	5	5	5
Page number	PP/7-12	PP/7-19	PS/3-35	PS/3-35	PS/3-35

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UC385-ADJ	UC386+	UC387+	UC388+
Output voltage	1.2V/adjustable	3.3V	5V	Adjustable down to 1.25V
Dropout voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA
Output voltage accuracy	1%	1.5%	1.5%	1.5%
Maximum input voltage	7.5V	9V	9V	9V
Shutdown current	-	2µA	2µA	2µA
Operating current	-	10µA	10µA	10µA
Line regulation	-	25mV max	25mV max	25mV max
Load regulation	-	10mV max	10mV max	10mV max
Special features	Fast transient response	TSSOP	TSSOP	TSSOP
Pin count ❖	5	8	8	8
Page number	PS/3-35	PP/7-29	PP/7-29	PP/7-29

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Special Function Linear Regulation ICs Selection Guide

Features	Part number UC560	UCC561+	UC563+
Type of output	Positive	Positive	Positive
Application	Source/sink regulator for the 18- and 27-line SCSI termination	LVD SCSI regulator for the 18- and 27-line termination	32-line VME bus bias generator
Input voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V
Output voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V
Dropout voltage	0.9V at 750mA	-	-
Bus standard	SCSI-1,2,3	SPI-2, 3	VME / VME64
Sink/source current	300mA / –750mA	200mA / –200mA	475mA / –575mA
Application/design note	-	-	-
Pin count ❖	5, 8	16	3, 8
Page number	IF/4-3	IF/4-7	IF/4-10

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Back-Light Controller ICs Selection Guide

Features	Part Number UC3871	UC3872	UCC3972+
Application	Fluorescent lamp driver with LCD Bias	Fluorescent lamp driver	Fluorescent lamp driver
Voltage range	4.5V–20V	4.5V–24V	4.5V–25V
Reference tolerance	1.2%	1.2	NA
Open lamp detect	Yes	Yes	Yes
PWM synchronization	Yes	Yes	Yes
PWM frequency	Programmable	Programmable	80kH–160kH
Analog dimming	Yes	Yes	Yes
Low-frequency dimming	Yes	Yes	Yes
Operating current	8mA	6mA	1mA
Package	18-pin SOIC	16-pin SSOP	8-pin TSSOP
Application/design note	U-141, U-148	DN-75, U-141, U-148	-
Page number	PP/8-2	PP/8-8	PP/8-13

+ New Product

IrDA Selection Guide

Device Type	Supply Voltage	Data Rate	Dynamic Range	Quiescent Current	Encoder/ Decoder	IrDA Compliant	LED Driver	Part Number	Page Number
Receiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	250µA	N	Y	N/A	UCC5341	PP/9-2
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100m A	250µA	N	Y	500mA	UCC5342	PP/9-6
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	280µA	Y	Y	500mA	UCC5343	PP/9-10

PWM Control

PWM Control

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3800	UCC3801	UCC3802	UCC3803	UCC3804
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-173	PS/3-173	PS/3-173	PS/3-173	PS/3-173

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3805	UCC3806	UCC3807-1	UCC3807-2	UCC3807-3
Application	DC-DC and Battery	Isolated Output, Push-pull Controller	DC-DC	Off-line	DC-DC and Battery
Topology	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1.5%	1%	1.5%	1.5%	1.5%
Peak Output Current	1A	0.5A	1A	1A	1A
Under Voltage Lockout	4.1V / 3.6V	7.5V / 6.75V	7.2V / 6.9V	12.5V / 8.3V	4.3V / 4.1V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y		Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	50% / 50%	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal		Y			
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-45, DN-51, DN-65, U-97, U-110, U-144	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A
Pin Count ❖	8	16	8	8	8
Page Number	PS/3-173	PS/3-180	PS/3-187	PS/3-187	PS/3-187

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3808-1	UCC3808-2	UCC3809-1	UCC3809-2	UCC3810
Application	Off-line	DC-DC and Battery	DC-DC	Off-line	Dual PWM Controller, Off-line, DC-DC
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	2%	2%	5%	5%	1.5%
Peak Output Current	0.5A Source, 1A Sink	0.5A Source, 1A Sink	0.4A Source, 0.8A Sink	0.4A Source, 0.8A Sink	1A
Under Voltage Lockout	12.5V / 8.3V	4.3V / 4.1V	10V / 8V	15V / 8V	11.3V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual, Totem Pole
Startup Current	130µA	130µA	100µA	100µA	150µA
Leading Edge Blanking					Y
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	50% / 50%	50% / 50%	90%	90%	50%
Separate Oscillator / Synchronization Terminal			N/A	N/A	Y
Application / Design Note	DN-65, U-97, U-110, U-170	DN-65, U-97, U-110, U-170	DN-65, DN-89, U-165, U-168	DN-65, DN-89, U-165, U-168	DN-65, U-97, U-110, U-133A
Pin Count ❖	8	8	8	8	16
Page Number	PS/3-192	PS/3-192	PS/3-198	PS/3-198	PS/3-205

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-0	UCC3813-1	UCC3813-2	UCC3813-3	UCC3813-4
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-212	PS/3-212	PS/3-212	PS/3-212	PS/3-212

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-5	UC3823	UC3823A	UC3823B	UC3824
Application	DC-DC and Battery	DC-DC	DC-DC	Off-line	Synchronous Rectifier, Forward Converter
Topology	Forward, Flyback	Buck, Boost	Buck, Boost	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1%	1%	1%	1%
Peak Output Current	1A	1.5A	2A	2A	1.5A
Under Voltage Lockout	4.1V / 3.6V	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	9.2V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Complementary, Totem Pole
Startup Current	100µA	1.1mA	0.1mA	0.1mA	1.1mA
Leading Edge Blanking	Y		Y	Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	100%	Programmable, <100%	Programmable, <100%	100%
Separate Oscillator / Synchronization Terminal		Y	Y	Y	Y
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	U-97, U-111, U-131	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-111
Pin Count ❖	8	16	16	16	16
Page Number	PS/3-212	PS/3-219	PS/3-225	PS/3-225	PS/3-233

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3825	UC3825A	UC3825B	UC3826❍	UC3827-1
Application	DC-DC	DC-DC	Off-line	Secondary Side, Average Current Mode	Multiple Output or High Voltage Output DC-DC Converters
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Buck Current Fed Push-pull
Voltage Reference Tolerance	1%	1%	1%	1%	4%
Peak Output Current	1.5A	2A	2A	0.25A	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers
Under Voltage Lockout	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	8.4V / 8.0V	9V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Floating Buck, Push-pull
Startup Current	1.1mA	0.1mA	0.1mA		1mA
Leading Edge Blanking		Y	Y	N/A	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable, <50%	Programmable, <50%	90% for Buck Stage, 50% / 50% for Push-pull Stage
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	U-97, U-110, U-111	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-135, U-140	
Pin Count ❖	16	16	16	24	24
Page Number	PS/3-240	PS/3-225	PS/3-225	PS/3-247	PS/3-257

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3827-2	UCC3830-4	UCC3830-5	UCC3830-6	UCC3839 ❍
Application	Multiple Output or High Voltage Output DC-DC Converters	Microprocessor Power	Microprocessor Power	Microprocessor Power	Secondary Side, Average Current Mode Control
Topology	Buck Voltage Fed Push-pull	Buck	Buck	Buck	Any Topology
Voltage Reference Tolerance	4%	1%*	1%*	1%*	1%
Peak Output Current	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers	1.5A	1.5A	1.5A	10mA to Drive Opto-coupler
Under Voltage Lockout	9V / 8.4V	10.5V / 10V	10.5V / 10V	10.5V / 10V	
Maximum Practical Operating Frequency	500kHz	100kHz	200kHz	400kHz	1MHz
Outputs	Floating Buck, Push-pull	Single	Single	Single	Opto-coupler Drive
Startup Current	1mA				
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	90% for Buck Stage, 50% / 50% for Push-pull Stage	95%	95%	95%	
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note					U-140
Pin Count ❖	24	20	20	20	14
Page Number	PS/3-257	PS/3-263	PS/3-263	PS/3-263	PS/3-276

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3841	UC3842	UC3842A	UC3843	UC3843A
Application	Primary Side, Programmable, Off-line, DC-DC	Off-line	Off-line	DC-DC	DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout		16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Open Collector	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	4.5mA	1mA	0.5mA	1mA	0.5mA
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	Programmable	100%	100%	100%	100%
Separate Oscillator / Synchronization Terminal					
Special Features			Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current
Application / Design Note	DN-28	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111
Pin Count❖	18	8, 14	8, 14	8, 14	8, 14
Page Number	PS/3-281	PS/3-289	PS/3-296	PS/3-289	PS/3-296

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3844	UC3844A	UC3845	UC3845A	UC3846
Application	Off-line	Off-line	DC-DC	DC-DC	Off-line, DC-DC
Topology	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	0.5A
Under Voltage Lockout	16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V	7.7V / 6.95V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	1mA	0.5mA	1mA	0.5mA	
Leading Edge Blanking					
Soft Start					Y
Maximum Duty Cycle	50%	50%	50%	50%	50% / 50%
Separate Oscillator / Synchronization Terminal					Y
Special Features		Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current	
Application / Design Note	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-45, U-93, U-97, U-100A, U-111
Pin Count ❖	8, 14	8, 14	8, 14	8, 14	16
Page Number	PS/3-289	PS/3-296	PS/3-289	PS/3-296	PS/3-302

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3847	UC3848 ❍	UC3849 ❍	UC3851	UC3856
Application	Off-line, DC-DC	Average Current Mode, Off-line, DC-DC	Secondary Side, Average Current Mode	Off-line, Programmable, Primary Side Controller	Isolated Output, Push-pull Controller
Topology	Push-pull, Full Bridge, Half Bridge	Forward, Flyback	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	0.5A	2A	0.25A	0.2A	1.5A
Under Voltage Lockout	7.7V / 6.95V	13V / 10V	8.3V / 7.9V		7.7V / 7.0V
Maximum Practical Operating Frequency	500kHz	1MHz	1MHz	500kHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current		500µA		4.5mA	
Leading Edge Blanking		N/A	N/A	Y	
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable	50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y		Y		Y
Application / Design Note	DN-45, U-93, U-97, U-100A, U-111	U-135, U-140	U-135, U-140	DN-28	DN-45, U-93, U-97, U-110
Pin Count ❖	16	16	24	18	16
Page Number	PS/3-302	PS/3-309	PS/3-317	PS/3-327	PS/3-333

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3880-4	UCC3880-5	UCC3880-6	UCC3882	UCC3884
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power	Off-Line or DC-DC Frequency Foldback Controller
Topology	Buck	Buck	Buck	Synchronous Buck	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%*	1%*	1%*	1%*	2%
Peak Output Current	1.5A	1.5A	1.5A	1.5A	0.5A Source, 1A Sink
Under Voltage Lockout	10.5V / 10V	10.5V / 10V	10.5V / 10V	10.5V / 10V	8.9V / 8.3V
Maximum Practical Operating Frequency	100kHz	200kHz	400kHz	700kHz	750kHz
Outputs	Single	Single		Dual, N-FET Drive	Single
Startup Current					200µA
Leading Edge Blanking					
Average Current Mode	Y	Y		Y	
Foldback Current Limiting	Y	Y		Y	
Soft Start					Y
Maximum Duty Cycle	95%	95%		95%	80%
Separate Oscillator / Synchronization Terminal					Y
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	
Application / Design Note	U-140	U-140	U-140	U-140	DN-65, U-164
Pin Count ❖	24	18	16	28	16
Page Number	PS/3-373	PS/3-373	PS/3-373	PS/3-380	PS/3-393

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3886				
Application	Microprocessor Power				
Topology	Buck				
Voltage Reference Tolerance	1.5%				
Peak Output Current	1.5A				
Under Voltage Lockout	10.3V / 10.05V				
Maximum Practical Operating Frequency	400kHz				
Outputs	Single				
Startup Current					
Leading Edge Blanking					
Average Current Mode					
Foldback Current Limiting					
Soft Start					
Maximum Duty Cycle	95%				
Separate Oscillator / Synchronization Terminal					
Special Features	External Reference Input, Use with UC3910				
Application / Design Note	U-140, U-156, U-157				
Pin Count ❖	16				
Page Number	PS/3-400				

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UC2577-12	UC2577-15	UC2577-ADJ
Description	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator
Application	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications
Output Voltage	12V	15V	Adjustable
Special Features	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available
Application / Design Note	DN-47, DN-49	DN-47, DN-49	DN-49
Pin Count ❖	5	5	5
Page Number	PS/3-31	PS/3-31	PS/3-36

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER				
	UC3572	UC3573	UC3578	UCC3585+	
Application	Low Power, High Efficiency, Spot Regulator	Low Power, High Efficiency, Spot Regulator	DC-DC	Low Input Voltage Synchronous Buck Regulator with Output Voltage Tracking	
Topology	Negative Output Flyback	Buck	Buck	Voltage Mode Synchronous Buck	
Voltage Reference Tolerance	2%	2%	2%	1%	
Peak Output Current	0.5A	0.5A	0.6A Source, 0.8A Sink	0.5A	
Maximum Practical Operating Frequency	300kHz	300kHz	100kHz Internal Oscillator	700kHz	
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Floating Totem Pole	P FET/N FET Synchronous	
Startup Current			N/A	2.3mA	
Voltage Feedforward				N	
Soft Start			Y	Y	
Maximum Duty Cycle	100%	100%	90%	100%	
Separate Oscillator / Synchronization Terminal				N	
Application / Design Note		DN-70	U-167		
Pin Count ❖	8	8	16	16	
Page Number	PS/3-108	PS/3-112	PS/3-116	PS/3-154	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39401+	UCC3941	UCC39411/2/3+
Description	Low Voltage Boost Controller / Charger	1V Synchronous Boost Converter	1V Low Power Boost Controller
Application	Pager Power	High Efficiency Integrated Boost Converter	High Efficiency Low Power Synchronous Boost Conversion
Special Features	•High Efficiency Boost •1V Input •Battery Charger •Backup LDO	•Full Load Startup at 1V •Power Limit Control •Auxiliary 9V Supply •Output Disconnect •Shutdown Mode	•200mW Output Power with Battery Voltages as low as 0.8V •Power Limit Control •Adaptive Current Mode Control •Auxiliary 7V Supply •Shutdown Mode
Application / Design Note			
Pin Count ❖	20	8	8
Page Number	PP/7-34	PP/7-45	PP/7-58

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39421/2+	UCC3954	
Description	Multimode HF PWM Controller	Single Cell Lithium-Ion to 3.3V Converter	
Application	High Efficiency Boost, Sepic Flyback Converter	High Efficiency Flyback Converter	
Special Features	•2mHz Operation •1.8V Input •Current Limit •Power-on Reset •Low Voltage Detect	•Fixed 3.3V Output •750mA Output Current •Low Battery Warning •Low Battery Disconnect •Shutdown Mode	
Application / Design Note			
Pin Count ❖	16, 20	8	
Page Number	PP/7-66	PP/7-93	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3588+	UCC3830-4	UCC3830-5	UCC3830-6	UCC3880-4
Application	Synchronous Buck Regulator with 5 Bit DAC	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power
Topology	Voltage Mode Synchronous Buck	Buck	Buck	Buck	Buck
Voltage Reference Tolerance	1%	1%*	1%*	1%*	1%*
Peak Output Current	1A	1.5A	1.5A	1.5A	1.5A
Maximum Practical Operating Frequency	700kHz	100kHz	200kHz	400kHz	100kHz
Outputs	Dual NFET Synchronous	Single	Single	Single	Single
Soft Start	Y				
Average Current Mode		Y	Y	Y	Y
Foldback Current Limiting		Y	Y	Y	Y
Maximum Duty Cycle	100%	95%	95%	95%	95%
Special Features		5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor
Application / Design Note					U-140
Pin Count ❖	16	20	20	20	20
Page Number	PS/3-163	PS/3-263	PS/3-263	PS/3-263	PS/3-373

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3880-5	UCC3880-6	UCC3882		
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power		
Topology	Buck	Buck	Synchronous Buck		
Voltage Reference Tolerance	1%*	1%*	1%*		
Peak Output Current	1.5A	1.5A	1.5A		
Maximum Practical Operating Frequency	200kHz	400kHz	700kHz		
Outputs	Single	Single	Dual, N-FET Drive		
Soft Start					
Average Current Mode	Y	Y	Y		
Foldback Current Limiting	Y	Y	Y		
Maximum Duty Cycle	95%	95%	95%		
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor		
Application / Design Note	U-140	U-140	U-140		
Pin Count ❖	20	20	28		
Page Number	PS/3-373	PS/3-373	PS/3-380		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Support	UNITRODE PART NUMBER		
	UCC391+	UC3910	UCC3946
Description	5-Bit DAC 5V Operation	Reference, 4-bit DAC and Fault Monitor	Microprocessor Supervisor with Watchdog Timer
Application	Sets Control Voltage for UC3886 and other Precision PWMs	Sets Control Voltage for UC3886, UC3870 and other Precision PWMS	Accurate Microprocessor Supervision
Special Features	•5V Operation •1% Combined Reference and DAC Tolerance •Meets VID Code for Pentium II Processors	•4-bit DAC Sets Output Voltage of PWM, Meets Intel VID Code •1% Combined Reference and DAC Tolerance •Over and Under Voltage Monitoring and Protection	•Programmable Reset Period •Programmable Watchdog Period •1.5% Accurate Threshold •4mA IDD
Application / Design Note		U-157, U-158	
Pin Count ❖	8	16	8
Page Number	PS/3-434	PS/3-437	PP/7-88

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Post Regulation Controllers	UNITRODE PART NUMBER				
	UCC3583	UC3584	UC3838A		
Application	Secondary Side Post Regulation	DC-DC Secondary Side Synchronous Post Regulator	Mag-Amp Controller		
Topology	Buck	Buck			
Voltage Reference Tolerance	1.5%	1%	1%		
Peak Output Current	1.5A Source, 0.5A Sink	1.5A Source and Sink	120mA Reset Current		
Maximum Practical Operating Frequency	500kHz	1MHz			
Undervoltage Lockout	9.0V / 8.4V	10.5V / 8.8V	N/A		
Outputs	Single, Totem Pole	Single, Totem Pole			
Startup Current	100µA	N/A			
Voltage Feedforward	N/A				
Soft Start	Y	Y			
Maximum Duty Cycle	95%	94%			
Separate Oscillator / Synchronization Terminal	Y	Y			
Special Features	• For Both Single Ended and Center Tapped Secondary Circuits • Operation From Floating Supply Referenced to Output	• Can Use Existing Windings • Internally Regulated 15V Boost Supply Bias for Low Voltage Applications • Short Circuit Protection with Programmable Delay	• Dual Op-Amps • –120V Reset Driver		
Application / Design Note	DN-64	DN-64, DN-83	DN-47		
Pin Count ❖	14	16	16, 20		
Page Number	PS/3-139	PS/3-148	PS/3-272		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Secondary Side PWM Control	UNITRODE PART NUMBER				
	UC3826	UCC3839 ❍	UC3849 ❍	UCC3960+	UCC3961+
Application	Secondary Side, Average Current Mode	Secondary Side, Average Current Mode Control	Secondary Side, Average Current Mode	Primary-Side Startup Control	Primary-Side Startup Control
Topology	Forward, Flyback, Buck, Boost	Any Topology	Forward, Flyback, Buck, Boost		
Voltage Reference Tolerance	1%	1%	1%	5%	5%
Peak Output Current	0.25A	10mA to Drive Opto-coupler	0.25A	1.5A	1.5A
Undervoltage Lockout	8.4V / 8V		8.3V / 7.9V	10V / 8V	10V / 8V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	400kHz Synchronizable Switching Frequency	400kHz Synchronizable Switching Frequency
Outputs	Single, Totem Pole	Opto-coupler Drive	Single, Totem Pole	Single	Single
Startup Current				150µA	150µA
Leading Edge Blanking	N/A		N/A	N/A	N/A
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	Programmable		Programmable		Programable V-S Clamp
Separate Oscillator / Synchronization Terminal	Y		Y		
Special Features					• Multimode OVC Protection, • Programable OV and UV, • Self Bias Regulation.
Application / Design Note	U-135, U-140	U-140	U-135, U-140	DN-99	DN-99
Pin Count ❖	24	14	24	8	14
Page Number	PS/3-247	PS/3-276	PS/3-317	PS/3-442	PS/3-450

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★	UC3860
Application	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Off-line, DC-DC, Zero Current Switching
Topology	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1%
Peak Output Current	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A	2A
Undervoltage Lockout	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V	17.3V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	2MHz
Outputs	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2	Dual Programmable, Totem Pole
Startup Current	50µA	50µA	50µA	50µA	300µA
Voltage Feedforward	Y	Y	Y	Y	
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	Programmable	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-65	DN-65	DN-65	DN-65	
Pin Count ❖	16	16	16	16	24, 28
Page Number	PS/3-122	PS/3-122	PS/3-122	PS/3-122	PS/3-341

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3861	UC3862	UC3863	UC3864	UC3865
Application	Off-line, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	Off-line, Zero Current Switching
Topology	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Undervoltage Lockout	16.5V / 10.5V	16.5V / 10.5V	8V / 7V	8V / 7V	16.5V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle	50% / 50%	100%	50% / 50%	100%	50% / 50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-349	PS/3-349

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3866	UC3867	UC3868	UC3875	UC3876
Application	Off-line, Zero Current Switching	DC-DC and Battery, Zero Current Switching	DC-DC and Battery, Zero Current Switching	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	2A	2A
Undervoltage Lockout	16.5V / 10.5V	8V / 7V	8V / 7V	10.75V / 9.5V	15.25V / 9.25V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Soft Start				Y	Y
Maximum Duty Cycle	100%	50% / 50%	100%	100%	100%
Separate Oscillator / Synchronization Terminal				Y	Y
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	DN-63, U-111, U-136A	DN-63, U-111, U-136A
Pin Count ❖	16	16	16	20, 28	20, 28
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-357	PS/3-357

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3877	UC3878	UC3879	UCC3895+	
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase, Shifted Bridge	
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	
Voltage Reference Tolerance	1%	1%	1%	1%	
Peak Output Current	2A	2A	0.1A	0.1A	
Undervoltage Lockout	10.75V / 9.5V	15.25V / 9.25V	Selectable 10.75V / 9.5V, 15.25V / 9.25V	11V / 9V	
Maximum Practical Operating Frequency	1MHz	1MHz	300kHz	1MHz	
Outputs	Quad, Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	
Startup Current	150µA	150µA	150µA	150µA	
Leading Edge Blanking					
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	100%	100%	100%	100%	
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	
Application / Design Note	DN-63, U-111, U-136A	DN-63, U-111, U-136A	DN-63, U-111, U-136A, U-154	DN-63, U-136A	
Pin Count ❖	20, 28	20, 28	20	20	
Page Number	PS/3-357	PS/3-357	PS/3-367	PS/3-425	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3524✣	UC3524A	UC3525A	UC3525B	UC3526
Application	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge
Voltage Reference Tolerance	4%	1%	1%	0.75%	1%
Peak Output Current	100mA	200mA	400mA	200mA	100mA
Undervoltage Lockout		7.5V / 7V	7V	7V	Y
Maximum Practical Operating Frequency	300kHz	500kHz	500kHz	500kHz	400kHz
Outputs	Dual Alternating, Uncommitted	Dual Alternating, Uncommitted	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current		4mA			
Voltage Feedforward					
Soft Start			Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	50% / 50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note			DN-36	DN-36	
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-43	PS/3-48	PS/3-54	PS/3-61	PS/3-68

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3526A	UC3527A	UC3527B	UC3548	UCC3570
Application	Fixed Frequency PWM Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Off-line, DC-DC	Wide Range, Off-line
Topology	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Flyback, Forward	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	1%	0.75%	1%	1%
Peak Output Current	100mA	400mA	200mA	2A	500mA
Undervoltage Lockout	Y	7V	7V	13V / 10V	13V / 9V
Maximum Practical Operating Frequency	550kHz	500kHz	500kHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current				500µA	85µA
Voltage Feedforward				Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	Programmable	100%
Separate Oscillator / Synchronization Terminal	Y	Y	Y		
Application / Design Note		DN-36	DN-36		DN-48, DN-62, DN-65, U-150
Pin Count ❖	18	16	16	16	14
Page Number	PS/3-75	PS/3-54	PS/3-61	PS/3-83	PS/3-91

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC35701+	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★
Application	Wide Range DC-DC and Off-line	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM
Topology	Forward, Flyback, Buck and Boost	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback
Voltage Reference Tolerance	1%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1.2A	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A
Undervoltage Lockout	13V / 9V	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V
Maximum Practical Operating Frequency	700kHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2
Startup Current	130µA	50µA	50µA	50µA	50µA
Voltage Feedforward	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-48, DN-62, DN-65, U-150	DN-65	DN-65	DN-65	DN-65
Pin Count ❖	14	16	16	16	16
Page Number	PS/3-99	PS/3-122	PS/3-122	PS/3-122	PS/3-122

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC3581	UCC3588+	UCC3888	UCC3889	UCC3890
Application	Off-line, Primary Side PWM for ISDN Applications	Synchronous Buck Regulator with 5 Bit DAC	Off-line Power Supply Controller	Off-line Power Supply Controller	Off-line Battery Charge Controller
Topology	Forward, Flyback	Voltage Mode Synchronous Buck	Flyback	Flyback	Flyback
Voltage Reference Tolerance	1.5%	1%	3%	3%	4%
Peak Output Current	1A	1A	0.15A	0.15A	0.15A
Undervoltage Lockout	7.3V / 6.8V	10.5V / 10V	8.4V / 6.3V	8.4V / 6.3V	8.6V / 6.3V
Maximum Practical Operating Frequency	100kHz	700kHz	250kHz	250kHz	250kHz
Outputs	Single, Totem Pole	Dual NFET Synchronous	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA		150µA	150µA	
Voltage Feedforward			Y	Y	Y
Soft Start	Y	Y			
Maximum Duty Cycle	Programmable	100%	55%	55%	N/A
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note	DN-48, DN65		DN-59A, U-149A	DN-59A, DN-65, U-149A	
Pin Count ❖	14	16	8	8	8
Page Number	PS/3-131	PS/3-163	PS/3-407	PS/3-412	PS/3-418

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC494A/AC	UC495A/AC			
Application	DC-DC	DC-DC			
Topology	Buck, Boost, Push-Pull, Half Bridge	Buck, Boost, Push-Pull, Half Bridge			
Voltage Reference Tolerance	1%	1%			
Peak Output Current	200mA	200mA			
Undervoltage Lockout	5V / 4.7V	5V / 4.7V			
Maximum Practical Operating Frequency					
Outputs	Dual Floating	Dual Floating			
Startup Current	6mA	6mA			
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle					
Separate Oscillator / Synchronization Terminal					
Special Features		On Chip 39V Zener			
Application / Design Note	DN-38	DN-38			
Pin Count ❖	16	18			
Page Number	PS/3-460	PS/3-460			

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction

Power Factor Correction

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC3817+	UCC3818+	UCC38500+	UCC38501+	UCC38502+
Soft Switching					
Maximum Practical Operating Frequency	250kHz	250kHz	250kHz	250kHz	250kHz
Current Error Amplifier Bandwidth	3MHz	3MHz	3MHz	3MHz	3MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1A	1A	1A	1A
Startup Current	0.1A	0.1A	0.1A	0.1A	0.1A
Undervoltage Lockout	16V / 10V	10.5V / 10V	16V / 10V	10.5V / 10V	16V / 10V
UVLO 2 Hysteresis			1.2V (300V Turn-off)	1.2V (300V Turn-off)	3V (200V Turn-off)
Overvoltage Protection	Y	Y	Y	Y	Y
Enable Input	Y (with OVP)	Y	Y	Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)
Special Features			DC / DC Controller Included	DC / DC Controller Included	DC / DC Controller Included
Application / Design Note	DN-39E	DN-39E	DN-39E		
Pin Count ❖	16	16	20	20	20
Page Number	PS/4-5	PS/4-5	PS/4-15	PS/4-15	PS/4-15

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UC3854B	UC3855A	UC3855B	UCC3857	UCC3858
Soft Switching		ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	200kHz	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1.5A	1.5A	1A	0.5A
Startup Current	0.3mA	0.15mA	0.15mA	0.06mA	0.1mA
Undervoltage Lockout	10.5V / 10V	16V / 10V	10.5V / 10V	13.8V / 10V	13.8V / 10V
Overvoltage Protection		Y	Y		Y
Enable Input	Y	Y	Y		Y
Multiplier / Divider Feedforward	Y	Y	Y	Y (Faster Response)	Y (Faster Response)
Special Features		Current Synthesizer	Current Synthesizer	Single Stage Isolated Output	Improved Efficiency at Light Load
Application / Design Note	DN-39E, DN-44, DN-66	DN-39E, DN-66, U-153	DN-39E, DN-66, U-153	DN-39E	DN-39E, DN-90
Pin Count ❖	16	20	20	20	16
Page Number	PS/4-42	PS/4-48	PS/4-48	PS/4-56	PS/4-65

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC38503+	UC3852	UC3853	UC3854	UC3854A
Soft Switching		ZCT			
Maximum Practical Operating Frequency	250kHz	Variable	125kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	3MHz	N/A	1MHz	800kHz	5MHz
Average Current Mode	Y		Y	Y	Y
Worldwide AC Input Voltage Operation	Y		Y	Y	Y
Output Drive	1A	0.5A	1A	1A	1A
Startup Current	0.1A	1mA	0.25mA	1.5mA	0.3mA
Undervoltage Lockout	10.5V / 10V	16.3V / 11.5V	11.5V / 9.5V	16V / 10V	16V / 10V
UVLO 2 Hysteresis	3V (200V Turn-off)				
Overvoltage Protection	Y		Y		
Enable Input	Y			Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	N/A	Y	Y	Y
Special Features	DC / DC Controller Included				
Application / Design Note		DN-39E, U-132	DN-39E, DN-77, DN-78, U-159	DN-39E, DN-41, U-134	DN-39E, DN-44, DN-66
Pin Count ❖	20	8	8	16	16
Page Number	PS/4-15	PS/4-22	PS/4-27	PS/4-32	PS/4-42

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation

Linear Controllers	UNITRODE PART NUMBER				
	UC3832	UC3833	UC3834	UC3835	UC3836
Type of Output	Positive Adjustable	Positive Adjustable	Positive / Negative Adjustable	5V Fixed	Positive Adjustable
Maximum Input Voltage	36V	36V	40V	40V	40V
Minimum Output Voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V
Output Drive	300mA	300mA	350mA	500mA	500mA
Type of Short Circuit Limit	Duty Cycle	Duty Cycle	Foldback	Foldback	Foldback
Reference Voltage Accuracy	2%	2%	3% / 4%	2%	2%
Special Features	Multiple Pins Accessible	8 Pin Package		Built in Rsense	Built in Rsense
Application / Design Note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95		
Pin Count ❖	14, 16	8, 16	16	8, 16	8, 16
Page Number	PS/5-11	PS/5-11	PS/5-18	PS/5-24	PS/5-24

Linear Controllers	UNITRODE PART NUMBER				
	UCC3837				
Type of Output	Positive Adjustable				
Maximum Input Voltage	12V				
Minimum Output Voltage	1.5V				
Output Drive	1.5mA				
Type of Short Circuit Limit	Duty Cycle				
Reference Voltage Accuracy	2%				
Special Features	• Internal Charge Pump • Direct N-FET Drive				
Application / Design Note					
Pin Count ❖	8				
Page Number	PS/5-28				

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output Voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V / Adjustable
Dropout Voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output Voltage Accuracy	2.5%	1%	1%	1%	1%
Maximum Input Voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown Current	10µA				
Operating Current	400µA				
Line Regulation	0.01% / V				
Load Regulation	0.1%, I_{OUT} = 0 to 1A				
Special Features	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count❖	8	5	5	5	5
Page Number	PP/7-5	PS/5-5	PS/5-5	PS/5-5	PS/5-5

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC383	UC384	UC385-1	UC385-2	UC385-3
Output Voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout Voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output Voltage Accuracy	2.5%	2.5%	1%	1%	1%
Maximum Input Voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown Current	40µA	17µA			
Operating Current	400µA	240µA			
Line Regulation	0.01% / V	0.01% / V			
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA			
Special Features	Power Limit	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count❖	3	8	5	5	5
Page Number	PP/7-12	PP/7-19	PS/5-35	PS/5-35	PS/5-35

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC385-ADJ	UC386+	UC387+	UC388+	
Output Voltage	1.2V / Adjustable	3.3V	5V	Adjustable down to 1.25V	
Dropout Voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA	
Output Voltage Accuracy	1%	1.5%	1.5%	1.5%	
Maximum Input Voltage	7.5V	9V	9V	9V	
Shutdown Current		2µA	2µA	2µA	
Operating Current		10µA	10µA	10µA	
Line Regulation		25mV max	25mV max	25mV max	
Load Regulation		10mV max	10mV max	10mV max	
Special Features	Fast Transient Response	TSSOP	TSSOP	TSSOP	
Pin Count ❖	5	8	8	8	
Page Number	PS/5-35	PP/7-29	PP/7-29	PP/7-29	

Special Functions Linear Regulators	UNITRODE PART NUMBER				
	UC560	UCC561+	UC563+		
Type of Output	Positive	Positive	Positive		
Application	Source / Sink Regulator for the 18 and 27 Line SCSI Termination	LVD SCSI Regulator for the 18 and 27 Line Termination	32 Line VME Bus Bias Generator		
Input Voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V		
Output Voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V		
Dropout Voltage	0.9V at 750mA				
Bus Standard	SCSI-1,2,3	SPI-2, 3	VME / VME64		
Sink / Source Current	300mA / –750mA	200mA / –200mA	475mA / –575mA		
Application / Design Note					
Pin Count ❖	5, 8	16	3, 8		
Page Number	IF/4-3	IF/4-7	IF/4-10		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers

Power and FET Drivers	UNITRODE PART NUMBER				
	L293/D	UC2950	UC3702	UC3705	UC3706
Power Driver	Quad	Single		Single	Dual
FET Driver					
Isolated Driver Pairs					
Relay Drivers			Quad		
Output Configuration	Non-Inverting	Sink / Source TTL	Non-Inverting	Complementary	Complementary
Enable					
Inhibit	Y		Y		Y
Analog Stop					Y
Output Rise Time	250ns			60ns	60ns
Maximum Voltage	36V	35V	42.5V	40V	40V
Peak Output Current	2.0A / 1.2A	4.0A	50mA per Relay	1.5A	1.5A
Application / Design Note				U-111, U-118, U-137	U-111, U-118, U-137
Pin Count ❖	16, 28	5	16	5, 8	16
Page Number	PS/6-5	PS/6-10	PS/6-12	PS/6-16	PS/6-19

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3707	UC3708	UC3709	UC3710	UC3711
Power Driver	Dual	Dual			
FET Driver			Single	Single	Dual
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Complementary	Non-Inverting	Non-Inverting	Complementary	Non-Inverting
Enable		Y			
Inhibit	Y				
Analog Stop	Y				
Output Rise Time	50ns	75ns	40ns	40ns	20ns
Maximum Voltage	40V	35V	40V	20V	40V
Peak Output Current	1.5A	3.0A	1.5A	6.0A	1.5A
Application / Design Note	U-111, U-118, U-137	DN-35, U-111, U-137	U-111, DN-118, U-137	U-111	U-111
Pin Count ❖	16	8, 16	8, 16	5, 8, 16	8
Page Number	PS/6-24	PS/6-31	PS/6-35	PS/6-38	PS/6-41

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3714	UC3715	UC3724	UC3725	UC3726
Power Driver					Transmitter
FET Driver	Dual	Dual	Transmitter	Single	
Isolated Driver Pairs			FET Drv	FET Drv	IGBT Drv
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting	Non-Inverting	Non-Inverting
Enable	Y	Y			
Inhibit					
Analog Stop					
Output Rise Time	100ns / 50ns	100ns / 50ns	30ns	30ns	75ns
Maximum Voltage	20V	20V	40V	40V	40V
Peak Output Current	1.0A / 2.0A	1.0A / 2.0A	2.0A	2.0A	4.0A
Application / Design Note	U-111	U-111	DN-35, U-127	DN-35, U-127	DN-57, DN-60, U-143C
Pin Count ❖	8, 16	8, 16	8, 16	8, 16	16, 28
Page Number	PS/6-43	PS/6-43	PS/6-50	PS/6-53	PS/6-57

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3727	UCC37423+	UCC37424+	UCC37425+	UCC37523+
Power Driver	Single				
FET Driver		Dual	Dual	Dual	Dual
Isolated Driver Pairs	IGBT Drv				
Relay Drivers					
Output Configuration	Non-Inverting	Inverting	Non-Inverting	One Inverting, One Non-Inverting	Inverting
Enable					Y
Inhibit					
Analog Stop					
Output Rise Time	75ns	20ns	20ns	20ns	20ns
Maximum Voltage	40V	20V	20V	20V	20V
Peak Output Current	4.0A	3.0A	3.0A	3.0A	3.0A
Special Features		UVLO	UVLO	UVLO	UVLO, Adaptive LEB
Application / Design Note	DN-57, DN-60, U-143C				
Pin Count ❖	20, 28	8, 16	8, 16	8, 16	8, 16
Page Number	PS/6-62	PS/6-68	PS/6-68	PS/6-68	PS/6-73

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UCC37524+	UCC37525+	UCC3776		
Power Driver					
FET Driver	Dual	Dual	Quad		
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting		
Enable	Y	Y	Y		
Inhibit					
Analog Stop					
Output Rise Time (ns)					
Maximum Voltage	20V	20V	18V		
Peak Output Current	3.0A	3.0A	1.5A / 2.0A		
Special Features	UVLO, Adaptive LEB	UVLO, Adaptive LEB	UVLO		
Application / Design Note					
Pin Count ❖	8, 16	8, 16	16		
Page Number	PS/6-73	PS/6-73	PS/6-79		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support

Power Supply Support

Feedback Signal Generators	UNITRODE PART NUMBER			
	UC3901	UC39431	UC39432	UC3965
Description	Isolated Feedback Generator	Precision Adjustable Shunt Regulator	Precision Analog Controller	Precision Reference with Low Offset Error Amplifier
Application	Amplitude Modulation System Used to Couple a Control Signal Across a Voltage Isolation Barrier	Adjustable 100mA Shunt Regulator, Voltage Reference Optocoupler Driver, Voltage to Current Converter	Adjustable 100mA Shunt Regulator, Optocoupler Driver, Programmable Transconductance Voltage to Current Converter	Used for High Precision PWM Switching Regulators
Key Features	•Transformer Couples Isolated Feedback Error Signal •Low Cost Alternative to Optical Couplers •5MHz Carrier Provides Fast Response Capability •Modulator Synchronizable to an External Clock	•Multiple On-chip Programmable Reference Voltages •2.2V to 36V Operating Supply Voltage and User Programmable Reference •Linear Transconductance for Optocoupler Feedback Applications	•Programmable, Linear Transconductance for Optimum Optocoupler Current Drive •Precision Reference and Error Amplifier Inputs Externally Available •2.2V to 36V Operating Supply Voltage and User Programmable Reference	•2.5V Precision Reference with 0.4% Accuracy •Low 1mV Offset Error Amplifier •2X Inverting Amplifier / Buffer Output •Drivers Optocoupler Diode for Isolated Applications
Application / Design Note	DN-19, DN-33, U-94		DN-52	U-165
Pin Count❖	14, 16	8	8	8
Page Number	PS/7-21	PS/7-50	PS/7-56	PS/7-60

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Load Share Controllers	UNITRODE PART NUMBER		
	UC3902	UC3907	
Description	8-Pin Load Share Controller	Load Share Controller	
Application	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	
Key Features	•Highly Tolerant of Voltage Differences Between Power Supply Return •2.7V to 20V Operation •High Gain, Low Offset Current Sense Amplifier Permits Low Shunt Resistor Values •Single Capacitor Sets Load Share Filter Response	•Fully Differential High Impedance Voltage Sensing •Accurate Current Amplifier for Precise Load Sharing •Optocoupler Driving Capability •4.5V to 35V Operation	
Application / Design Note	U-129, U-163	U-129, U-163	
Pin Count❖	8	16	
Page Number	PS/7-27	PS/7-44	

Schottky Diode Array / Bridges	UNITRODE PART NUMBER		
	UC3610	UC3611	UC3612
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	•Monolithic Eight-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time	•Matched, Four-diode Monolithic Array •High Peak Current •Low Forward Voltage •Parallelable for Higher Current or Lower Voltage Drop	•Monolithic Two-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time
Application / Design Note			DN-48
Pin Count❖	8, 16	8, 16	8
Page Number	PS/7-10	PS/7-12	PS/7-15

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Supervisory and Monitor Circuits	UNITRODE PART NUMBER				
	UC3543	UC3544	UC3730	UC3903	UC3904
Power Supply Monitor	Single	Single		Quad	Quad
Temperature Monitor			Y		
Description	Power Supply Supervisory with OV, UV and Current Sensing	Power Supply Supervisory with OV, UV and Current Sensing	Combines a Temperature Transducer, Precision Reference, and Temperature Comparator for Maximum System Flexibility	Quad Supply and Line Monitor	Quad Supply and Line Monitor
Voltage Clamp					
Voltage Range	5V to 35V	5V to 35V		8V to 40V	4.75V to 18V
Window Adjust	N	N		Y	Y
Current Range					
Current Limit	Y	Y		N	N
Programmable Threshold	Y	Y		Y	Y
Programmable Time Delay	Y	Y		Y	Y
Special Features		Uncommitted OV Inputs			
Application / Design Note				DN-33	
Pin Count ❖	16	18	5, 8, 20	18	18
Page Number	PS/7-5	PS/7-5	PS/7-17	PS/7-32	PS/7-39

Supervisory and Monitor Circuits	UNITRODE PART NUMBER		
	UCC3946		
Description	Microprocessor Supervisor with Watchdog Timer		
Application	Accurate Microprocessor Supervision		
Key Features	• Programmable Reset Period • Programmable Watchdog Period • 1.5% Accurate Threshold • 4mA IDD		
Pin Count ❖	8		
Page Number	PP/7-88		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control

Brushless Motor Products	UNITRODE PART NUMBER				
	UC3625	UCC3626+			
Hall Logic	Y	Y			
Tachometer	Y	Y			
Output Current per Output	0.1A	0.01A			
Operating Voltage	10V - 18V	11V - 15V			
Differential Current Sense Amplifier	Y	Y			
Current Limit	Y				
Application / Design Note	DN-50, U-115, U-120, U-130	U-120			
Pin Count ❖	28	28			
Page Number	PS/8-37	PS/8-50			

DC Motor Controllers	UNITRODE PART NUMBER				
	UC3637	UC3638			
Output Clamp Diodes					
Output Current per Output	0.1A	0.1A / 0.05A			
Operating Voltage	5V - 36V	10V - 36V			
Differential Current Sense Amplifier		Y			
Thermal Shutdown					
Current Limit	Y	Y			
Application / Design Note	DN-53A, U-102, U-112, U-120	DN-76, U-120			
Pin Count ❖	18, 20	20			
Page Number	PS/8-78	PS/8-84			

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Linear Power Amplifier Products	UNITRODE PART NUMBER				
	UC3173A	UC3175B	UC3176	UC3177	UC3178
Output Clamp Diodes	Y	Y	Y	Y	Y
Output Current per Output	0.55A	0.8A	2A	2A	0.45A
Operating Voltage	4V - 15V	4V - 15V	3V - 35V	3V - 35V	3V - 15V
Differential Current Sense Amplifier	Y	Y	Y	Y	Y
Thermal Shutdown	Y	Y	Y	Y	Y
Current Limit	Y	Y	Y	Y	Y
Four Quadrant	Y	Y	Y	Y	Y
Number of Outputs	2	2	2	2	2
BW	2MHz	2MHz	1MHz	1MHz	2MHz
Special Features			B+ Input Pin	Supply OK Pin	
Pin Count ❖	24	24	28	28	28
Page Number	PS/8-5	PS/8-16	PS/8-21	PS/8-21	PS/8-25

Phase Locked Frequency Controllers	UNITRODE PART NUMBER				
	UC3633	UC3634	UC3635		
Internal Oscillator	Y	Y	Y		
Divider Output Provided			Y		
External Phase Detector Inputs			Y		
2 Phase Drive Logic		Y	Y		
Divide Logic Select	4/5 & 2/4/8	2/4/8	2/4		
Operating Voltage	8V - 15V	8V - 15V	8V - 15V		
Maximum Frequency	10MHz	10MHz	10MHz		
Application / Design Note	U-113	U-113	U-113		
Pin Count ❖	16, 20	16, 20	16		
Page Number	PS/8-63	PS/8-70	PS/8-74		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Stepper Motor Controllers	UNITRODE PART NUMBER				
	UC3517	UC3717	UC3717A	UC3770A	UC3770B
Output Clamp Diodes		Y	Y	Lower	Lower
Output Current per Output	0.35A	0.8A	1A	1.3A	1.3A
Operating Voltage	10V - 40V	10V - 45V	10V - 46V	10V - 50V	10V - 50V
Differential Current Sense Amplifier					
Thermal Shutdown		Y	Y	Y	Y
Current Limit		Y	Y	Y	Y
Current Sense Thresholds					Tailored for half stepping applications
Application / Design Note		U-99	U-99		
Pin Count ❖	16	16, 20	16, 20	16, 28	16, 28
Page Number	PS/8-30	PS/8-92	PS/8-100	PS/8-108	PS/8-108

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions

Special Functions

Current Sensors	UNITRODE PART NUMBER					
	UCC3926					
Application	Current Sensing					
Maximum Current	±20A					
Application / Design Note	DN-91					
Pin Count ❖	16					
Page Number	PS/9-43					

Lighting Controllers	UNITRODE PART NUMBER					
	UCC3305✣					
Application	Constant Power HID Lamp Controller					
Topology	Boost, Flyback					
Outputs	3 - Single and Dual Alternating, Totem Pole					
Reference Tolerance	2%					
Open Lamp Detect	Y					
Soft Start	Y					
External Synchronization	Y					
Shutdown Current	N/A					
Maximum Frequency	500kHz					
Lamp Intensity Control	Y					
Application / Design Note	DN-72, U-161					
Pin Count ❖	28					
Page Number	PS/9-5					

❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

Special Functions (cont.)

Ring Generator Controllers	UNITRODE PART NUMBER		
	UCC3750	UCC3751+	UCC3752+
Description	Source Ringer Controller	Single Line Ring Generator Controller	Mulit-Line Ring Generator Controller
Application	4 Quadrant Flyback Controller Develops High Voltage AC Output	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset
Key Features	• On Chip Low THD Sinewave Reference, Pin Selectable 20Hz, 25Hz, and 50Hz • Programmable Output Amplitude and DC Offset • AC and DC Current Limiting With Short Circuit Protection	• Off-hook Detection With Automatic Transition to DC Operation • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection	• Off-hook Detection and Indication • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection
Application / Design Note	DN-79, U-169		
Pin Count ❖	28	16	16
Page Number	PS/9-22	PS/9-32	PS/9-38

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions (cont.)

Sensor Drivers	UNITRODE PART NUMBER				
	UC37131+	UC37132+	UC37133+		
Part Name	Smart Power Switch	Smart Power Switch	Smart Power Switch		
Description	65V Universal Low Side Driver with Current Limiting	65V Universal High or Low Side Driver with Current Limiting	65V Universal High Side Driver with Current Limiting		
Pin Count ❖	8	14, 16	8		
Page Number	PS/9-13	PS/9-13	PS/9-13		

Serial DACs	UNITRODE PART NUMBER		
	UCC5950		
Part Name	Digital to Analog Converter		
Description	10-Bit BiCMOS Digital to Analog Converter for Servo and Instrumentation Systems		
Pin Count ❖	8		
Page Number	PS/9-48		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Military/Aerospace Products

General Information

Die and Wafers

Unitrode offers most of its products in die and/or wafer form through die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques. Die thickness is either 12 mils or 15 mils, ±1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing. All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications with the exception of some high power or high speed devices where production probe equipment limit the test environment.

Inspection. Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering. Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.

Military/Aerospace Products

Unitrode offers its innovative, quality products in military/aerospace and high reliability versions. Our certification to MIL-PRF-38535 demonstrates our commitment to our customer's requirements in this important market segment. Our product offering includes:

- ***STANDARD MILITARY DRAWINGS (SMD)*** ~ *Conformance to Class Q performance requirements of MIL-PRF-38535, and individual SMD electrical parameters. Unitrode offers over 100 SMD products.*
- ***CLASS V*** ~ Conformance to all Class V requirements of MIL-PRF-38535, or to individual customer source control documents.
- ***SCDClass B*** ~ Unitrode also accepts unique customer source control drawings for Class B, MIL-STD-883 type products.
- ***Bare Die / Lot Acceptance Testing*** ~ Tested to individual source control documents.

Unitrode has had DESC facility certification continuously since November 1985.

Space Level Products

Unitrode is a leader in producing linear ICs to customers' Class S specifications and has many years of proven experience in this field. Our abilities in this area include all processing requirements of Class S (including MIL-PRF-38535, MIL-STD-883, and SCC9000), as well as an extensive library of radiation data on our most popular devices (see below). Our superior design support, years of experience, and flexibility to service our customers' unique requirements make us the best choice for Class S linear products.

Radiation Data Availability

Unitrode has provided products screened to the S-level requirements of MIL-STD-883, MIL-PRF-38535, and the European specification SCC9000. Due to our participation in this market, we have collected a variety of radiation reports including SEU, total dose (including low dose rate), and neutron fluence, which are available upon customer request (see listing below). These reports are results of independent testing by our customers and do not represent guaranteed levels of radiation tolerance by Unitrode. The availability of this data is subject to change. Contact your local Unitrode sales representative.

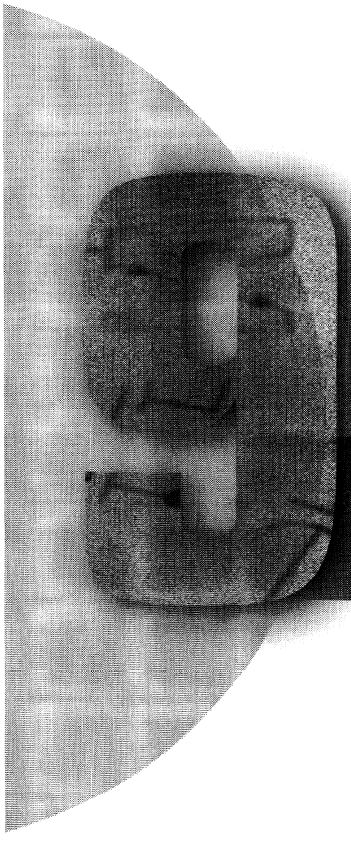
Raditation data is available for the following Unitrode products: UC1625, UC1635, UC1710, UC1711, UCC1800, UCC1806, UC1823, UC1825/A, UC1832, UC1834, UC1838A, UC1843A, UC1845, UC1846, UC1856, UC1863, UC1875, UC1901, UC1907, UCC1912.

Standard Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD Number	*Unitrode Part Number*
5962-8670401PA	UC1842J/883B
5962-8670401XA	UC1842L/883B
5962-8670402PA	UC1843J/883B
5962-8670402XA	UC1843L/883B
5962-8670403PA	UC1844J/883B
5962-8670403XA	UC1844L/883B
5962-8670404PA	UC1845J/883B
5962-8670404XA	UC1845L/883B
5962-8670405PA	UC1842AJ/883B
5962-8670405XA	UC1842AL/883B
5962-8670406PA	UC1843AJ/883B
5962-8670406XA	UC1843AL/883B
5962-8670407PA	UC1844AJ/883B
5962-8670407XA	UC1844AL/883B
5962-8670408PA	UC1845AJ/883B
5962-8670408XA	UC1845AL/883B
5962-86806012A	UC1846L/883B
5962-8680601EA	UC1846J/883B
5962-86806022A	UC1847L/883B
5962-8680602EA	UC1847J/883B
5962-87619012A	UC1707L/DESC
5962-8761901EA	UC1707J/DESC
5962-8764502EA	UC1524AJ/DESC
5962-87681012A	UC1825L/883B
5962-8768101EA	UC1825J/883B
5962-87681022A	UC1825AL/883B
5962-8768102EA	UC1825AJ/883B
5962-8768102XA	UC1825ALP/883B
5962-87681032A	UC1825BL/883B
5962-8768103EA	UC1825BJ/883B
5962-8768103XA	UC1825BLP/883B
5962-8774001EA	UC1543J/883B
5962-8774002EA	UC1544J/883B
5962-87742012A	UC1834L/883B
5962-8774201EA	UC1834J/883B
5962-88697012A	UC1903L/883B
5962-8869701VA	UC1903J/883B
5962-89441012A	UC1901L/883B
5962-8944101CA	UC1901J/883B
5962-89511012A	UC1525AL/DESC
5962-8951101EA	UC1525AJ/DESC
5962-89511032A	UC1525AL/883B
5962-8951103EA	UC1525AJ/883B
5962-8951104EA	UC1527AJ/883B
5962-89611012A	UC1706L/DESC
5962-8961101EA	UC1706J/DESC
5962-89899012A	UC1838AL/883B
5962-8989901EA	UC1838AJ/883B
5962-89905012A	UC1823L/883B
5962-8990501EA	UC1823J/883B
5962-89905022A	UC1823AL/883B
5962-8990502EA	UC1823AJ/883B
5962-89905032A	UC1823BL/883B
5962-8990503EA	UC1823BJ/88B
5962-89920012A	UC1840L/883B
5962-8992001VA	UC1840J/883B
5962-89920022A	UC1841L/883B
5962-8992002VA	UC1841J/883B
5962-89957012A	UC1637L/883B
5962-8995701VA	UC1637J/883B

SMD Number	Unitrode Part Number
5962-90538012A	UC1611L/883B
5962-9053801PA	UC1611J/883B
5962-90650012A	UC1835L/883B
5962-9065001PA	UC1835J/883B
5962-9098701M2A	UC1633L/883B
5962-9098701MEA	UC1633J/883B
5962-9168901MXA	UC1625J/883B
5962-9203101M2A	UC1864L/883B
5962-9203101MEA	UC1864J/883B
5962-9203102MEA	UC1865J/883B
5962-9235001MXC	L293DSP/883B
5962-9320601M2A	UC1907L/883B
5962-9320601MEA	UC1907J/883B
5962-9321501M2A	UC1517L/883B
5962-9321501MEA	UC1517J/883B
5962-9326101M2A	UC1854L/883B
5962-9326101MEA	UC1854J/883B
5962-9326102M2A	UC1854BL/883B
5962-9326102MEA	UC1854BJ/883B
5962-9326103M2A	UC1854AL/883B
5962-9326103MEA	UC1854AJ/883B
5962-9326501M2A	UC1832L/883B
5962-9326501MCA	UC1832J/883B
5962-9326502M2A	UC1833L/883B
5962-9326502MPA	UC1833J/883B
5962-9451301MPA	UCC1801J/883B
5962-9451302MPA	UCC1802J/883B
5962-9451303MPA	UCC1803J/883B
5962-9451304MPA	UCC1804J/883B
5962-9451305MPA	UCC1805J/883B

SMD Number	Unitrode Part Number
5962-9453001M2A	UC1856L/883B
5962-9453001MEA	UC1856J/883B
5962-9455501M3A	UC1875L/883B
5962-9455501MRA	UC1875J/883B
5962-9455501MXA	UC1875LP/883B
5962-9457501MEA	UCC1806J/883B
5962-9462201M2A	UC1871L/883B
5962-9462201MVA	UC1871J/883B
5962-9474601M2A	UC1717L/883B
5962-9474601MEA	UC1717J/883B
5962-9554401MJC	UC1620SP/883B
5962-9558601MVA	UC1851J/883B
5962-9579801M2A	UC1705L/883B
5962-9579801MPA	UC1705J/883B
77034012A	UC117L/883B
77034052A	UC117AL/DESC
7802801EA	UC1524J/DESC
85515012A	UC1526L/883B
8551501VA	UC1526J/883B
85515022A	UC1526AL/883B
8551502VA	UC1526AJ/883B



Packaging Information

Packaging Information

The following are Unitrode's recommended profiles and limits for plastic package surface-mounting and de-soldering methods. To achieve and maintain the recommended conditions near the plastic package, time/temperature profiles of the surface-mount processing equipment may differ from those below, depending on board density, oven mass, exhaust rate, and other factors.

Unitrode uses a solder reflow pre-conditioning process with a 220° C peak temperature to determine moisture sensitivity ratings for plastic packaged components. The profiles shown are used with Unitrode's moisture-sensitivity ratings of the plastic packaged surface-mount components. Published moisture sensitivity ratings may not apply when a process with a more extreme peak temperature (such as wave solder) is used. If the temperatures or rates of temperature increase exceed those noted for IR reflow, then we recommend that the packaged component be either baked before surface-mount assembly or handled in consistence with the next lower moisture-sensitivity rating. (For example, handle a Level-2 rated part as Level 3.) For baking conditions and/or definitions of moisture-sensitivity level ratings, consult JEDEC J-STD-020A and J-STD-033.

For more than one soldering pass (e.g., on boards with components on top and bottom), time between the two soldering processes must be between 5 minutes and 48 hours. Between passes, if the environmental conditions of the plastic packaged component exceed 30° C/60% RH, then the component must be baked before the second pass.

Wave Solder *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120 seconds
- Maximum rate of increase to maximum solder temperature 3° C/s
- Solder temperature of first (turbulent) wave < 250° C (4 seconds maximum)
- Solder temperature of second (broad) wave < 240° C (10 seconds maximum, 2° C/s maximum rate of cooling from first wave)
- Maximum cooling to room temperature 4° C/s maximum
- Total time over 183° C < 90s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Maximum time from 25° C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

NOTE: We **STRONGLY RECOMMEND** that the component's plastic body not contact the solder wave or bath during assembly. Contact can be prevented by shielding. If contact occurs, then do the following:

- Pre-bake parts within 4 hours before board-mount assembly (24 hours at 125° C or 192 hours at 40° C).
- Limit all rates of temperature change to 2.5° C/s.
- Limit total time over 183° C to less than 45s.

Recommended Profile Limits (cont.)

IR Reflow or Convection Reflow *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 3° C/s
- Maximum reflow temperature < 240° C (20s maximum with 5° C of peak temperature)
- Maximum rate of decrease to room temperature 6° C/s
- Maximum time over 210° C < 40s
- Maximum total time over 183° C < 150s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Maximum time from 25° C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

Vapor Phase Reflow *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 10° C/s
- Maximum reflow temperature < 219°C (60s maximum with 5° C of peak temperature)
- Maximum rate of decrease to room temperature 10° C/s
- Maximum time over 183°C < 80s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Minimum 5-minute cool-down time between cycles

Rework *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

To preserve the integrity of the plastic packaged component (for further analysis), we suggest the following steps to minimize damage from component removal.

- Always keep the package body temperature below 200° C.
- Bake out moisture in packages rated JEDEC Level 2-6 or in packages exposed to uncontrolled ambient conditions since being assembled.
- For hand de-soldering (i.e., soldering iron), do not allow maximum temperature at the leads to exceed 300° C for more than 5s.

For forced-hot-air de-soldering, the following limits apply:

- Limit the rate of temperature increase to 25° C/s between ambient and 100° C.
- Limit the rate of temperature increase to 4° C/s maximum from 100° C to de-soldering temperature.
- Limit maximum de-soldering temperature at leads to less than 240° C (10s maximum).
- Carefully minimize the cooling rate after removing the part from the printed circuit board.

Introduction

All operating circuit components dissipate power, causing their temperature to rise. Unitrode integrated circuits are designed to operate in a considerable range of temperatures, but there are limits. This note suggests ways to ensure that specified temperature limits for each part are not exceeded.

Junction Temperature (Tj)

For reliability and long-term operating life of the device, the system designer must manage the power dissipated by the device in the system so junction temperature (Tj) not only does not exceed specified limits, but also is kept as low as possible. This temperature control is necessary, because higher junction temperatures adversely affect the operating life of the device.

Power Dissipation (Pd) and Thermal Resistance (q)

With power off, all components of a given circuit approach (and in time reach) ambient temperature. With the power on, the components are warmed by their internal power dissipation until a new equilibrium is reached. Some electrical power is dissipated as heat by an integrated circuit (Pd) during operation, thus raising the junction temperature. The effectiveness of the IC package and the system in dissipating this heat is "thermal resistance" (θ), a term analogous to electrical resistance in the sense that the materials of the IC, package, and system restrict the flow of heat from the higher junction temperature (Tj) to the lower ambient temperature of the system (Ta). Understanding the thermal resistance characteristics of the package and system facilitates management of the device junction temperature within desired limits.

The rate of heat flow depends on the temperature difference (DT) between the two endpoints (Tj and Ta), and also on the thermal resistance, θ, of the package and system. Heat is a form of energy, and if we choose the joule as the measuring unit we can specify the rate of heat flow in units of joules per second. Therefore, $Pd\,[joules\,per\,second] = \frac{\Delta T}{\theta}$ and since one *joule per second* is the same as a watt (W), we have $\theta = \frac{\Delta T}{Pd}(°C/W)$

Thermal resistance is typically expressed in terms of resistance from junction-to-ambient (θja), which incorporates not only the internal resistance of the IC package, but also the resistance of the system as well. θja can be broken down into the sum of these two different thermal resistances, from junction-to-case, θjc (or in the case of power surface-mount packages, junction-to-lead, θjl) and case-to-ambient, θca. Therefore, $\theta ja = \frac{Tj - Ta}{Pd} = \theta jc + \theta ca$

Variables Which Affect θja

The thermal resistance of the package is a function of many variables, such as the leadframe material and design configuration, the plastic encapsulant material, the silicon die area, the die attach material, and others. However, as previously indicated, the effectiveness of the system in removing heat from the package also has a significant impact on θja. These variables include the material and configuration of the circuit board on which the package is mounted, the type of cooling used (i.e., conduction or convection), the size of the traces on the circuit board, the use of heatsinks, etc. It is essential that the system designer understand these variables and how they affect θja.

Unitrode Test Procedures

Table 1 shows thermal resistance values for Unitrode IC packages. Thermal resistance junction-to-case (θjc) is measured by mounting the device to an essentially infinite heat sink. Power leadframe surface-mount packages and the batwing DIP conduct most of the dissipated power through their leads rather than through the case. For these noted packages, the specified thermal resistance is junction-to-lead (θjl).

Junction-to-ambient (θja) thermal resistance is measured on a 5.0-square-inch printed circuit board in 1 cubic foot of still air. For through-hole packages, single-side FR-4 boards with 1-ounce copper traces are used. (See Figure 1.) However, since surface-mount devices, including those without power leadframes, conduct a significant amount of heat through their leads to the pc-board, various types of surface-mount boards are measured. (See Figure 2.) To indicate the effect of the pc-board on θja, a range of values is given. The lower value is for a device mounted on a 5.0-square-inch, 0.062 inch thick aluminum pc-board. The highest value is for a device mounted on a 5.0-square-inch single-sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. Some interpolation may be needed based on an individual application to arrive at an accurate estimate of the actual θja.

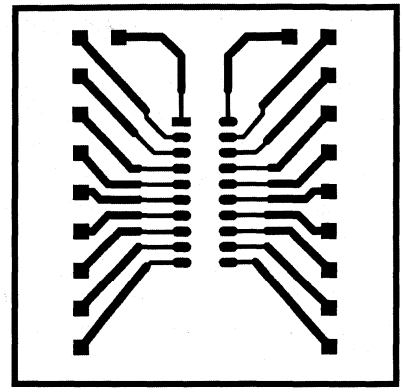


Figure 1. Typical through-hole pc-board design.

To determine the device θja, a measurement of the device junction temperature is made under the above conditions using a technique called the "temperature-sensitive parameter" method. This technique involves measuring the voltage drop of calibrated component, typically a diode, which then allows calculation of the device junction temperature. Since Pd, Tj, and Ta are known, θja can be determined. For the case of power leadframe surface-mount packages, θjl is determined by measuring the temperature of the pc-board at the device leads and then using this temperature in place of the ambient temperature in the calculation. For a more detailed discussion on surface-mount packages, refer to "Thermal Characteristics of Surface-Mount Packages," found later in this section.

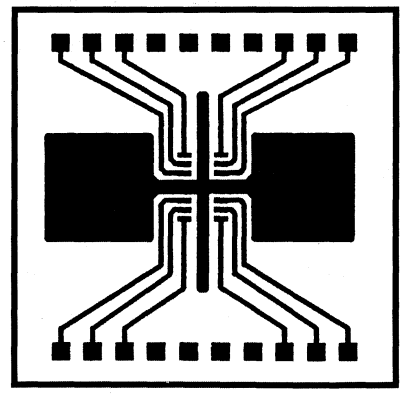


Figure 2. Typical surface mount pc-board design for power leadframe SOIC packages.

Example

Estimate the junction temperature of a UC5601DWP 18-Line SCSI Active Terminator on a 4-layer 0.062 inch thick multilayer pc-board at 1.0 watt power dissipation in a still-air environment at 30°C.

1. Determine θja. Table 1 shows that the the DWP package is a power leadframe surface-mount device, so the use of thermal resistance junction-to-lead (qjl) is appropriate. For the DWP package, qjl = 16°C/W. From Figure 8 in "Thermal Characteristics of Surface-Mount Packages," thermal resistance board-to-ambient (θba) = 19°C/W. We know that for a power leadframe surface-mount package, θja = θjl + θba, so, θja = 16°C/W + 19°C/W = 35°C/W.

2. Calculate the junction temperature, Tj.

$$Tj = (Pd \times \theta ja) + Ta$$
$$Tj = (1.0\ W \times 35°C/W) + 30°C$$
$$Tj = 65°C$$

This is well below the maximum rated junction temperature of 150°C listed in the Absolute Maximum Ratings section of the UC5601 product data sheet, so the thermal dissipation is satisfactory.

System Design Considerations

Through-hole devices such as dual in-line packages (DIPs) can be cooled by forcing airflow over the device in order to improve the convection cooling performance, or by conduction cooling of the package case to a heat sink such as the system chassis or cold-wall. Plastic DIPs are not particularly well suited to either of these techniques since the plastic encapsulant is a relatively poor thermal conductor. However, Unitrode offers several through-hole packages which have been optimized for conduction cooling techniques, namely the batwing DIP, the SP power ceramic DIP and the power leadframe Zig-Zag (ZIP) package. All of these packages provide low thermal resistance paths from the junction to the pc-board. Refer to Table 1 for the applicable ratings.

Surface-mount packages are well suited to conduction cooling since, as previously indicated, the package leads conduct a significant amount of heat to the pc-board. The pc-board itself can be utilized effectively as a heat sink when designed properly. For example, as seen in the discussion "Thermal Characteristics of Surface Mount Packages," when a power leadframe package is mounted on a multi-layer pc-board such that the heat-sink leads are thermally coupled to a ground plane in the board, or an area of copper fan-out on the board, then the overall thermal resistance is considerably lower than on a single-sided board with no heat-sinking. Additionally, Unitrode offers a power ceramic leadless chip carrier with a metallized thermal grid on the package case, which can be soldered directly to the board, thus greatly reducing its overall thermal resistance.

In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away from the device more effectively. Also, one should avoid grouping higher power devices tightly together on the board. A better approach would be to spread out the higher power devices to the cooler areas of the board. The choice of pc-board material will greatly affect the overall thermal performance of the system as well, although there are many factors involved when selecting the board material, such as cost, mechanical properties and environmental requirements.

Summary

Thermal management has been shown to be an essential factor in the reliable use of Unitrode integrated circuits. Thermal characteristics of Unitrode packages have been provided to the system designer in order to ensure that the system design effectively dissipates the power generated by the integrated circuit during operation.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
Ceramic DIP	8	J	390x288x140	150x200	N/A
	14		760x248x140	110x140	N/A
	16		760x288x140	160x250	N/A
	18		890x288x140	160x250	N/A
	20		950x288x140	160x250	N/A
	24		1250x520x170	250x250	N/A
	28		1450x520x165	250x250	N/A
Ceramic LCC	20	L	350x350x80	194x194	N/A
	28		450x450x80	250x250	N/A
Ceramic LCC Power	28	LP	450x450x80	250x250	N/A
LQFP	48	FQ	7x7x1.4 mm	200x200x5	100x100x12
	64		10x10x1.4 mm	260x260x5	100x100x12
	100		14x14x1.4 mm	276x276x5	100x100x12
LQFP Power	48	FQP	7x7x1.4 mm	185x185x5	100x100x12
	48		7x7x1.4 mm	190x190x5	100x100x12
MSOP	8	P	3x3x0.86 mm	68x94x6	50x50x8
	10		3x3x0.86 mm	68x98x6	50x50x8
PDIP	8	N	360x253x137	140x150x10	N/A
	14		760x253x137	110x140x10	N/A
	16		760x253x137	140x170x10	N/A
	18		905x253x137	160x250x10	N/A
	20		1020x253x137	150x190x10	N/A
	24		1250x525x137	180x220x10	N/A
	28		1425x525x137	200x200x10	N/A
PDIP Power	16	NP	760x253x137	160X170X10	N/A
PLCC	20	Q	350x350x155	180x180x10	N/A
	28		450x450x155	230x230x10	N/A
	44		650x650x155	230x230x10	N/A
PLCC Power	28	QP	450x450x155	200x200x10	N/A
	44		650x650x155	300x300x10	N/A

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θja, lower value is for 3x3 in. 1 oz. internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

Package Thermal Resistance Data

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
125-160	28 (8)	
90-120	28 (8)	
80-120	28 (8)	
70-90	28 (8)	
70-85	28 (8)	
60-75	28 (8)	
50-65	28 (8)	
70-80	20 (8)	
60-70	20 (8)	
N/A	5-8*	θjc estimated for backside of device, through the metalized thermal conduction pads.
58-76**	15**	Modeled using .3 mm trace width
44-59**	12**	Modeled using .3 mm trace width
31-46**	11**	Modeled using .3 mm trace width
34 (9) 38-61**	8**	Leads 5,6,7,8,17, 18,19,29,30,31,32, 42,43 and 44 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
35 (10) 43-65**	8**	Leads 4,5,6,7,8,9,28,29,30,31,32 and 33 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
238-269** 312-373**(7)	41**	Modeled using .3 mm trace width.
210-241** 273-330**(7)	39**	Modeled using .3 mm trace width.
110 (3)	50	
90 (3)	45	
90 (3)	45	
85 (3)	40	
80 (3)	35	
60 (3)	30	
60 (3)	30	
25-50 (4)	12 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle.
43-75 (3)	34	
40-65 (3)	30	
35-50 (3)	20	
28-50 (3)	14 (2)	Leads 12,13,14,15,16,17 and 18 are fused to the die attach paddle. Single layer board used 1.2 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
24-38 (3)	12 (2)	Leads 6,7,17,29,39 and 40 are fused to the die attach paddle. Single layer board used 1.1 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
QSOP	16	M	193x154x59	96x130x8	50x50x12
	20		340x154x59	96x140x8	50x50x12
	28		389x154x59	96x150x8	50x50x12
QSOP Wide Body Power	36	MWP	606x295x92	180x240x10	100x100x15 100x100x12**
	44		704x295x92	190x260x10	100x100x15 100x100x12**
SOIC Narrow Body	8	D	192x154x54	95x152x8	N/A
	14		340x154x54	83x142x8	N/A
	16		390x154x54	90x150x8	N/A
SOIC Narrow Power	8	DP	192x154x54	95x150x8	N/A
	16		390x154x54	95x165x8	N/A
SOIC Wide Body	16	DW	408x296x94	165x205x10	N/A
	18		458x296x94	145x190x10	100x100x12
	20		508x296x94	165x205x10	N/A
	24		602x296x94	165x205x10	100x100x12
	28		705x296x94	165x205x10	100x100x12
SOIC Wide Body Power	28	DWP	705x296x94	156x205x10	N/A
TO220	3	T, TH, TV	400x592x165	180x180x18	N/A
	5		400x605x165	180x180x18	N/A
TO263	3	TD	395x415x175	240x180x23	N/A
	5		395x415x175	240x180x23	N/A
TSSOP	8	PW	118x174x35	126x87x5	50x50x10
	14		197x174x35	118x150x5	100x100x10
	16		197x174x35	118x154x5	100x100x10
	20		255x174x35	118x165x5	100x100x10
	24		307x174x35	118x217x5	100x100x10
	28		382x174x35	118x217x5	100x100x10
TSSOP Power	24	PWP	307x174x35	118x217x5	100x100x10
	28		382x174x35	118x250x5	100x100x10
	28		382x174x35	118x250x5	100x100x10

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θ ja, lower value is for 3x3 in. 1 oz internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

Package Thermal Resistance Data

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
144-172**	38**	Modeled using .3 mm trace widths.
116-138**	36**	Modeled using .3 mm trace widths.
96-118**	33**	Modeled using .3 mm trace widths.
31 (11) 36-52**	8**	Leads 8,9,10,26,27 and 28 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
29 (12) 32-46**	7**	Leads 10,11,12,13,32,33,34 and 35 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
84-160 (3)	42	
50-120 (3)	35	
50-120 (3)	35	
40-70 (3)	22 (2)	Leads 2,3,6 and 7 are fused to the die attach paddle.
36-58 (3)	20 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle. Single layer board used .68 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
50-100 (3)	27	
89-102**	26**	Modeled using .3 mm trace widths.
45-95 (3)	25	
71-83**	24**	Modeled using .3 mm trace widths.
65-76**	21**	Modeled using .3 mm trace widths.
30-50 (3)	16 (2)	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. . Single layer board used 0.165 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
83*	3*	
65-75*	3*	
50-87*	3	
65-75*	3	
232-257**	32**	Modeled using .3 mm trace widths.
132-158**	15**	Modeled using .3 mm trace widths.
123-147**	15**	Modeled using .3 mm trace widths.
102-125**	14**	Modeled using .3 mm trace widths.
150 (3) 88-109**	13**	Modeled using .3 mm trace widths.
77-96**	13**	Modeled using .3 mm trace widths.
30-70 (3) 63-87**	20 (2) 9**	Leads 5,6,7,8,17,18,19 and 20 are fused to the die attach paddle. Empirical tests used 1.1 in^2 of 1 oz top copper on top of PWB for heatsinking to fused leads. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
33 (13) 61-80**	20 (2) 11**	Leads 8 and 21 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead gnd plane and .3 mm trace width.
30-70 (3) 57-79**	20 (2) 9**	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.

Package Thermal Resistance Data

Databook numbers for thermal resistance are for reference in making relative package-to-package performance comparisons and are not a statement of absolute performance in a system application.

Notes:

1) All data assumes testing with the long side of the die coinciding with the long side of the die attach mounting area.
2) Specified thermal resistance is jl (junction to lead) where noted.
3) Specified θja (junction to ambient) is for devices mounted to 5 in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in^2 aluminum PC board. Test PWB was .062 in thick and typically used 0.635 mm trace widths for power pkgs and 1.3 mm trace widths for non-power pkgs with a 100x100 mil probe land area at the end of each trace - see *Thermal Characteristics of Surface Mounted Packages* by John O'Connor.
4) Lower value is for 5 in^2 multi-layer PC board. The multi layer PWB was .062 in. thick and typically used 0.635 mm trace widths for power pkgs, 1.3 mm trace widths for non-power pkgs with a 100x100 mil probe land area at the end of each trace. The backside of the PWB used 1.0 mm traces in the X and Y directions to simulate 20% coverage by multilayer traces. Thermal vias were not used to connect fused leads to backside traces. - see "Thermal Characteristics of Surface Mounted Packages" by John O'Connor.
5) Lower value is with a finned heatsink.
6) θja tests were performed in still air. θja results will vary depending on test conditions and setup. Airflow can lower the θja value stated by 15-30%, depending on air speed, package type and PWB configuration.
7) Modeled with no internal gnd plane. Lower value is for .5 mm trace widths, higher value for .3 mm trace widths.
8) θjc data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "*The baseline values shown are worst case (mean + 2s) for a 60x60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W*".
9) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.43 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
10) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz. copper internal planes, 10 mil trace widths and 1.53 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
11) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.28 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
12) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz. copper internal planes, 10 mil trace widths and 2.74 in^2 of copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
13) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.2 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
14) Trace width for test PWBs is typically 10 mils.
15) Test conditions typically use a 110-125C junction temperature with an ambient temperature of 25-30°C.
16) Die size noted is for a thermal test die with a uniformly distributed heating area.

Typical Materials Used for Assembly

Package	Unitrode Package Code	Die Thickness (mils)	Die Attach (2)	Leadframe Material Thermal Conductivity (1)	Molding Compound or Package Material
Ceramic DIP	J	15	Eutectic or Silver Glass	75	Alumina
Ceramic LCC	L	15	Eutectic or Silver Glass	N/A	Alumina
Ceramic LCC Power	LP	15	Eutectic or Silver Glass	N/A	Alumina
LQFP	FQ	12	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
LQFP Power	FQP	12	Silver Filled Epoxy	220	Standard, non-thermally enhanced epoxy
PDIP	N	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
MSOP	P	8	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PDIP Power	NP	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PLCC	Q	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
PLCC Power	QP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
QSOP	M	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
QSOP Wide Body Power	MWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Narrow Body	D	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Narrow Power	DP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Wide Body	DW	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Wide Body Power	DWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
TO220	T	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TO263	TD	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TSSOP	PW	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
TSSOP Power	PWP	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy

Note (1): $\frac{BTU \bullet in}{ft^2 \bullet hr \bullet {}^\circ F}$.

Leadframe downset is typically 8 to 15 mils. Leadframe thickness is typically 5-10 mils.

Note (2) :Die attach thickness is between 0.5-1.5 mils for plastic devices; 1.9-2.4 mils for ceramic.

Table 1. Typical materials used for assembly.

UNITRODE

THERMAL CHARACTERISTICS OF SURFACE MOUNT PACKAGES

John A. O'Connor

Introduction

Surface mount packaging continues to expand market share, displacing dual in-line packages (DIPs) at an ever increasing rate. Smaller surface mount devices allow a significant increase in circuit density with a corresponding decrease in system size. Miniaturization is not without penalty however, as thermal management can quickly dominate system packaging design.

With the familiar DIP, the majority of heat is removed through the case. Typically, this is accomplished by convection air currents, although forced air or conduction cooling is often used in more demanding applications. Unlike the DIP however, the majority of heat is removed from surface mount packages through the leads. This means that the PC board design directly affects the thermal capability of surface mounted circuitry. For optimal thermal design, the integrated circuit, the package, and the PC board must be considered as a system.

Many designers use steady-state thermal behavior (thermal resistance) to predict IC junction temperature. While this approach certainly is valid for devices subjected to continuous power dissipation, it often results in an overly conservative design when dissipation varies over time. Generating a model which accounts for transient thermal behavior allows the designer to fully exploit the system's thermal mass. Instantaneous junction temperature can then be calculated, insuring reliability with minimal system size.

Thermal Model

Figure 1 shows the basic model which is expanded for more complex situations. The power dissipated is represented by the current source. Resistance to heat flow is represented by the resistor, and the thermal mass is represented by the capacitor. The analogous thermal units for the current, thermal resistance, and thermal capacitance are also shown in figure 1. Ground is ambient temperature, so all values are temperature rise above ambient. With more complex systems, it is usually easiest to initially convert to electrical units, analyze the circuit, then convert back to thermal units. This approach allows standard electrical circuit analysis tools and techniques to be used without unnecessary confusion.

A surface mounted device on a PC board can be modeled as in figure 2. Each R-C section roughly

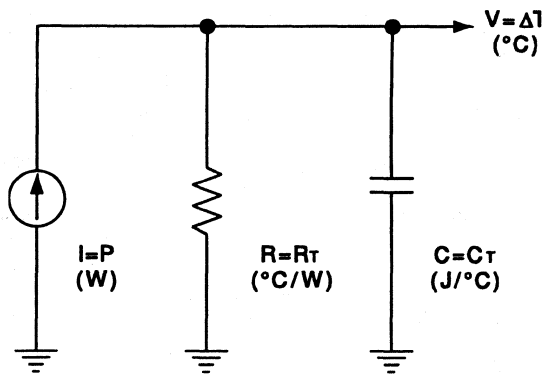


Figure 1. Basic Thermal Model

correlates to the physical system. The first R-C is the device die. The second is the lead frame and package, and the third is the PC board. Other parameters such as the junction to case and case to ambient thermal resistances, are lumped into the three R-C sections. This simplification does cause transient thermal response errors, although normally these errors are small. The additional elements can be broken out separately if greater accuracy is required. Although the physical correlation is far from perfect for the 3 R-C model, the thermal correlation can be very good.

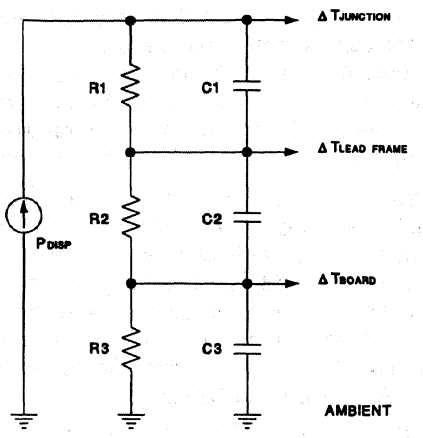


Figure 2. Surface Mounted Device on a PC Board Model

Parameter Measurement

The circuit technique shown in figure 3 can be used to evaluate the thermal performance of almost any IC. Device power dissipation must be known and constant. This is achieved with resistive loading for devices such as voltage regulators or amplifiers. Other devices may require additional circuitry to insure constant dissipation.

The change in forward voltage of a diode is typically utilized for temperature measurement, although any temperature dependant parameter could also be used. Ideally, the diode should be close to the output transistors for maximum accuracy. In practice, this is not critical since the temperature drop across the die will only be a few degrees C in a surface mountable IC. During the test, the measurement diode must not have any current other than the fixed bias current. The bias current should be as small as possible to avoid self-heating the diode.

Many devices have a diode intended for forward biased operation in the actual application circuit such as an output stage clamping diode. If such a diode is not available it may be necessary to forward bias a parasitic diode for measurement. While this approach should be considered a last resort, it can yield acceptable data. If a parasitic diode is forward biased, erratic or unspecified behavior is likely, even with low bias currents. Evaluate the test circuit carefully, insuring that dissipation is constant over the measurement temperature range.

Kelvin all connections to avoid interconnect voltage drops. Every 2mV is approximately 1°C, so even small DC offsets can cause significant error. Without any power applied to the device other than the diode bias current, characterize the diode's forward voltage in an oven at several temperatures over the expected operating junction temperature range. The slope of a best-fit line gives the thermal coefficient (T_C) which is used in subsequent calculations.

Thermocouples are used to sense PC board and ambient temperature. PC board temperature is measured as close to the device as possible.

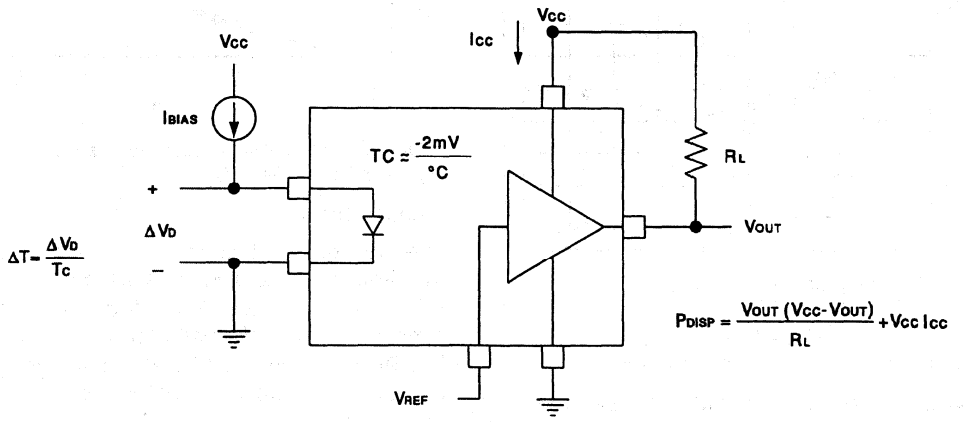


Figure 3. Typical Thermal Test Circuit

Some parameters are measured directly while others are derived by curve fitting. Junction to PC board, and PC board to ambient thermal resistance are measured by dissipating a constant power. Allow 15 minutes for the temperature to stabilize. The change in diode forward voltage and PC board temperature give the junction to ambient and board to ambient thermal resistance:

$$R_{(j\text{-}a)} = \Delta V_D / (T_C P_{DISP})$$

$$R_{(b\text{-}a)} = \Delta T_B / P_{DISP}$$

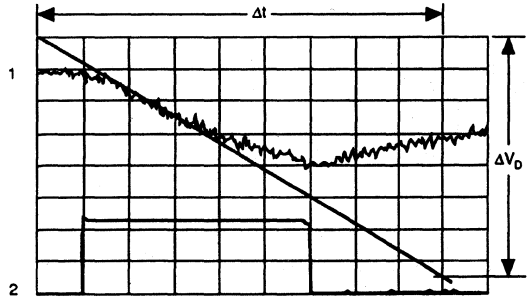
Note that these resistances are based on change in temperature - ambient is assumed constant for the duration of the test. These values correlate to R1, R2, and R3 by:

$$R1 + R2 = R_{(j\text{-}a)} - R_{(b\text{-}a)} \quad (1)$$

$$R3 = R_{(b\text{-}a)} \quad (2)$$

The thermal capacitance of the die is measured by applying a pulsed load and recording the junction temperature waveform. Varying the dissipation pulse width allows observation of each capacitance's effect, although only the die's thermal capacitance can be measured directly. A typical 10ms transient dissipation waveform is shown in figure 4. The thermal time constant of the die is on the order of 30ms. To minimize exponential decay error, the slope of the waveform is measured at (t) = 3ms. The die's thermal capacitance is then:

$$C1 = P_{DISP}\, \Delta t\, T_C / \Delta V_D \quad (3)$$



VERTICAL: (1) V_D, 1mV/DIV
(2) P_{DISP}, 1W
HORIZONTAL: 2ms/DIV

Figure 4: 10ms Transient Dissipation Waveform

Transient waveforms should also be taken for 100ms, 1s, and 10s dissipation intervals to generate an accurate temperature versus time curve. If transient thermal behavior is critical beyond 10 seconds then additional curves must be taken. The thermal time constant of the PC board can go out to several minutes, so a strip chart recorder or computer based data acquisition system will be required. For most systems, this additional data is unnecessary.

The remaining parameters are determined by curve fitting. Visual comparison of measured versus calculated curves is easily done with a spread sheet program. Measured junction temperature versus time data (4 points per decade is sufficient) is entered into the spread sheet. Junction temperature is then calculated at each point with estimated values for R2 and C2 and C3 using:

$$T(t) = P_{DISP}\,[R1(1-e^{-t/\tau 1}) + R2(1-e^{-t/\tau 2}) + R3(1-e^{-t/\tau 3})] \quad (4)$$

Data presented in the following section will help in estimating initial values. This procedure is iterated until an acceptable curve fit is achieved. C3's value is iterated only if the measured curve goes out to several minutes. Figure 5 is a typical measured and calculated junction temperature versus time curve. A logarithmic time axis aids in curve fitting by spreading data points evenly.

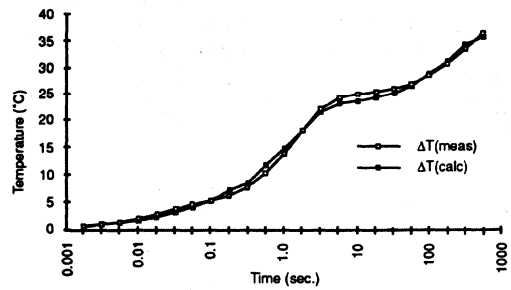


Figure 5. Juction Temperature versus Time for FQP48 Package Dissipating 1W.

Typical Data

The preceding technique was used to characterize two devices in nine different packages. Five different PC board types were also tested to provide relative comparison. This information should be used to help initially determine package, PC board type, and layout. It must be stressed that this typical data should not substitute for a rigorous thermal analysis of the actual application.

PACKAGE	R1 (°C/W)	C1 (J/°C)	τ1 (sec)	R2 (°C/W)	C2 (J/°C)	τ2 (sec)	R3 (°C/W)	C3 (J/°C)	τ3 (sec)	R(J-a) (°C/W)
D8	5	0.0035	0.02	64	0.030	1.9	15	24	360	84
D14	4	0.0045	0.02	45	0.035	1.6	16	24	384	65
DW16	4	0.0045	0.02	44	0.070	3.1	15	24	360	63
DW16	4	0.011	0.04	34	0.11	3.7	13	24	312	51
DWP28	2.5	0.008	0.02	13	0.13	1.7	15	24	360	30
Q20	3	0.010	0.02	26	0.12	3.1	14	24	336	43
Q28	2.5	0.008	0.02	25	0.12	2.9	13	24	312	40
QP28	2.5	0.009	0.02	12	0.25	3.0	14	24	336	28
FQ48	4	0.006	0.02	57	0.07	4.0	15	24	360	76
FQP48	4	0.005	0.02	21	0.08	1.7	14	25	350	39

Figure 6. Model Values Versus Package Type for 1W Dissipation on Aluminum PC Board.

Figure 6 shows model values and time constants versus package type, mounted on an aluminum PC board [1]. Junction to ambient thermal resistance is also shown to indicate overall steady state thermal performance. All data was taken with one watt dissipated. The values that were determined by curve fitting result in a fairly conservative model. Values were chosen which tended to predict higher temperature than actually measured where errors could not be eliminated. As indicated, two devices were used for testing. At 7,500 square mils, the UC3730 is representative of the smaller dies typically packaged in D8, D14, and DW16 packages. The UC3173 is 16,500 square mils, and is typical of the dies packaged in the other larger packages.

Both devices were packaged in the DW16 to isolate the effect of die size. The UC1730's smaller die increased R2 by about 30%. Interpolating between these two data points is difficult since the relationship between die size and thermal resistance is nonlinear. Curves are available which account for this dimensional difference [2], although the actual conditions differ and are more complicated than the configuration used to generate the curves. Fortunately, the resulting error will be small in most applications. Conservatively estimating R2 will minimally impact system size, but if a more accurate value is required the actual device can be characterized on a test PC board.

Figure 7 illustrates the power lead frame's dramatic improvement in thermal performance over standard lead frames by comparing the junction to ambient thermal resistances of the QP28 to the Q28, and the FQP48 to the FQ48. Standard lead frames connect the die to the leads thermally through the epoxy molding compound. Power lead frame packages incorporate a single piece for die attachment and ground leads. This uninterrupted, high thermal conductivity path offers a significant improvement over standard lead frames. Occasionally a stiffer but less conductive alloy is used for standard lead frames. The FQ48's poorer thermal performance is partially caused by the lower conductivity alloy.

Printed circuit board design significantly affects the overall thermal performance of the system, particularly with the power lead frame packages. The UC3173 in the DWP28 package was used to

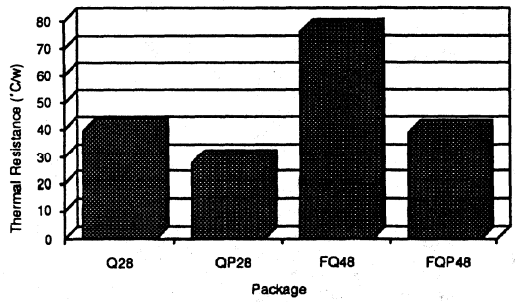


Figure 7. Power lead frames significantly reduce thermal resistance.

compare PC board thermal performance. Five different PC board types were evaluated with one watt dissipated:

1. Single side 1 oz. copper, 0.062 aluminum
2. Single side 1 oz. copper, 0.062 FR4 epoxy fiberglass
3. Single side 2 oz. copper, 0.062 FR4 epoxy fiberglass
4. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.031 FR4 epoxy fiberglass
5. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.062 FR4 epoxy fiberglass

PCB TYPE	R(b-a) (°C/W)	C(b-a) (J/°C)	τ (sec)
Aluminum	15	24	360
FR4-1oz	31	2.5	78
FR4-2oz	25	3	74
4 layer-0.031	21	4	84
4 layer-0.062	19	5	94

Figure 8. Board to ambient thermal resistance and capacitance versus PC board type for DWP28 package dissipating 1W.

The thermal resistance, capacitance, and time constants for the five PC boards are shown in figure 8. The PC board layouts used for testing are shown in figure 9. Only the component side is shown for the four layer boards. The back side, which has 10 mil traces on 50 mil centers to provide a typical amount of interconnect copper, and the Vcc plane were unconnected. The inner ground plane is connected to the small component side ground plane through 16 feed-throughs.

As expected, the aluminum PC board's significantly higher specific heat results in nearly an order of magnitude increase in thermal capacitance. Surprisingly the four layer 0.062 board's thermal resistance is nearly as low as the aluminum board's, indicating good heat distribution through the inner planes. Note that although the Vcc plane is unconnected, it does help distribute the heat across the board. Conduction or forced air cooling is necessary to fully exploit the aluminum board's capability.

Summary

A method for accurately modeling the thermal behavior of a surface mounted IC has been presented. The model relies on measured data, insuring excellent correlation to the physical system. Typical thermal behavior of nine different packages and five different PC boards were also presented, indicating relative thermal performance differences. Optimum thermal system design is achievable using the techniques and data presented.

References

1. Thermal Clad insulated metal substrates, The Bergquist Company, 5300 Edina Industrial Blvd., Minneapolis, MN 55439, 612-835-2322
2. R. Tummala, E. Rymaszewski, "Microelectronics Packaging Handbook", Van Nostrand Reinhold, 1989, pp173-179

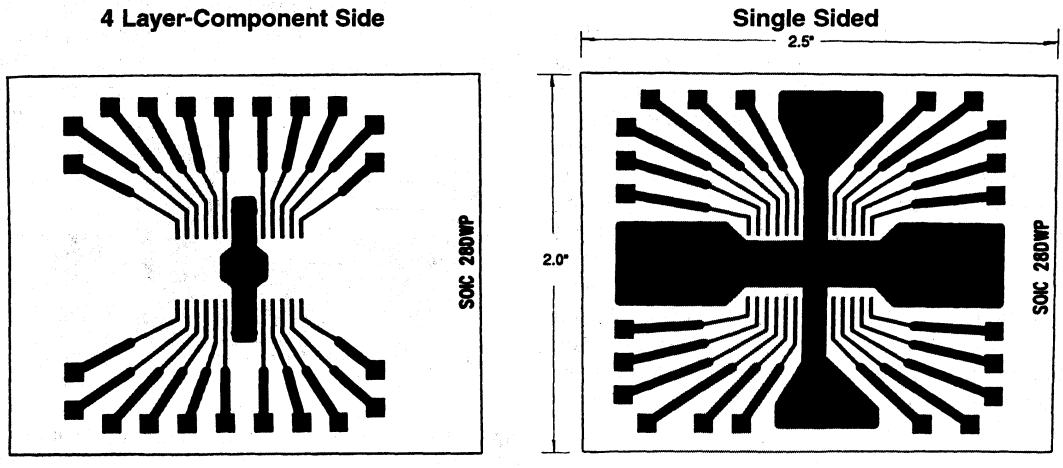
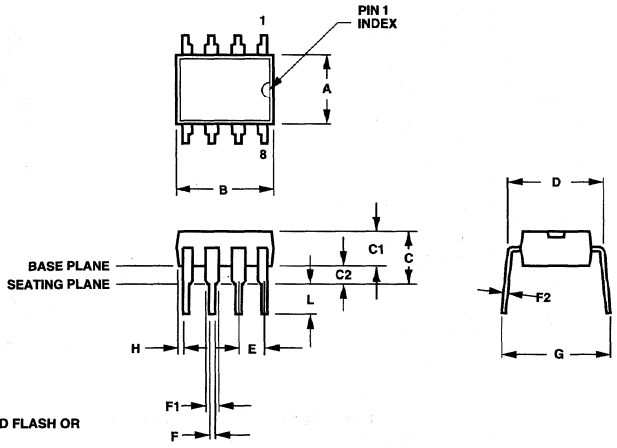


Figure 9. Test PC Board Layouts (SOIC 28DWP)

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

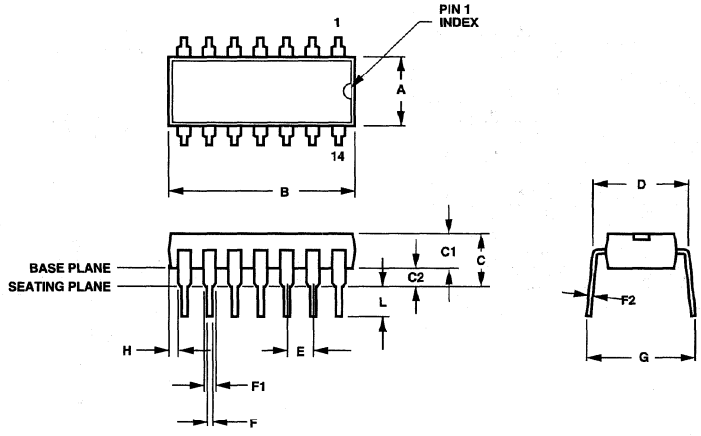
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

14-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

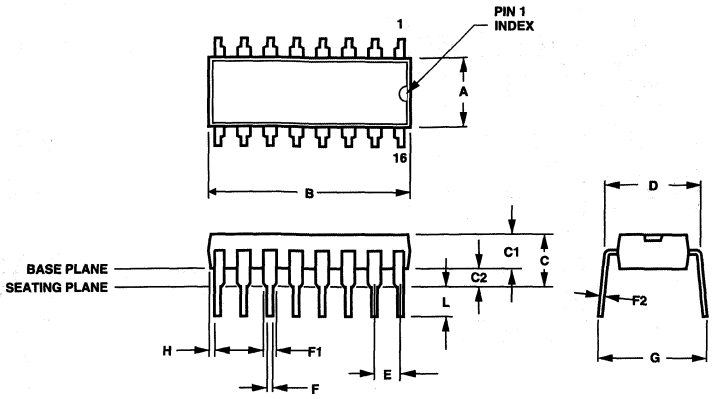
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

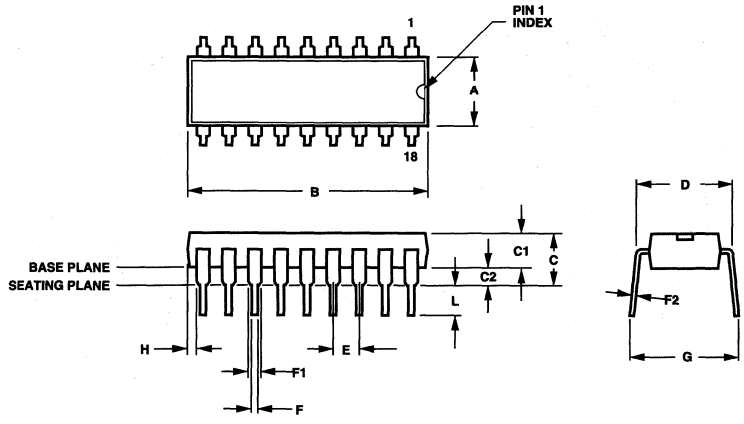
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

18-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

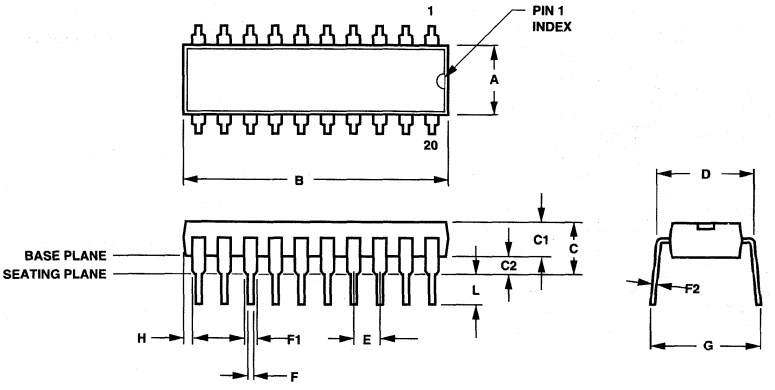
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

20-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

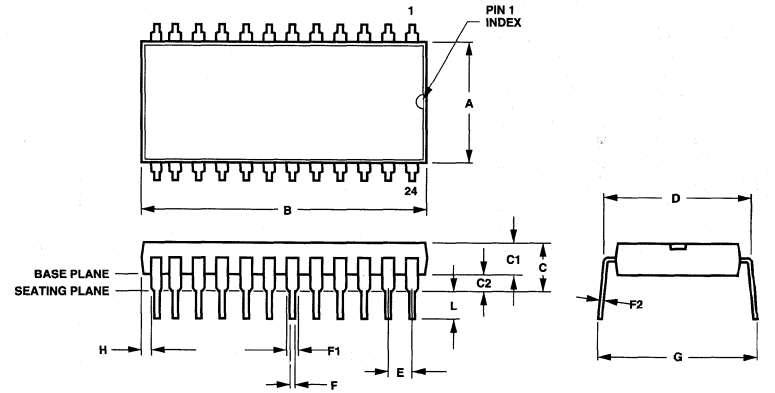
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	1.010	1.030	25.65	26.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

24-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

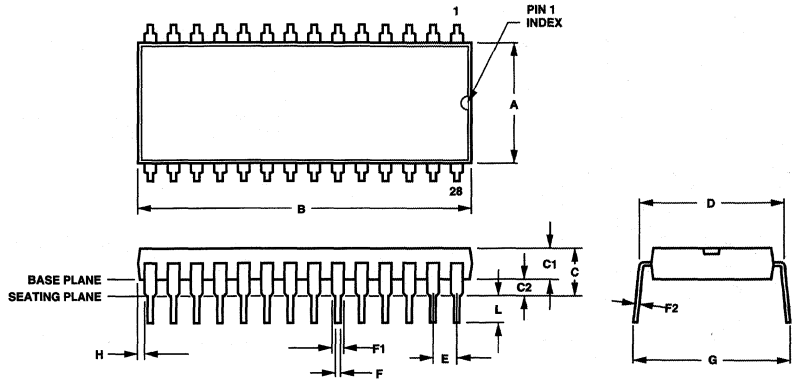
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.230	1.270	31.24	32.26	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

28-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

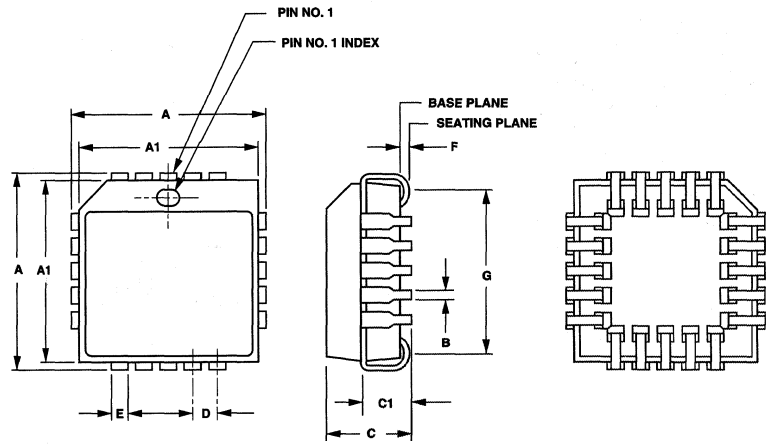
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.380	1.470	35.10	37.34	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

20-PIN PLASTIC PLCC SURFACE MOUNT ~ Q PACKAGE SUFFIX

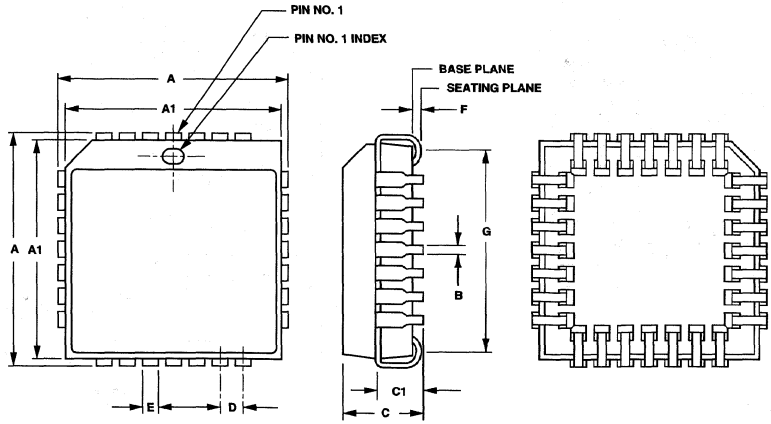
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.290	.330	7.37	8.38	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

28-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

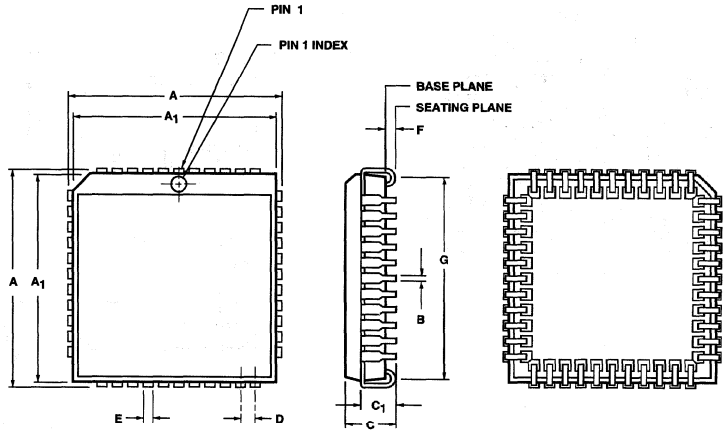
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.485	.495	12.32	12.57	
A1	.450	.456	11.43	11.58	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.390	.430	9.91	10.92	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

44-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

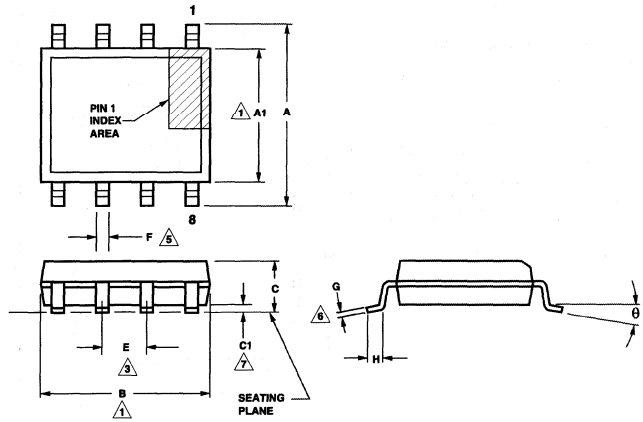
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.685	.695	17.40	17.65	
A1	.650	.656	16.51	16.66	1
B	.013	.021	0.33	0.53	
C	.165	.180	4.19	4.57	
C1	.095	.110	2.41	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3,4
G	.590	.630	14.99	16.00	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

8-PIN SOIC SURFACE MOUNT - D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

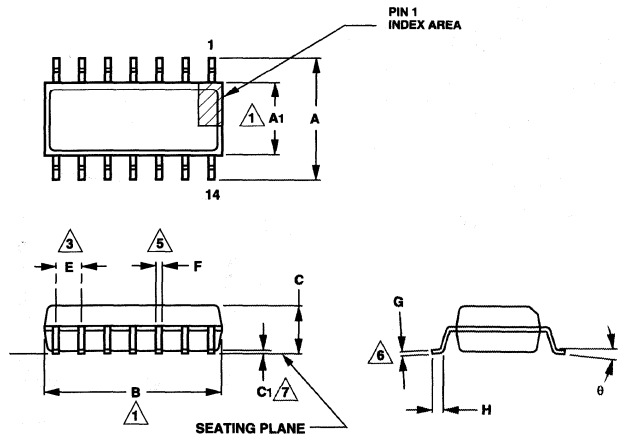


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

14-PIN SOIC SURFACE MOUNT - D PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

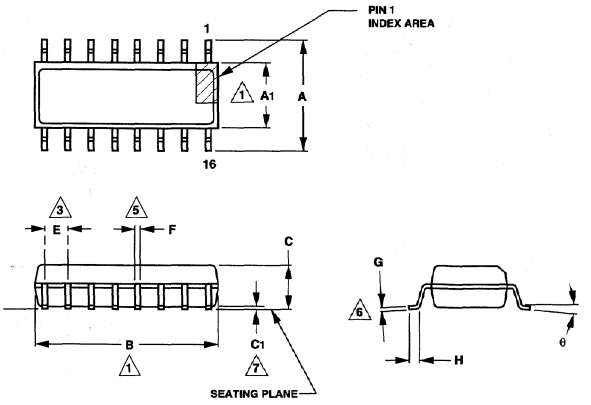


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SOIC SURFACE MOUNT ~ D, DP, DS PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

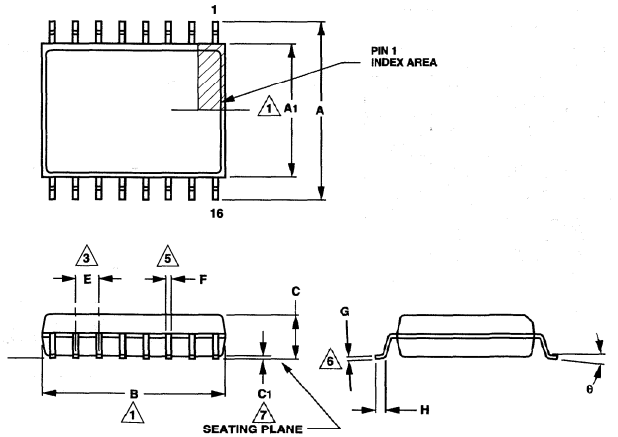


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

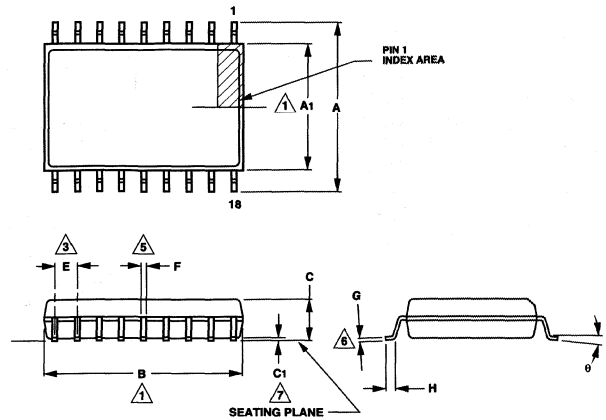


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

18-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

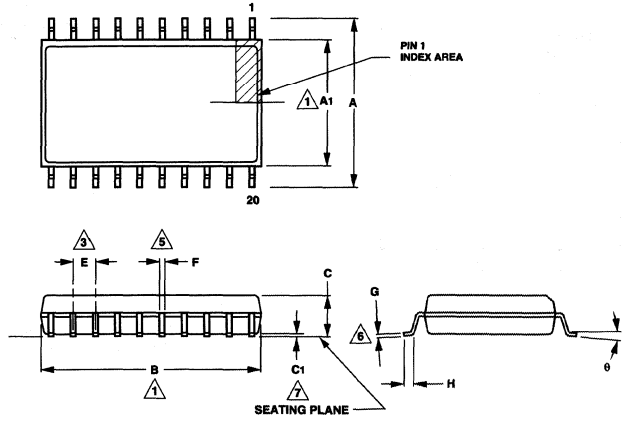


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

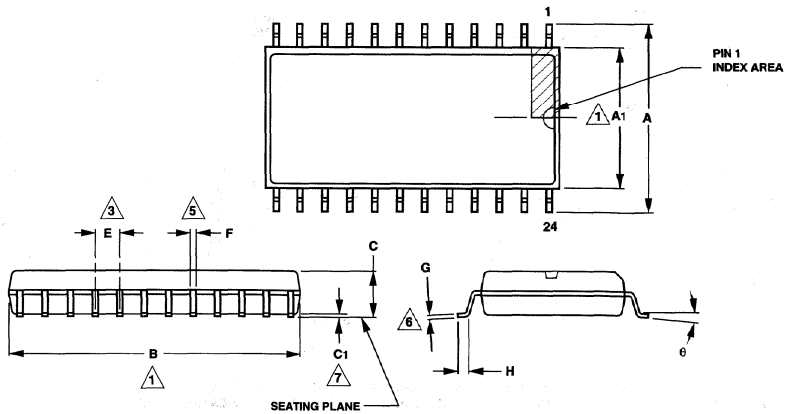


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

24-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.598	.606	15.20	15.40
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.019	.035	0.46	0.89
θ	0°	8°	0°	8°

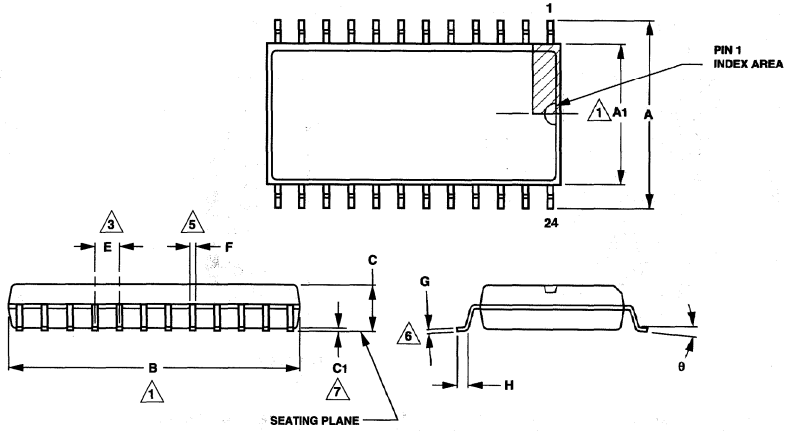


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

28-PIN SOIC SURFACE MOUNT ~ DW, DWP PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.698	.712	17.73	18.08
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

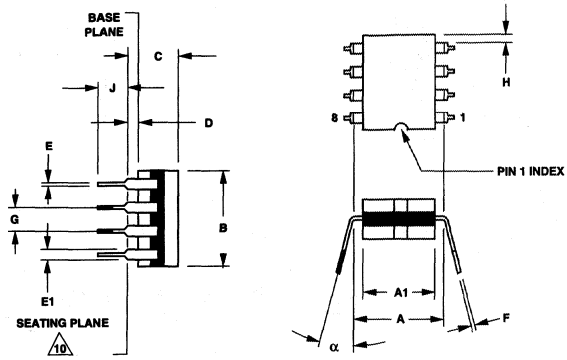


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.405	—	10.29	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

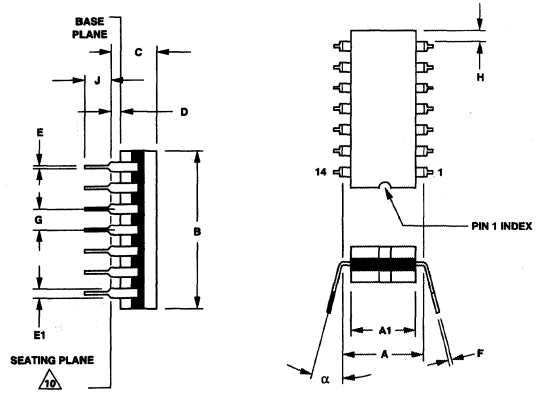


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

14-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.785	—	19.94	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

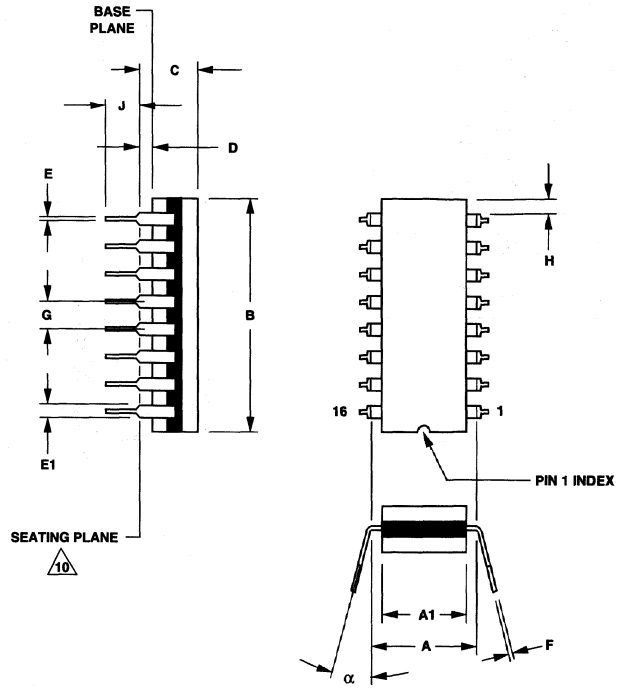


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.840	—	21.34	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

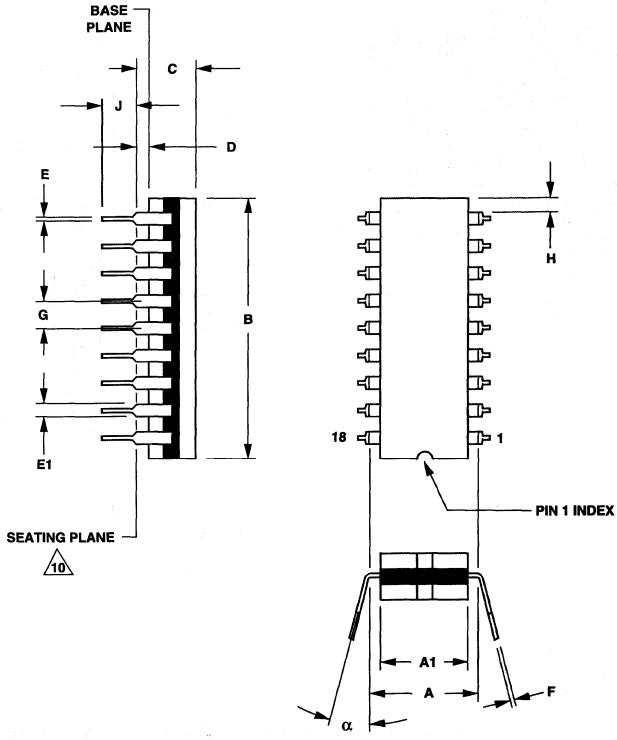


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

18-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.960	—	24.38	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

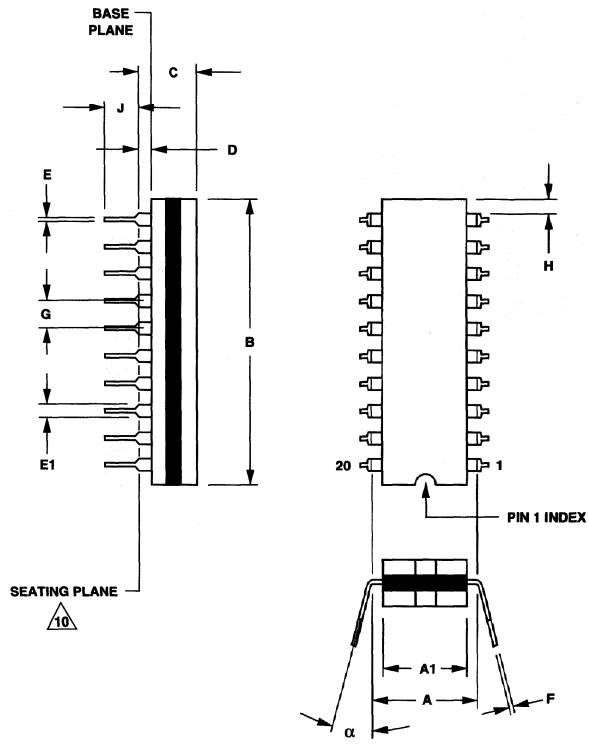


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 9, 10 AND 18 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 9, 10 AND 18).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

20-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	1.060	—	26.92	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



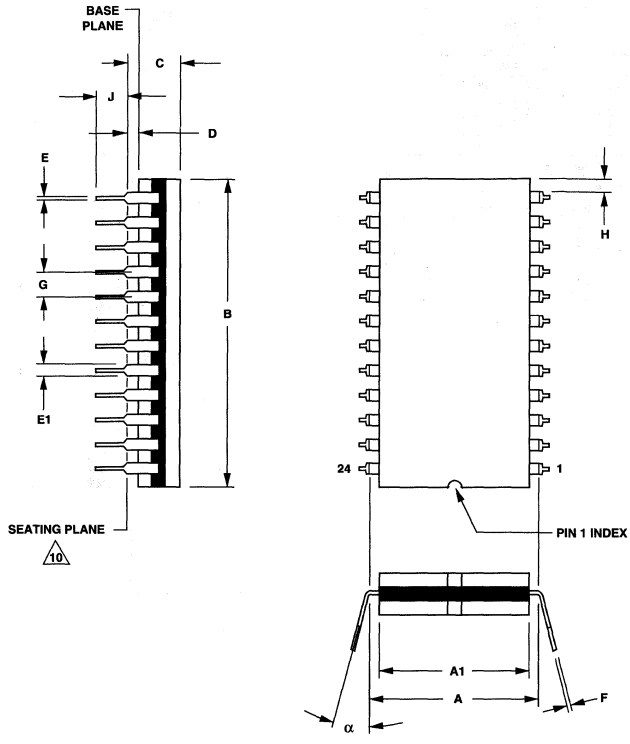
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 10, 11 AND 20 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 10, 11 AND 20).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α = 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY,

10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

24-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.515	0.605	13.08	15.37	4
B	1.180	1.260	29.97	32.00	4
C	—	0.225	—	5.72	
D	0.015	0.055	0.38	1.40	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	0.065	0.127	1.65	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

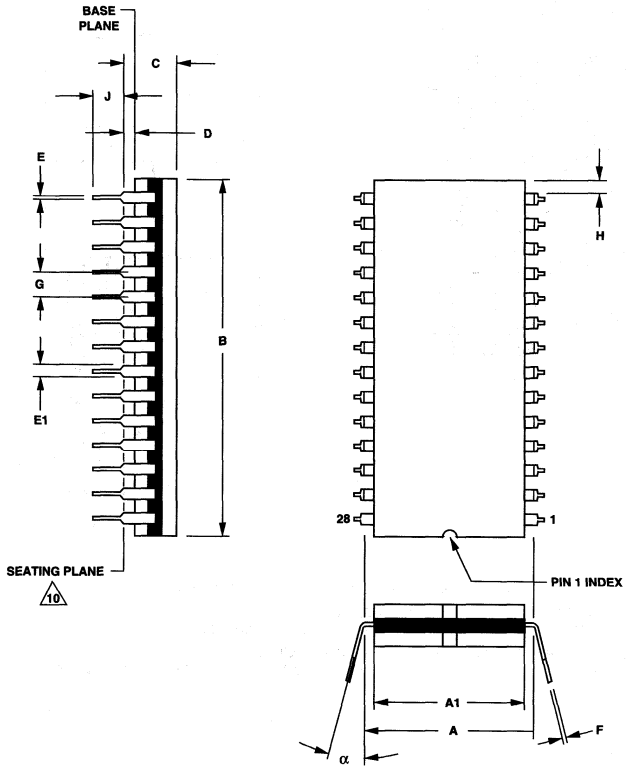


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 12, 13 AND 24 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 12, 13 AND 24).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

28-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.570	0.605	14.48	15.37	4
B	1.380	1.460	35.05	37.08	4
C	—	0.225	—	5.72	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.127	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

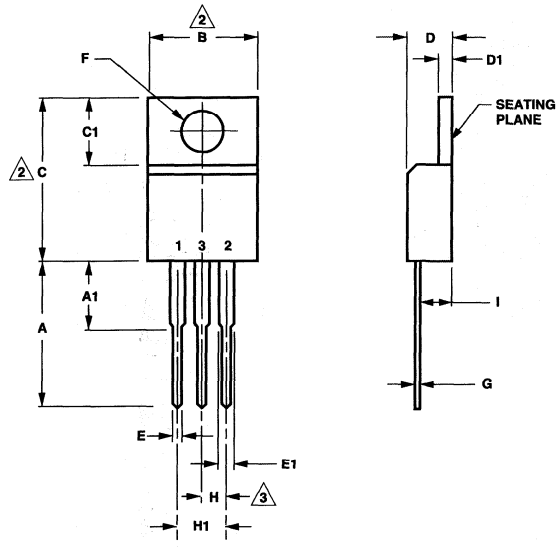


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENT IFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 14, 15 AND 28 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 14, 15 AND 28).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

3-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A1	–	.250	–	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E1	.045	.070	1.14	1.77
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.090	.110	2.29	2.79
H1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



NOTES:

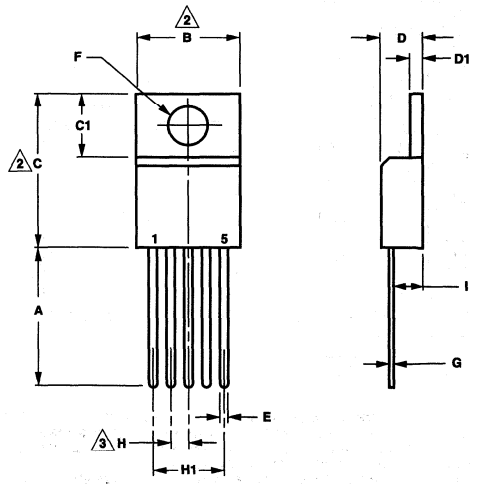
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

2 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.

3 THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES.
EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

5-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

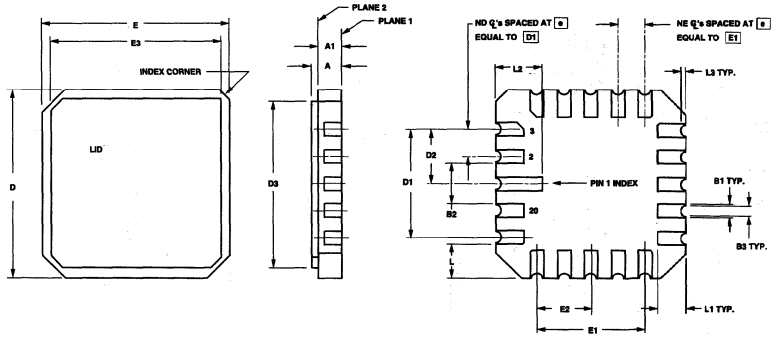
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D1	.045	.055	1.14	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.057	.077	1.45	1.96
H1	.258	.278	6.55	7.06
I	.080	.115	2.03	2.92



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.067 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

20-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

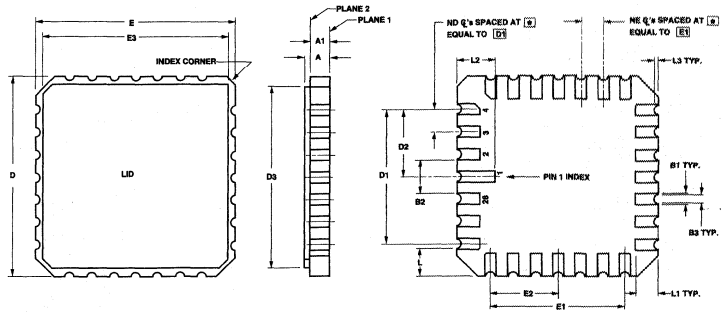
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	–	.358	–	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

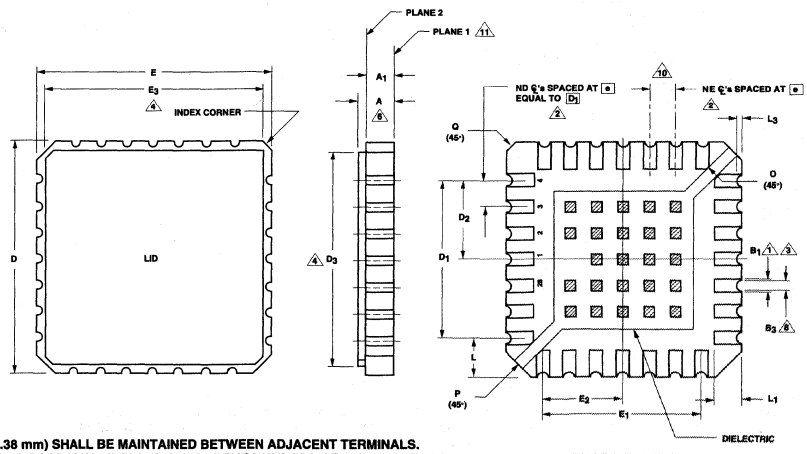
	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	–	.460	–	11.68	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	28		28		2
ND/NE	7		7		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BELOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ LP PACKAGE SUFFIX

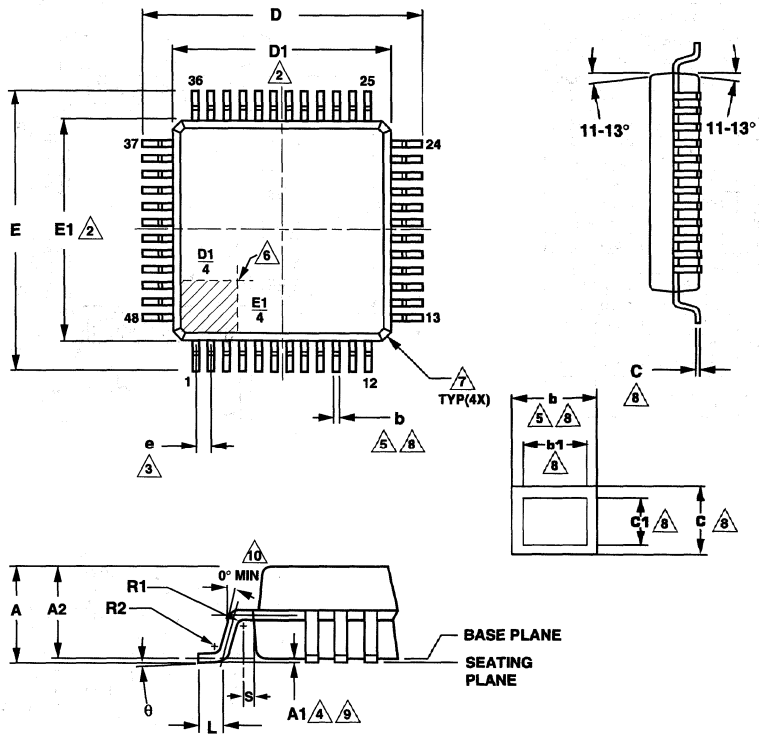
	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.060	.100	1.52	2.54
A1	.050	.088	1.27	2.24
B1	.022	.028	0.56	0.71
B3	.006	.022	0.15	0.56
D/E	.442	.458	11.23	11.63
D1/E1	.300 BSC		7.62 BSC	
D2/E2	.150 BSC		3.81 BSC	
D3/E3	–	.460	–	11.68
L	.075 REF		1.905 REF	
L1	.045	.055	1.14	1.40
L3	.003	.013	0.08	0.33
N	28		28	
ND/NE	7		7	
O	.006 REF		0.152 REF	
P	.040 REF		1.016 REF	
Q	.020 REF		0.508 REF	
e	.050 BSC		1.27 BSC	



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

48-PIN LQFP ~ FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	1.60	–	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
b	0.17	0.27	.007	.011
b1	0.17	0.23	.007	.009
C	0.09	0.20	.003	.008
C1	0.09	0.16	.003	.006
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
e	0.50 BSC		.020 BSC	
L	0.45	0.75	.018	.030
R1	0.08	–	.003	–
R2	0.08	0.20	.003	.008
S	0.20	–	.008	–
θ	0°	7°	0°	7°

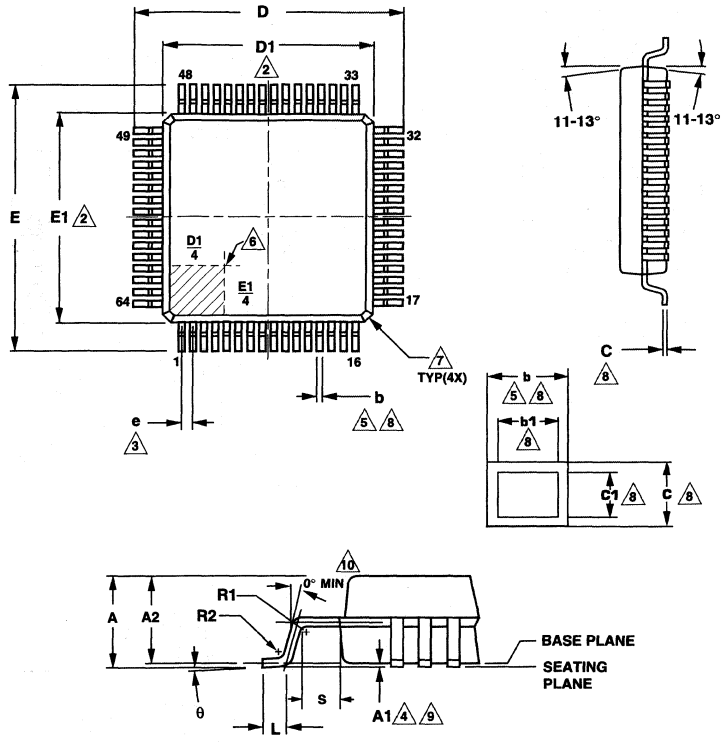


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1'AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1'AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

64-PIN LQFP - FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.53	0.57
b	0.17	0.27	0.007	0.011
b1	0.17	0.23	0.007	0.009
C	0.09	0.20	0.004	0.008
C1	0.09	0.16	0.004	0.006
D	12.00 BSC		0.472 BSC	
D1	10.00 BSC		0.393 BSC	
E	12.00 BSC		0.472 BSC	
E1	10.00 BSC		0.393 BSC	
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.18	0.03
R1	0.08	–	0.003	–
R2	0.08	0.20	0.003	0.008
S	0.20	–	0.008	–
θ	0°	7°	0°	7°

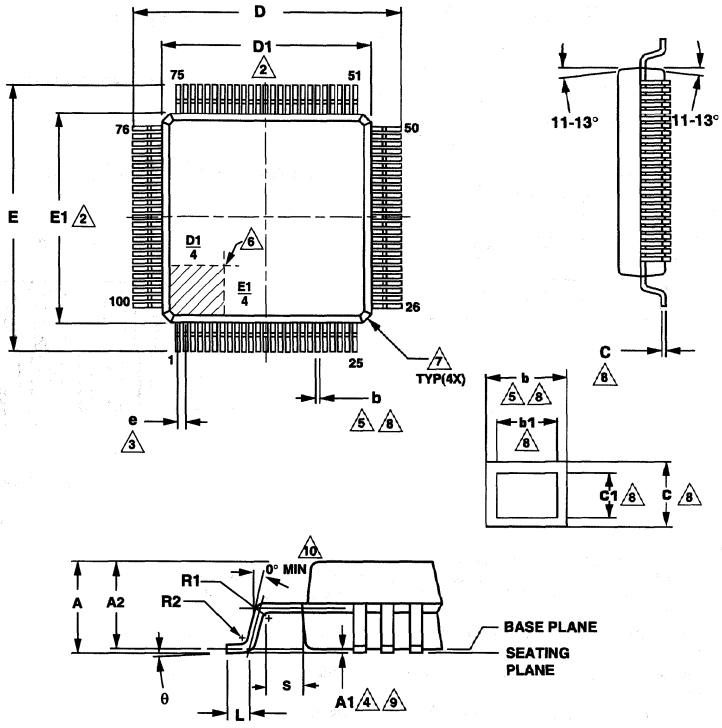


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1' AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

100-PIN LQFP ~ FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.53	0.57
b	0.17	0.27	0.007	0.011
b1	0.17	0.23	0.007	0.009
C	0.09	0.20	0.004	0.008
C1	0.09	0.16	0.004	0.006
D	16.00 BSC		0.630 BSC	
D1	14.00 BSC		0.551 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.18	0.03
R1	0.08	–	0.003	–
R2	0.08	0.20	0.003	0.008
S	0.20	–	0.008	–
θ	0°	7°	0°	7°

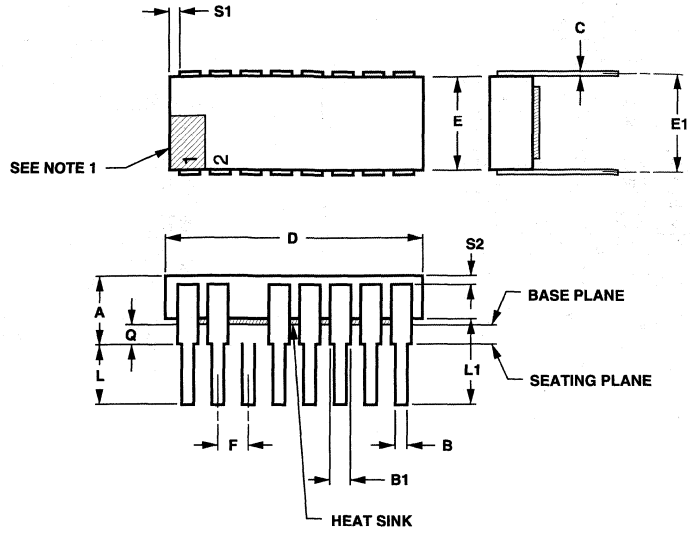


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1'AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1'AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

16-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.200	–	5.08	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	.840	–	21.34	4
E	.220	.310	5.59	7.78	4
E_1	.290	.320	7.37	8.13	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	

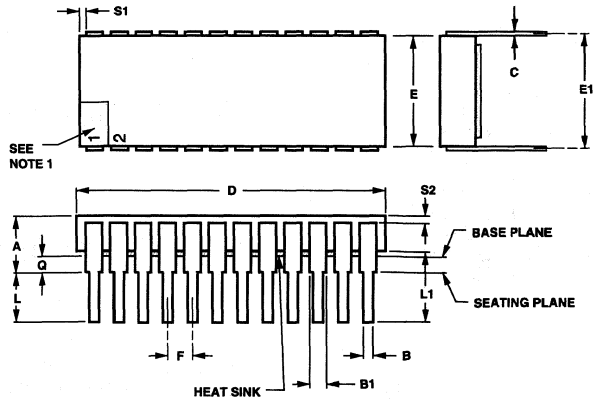


NOTES:

1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN.THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN. (0.58mm) FOR CORNER LEADS.
3. DIMENSION 'Q' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN. (2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN.(0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 14 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

24-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

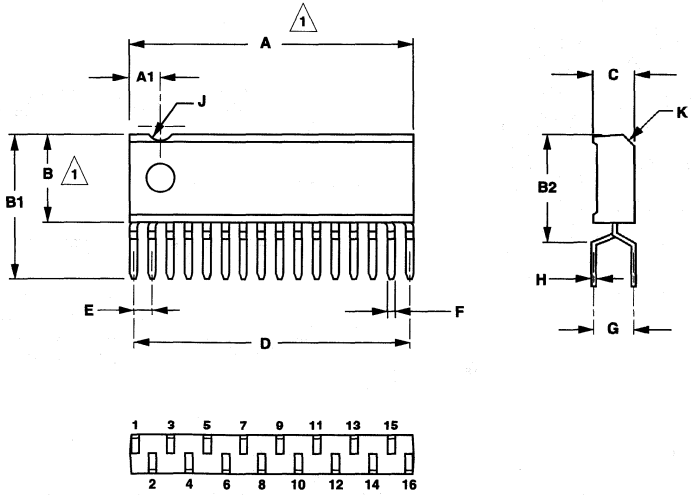
	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.225	–	5.72	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	1.220	–	30.99	4
E	.580	.610	14.73	15.49	4
E_1	.585	.615	14.86	15.62	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	



NOTES:
1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN.(0.58mm) FOR CORNER LEADS.
3. DIMENSION "Q" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN.(2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN. (0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 22 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN ZIG-ZAG INLINE ~ Z PACKAGE SUFFIX

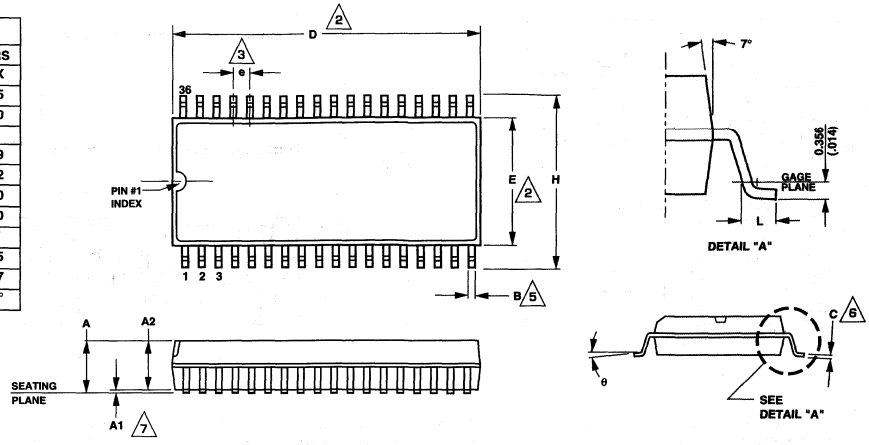
	DIMENSIONS				
	MILLIMETERS		INCHES		NOTES
	MIN	MAX	MIN	MAX	
A	19.40	19.60	.764	.772	
A1	–	2.00	–	.079	
B	5.70	5.90	.224	.232	
B1	9.40	10.40	.370	.409	
B2	6.50	7.50	.256	.295	
C	2.70	2.90	.106	.114	
D	18.75	19.35	.738	.762	
E	1.07	1.47	.042	.058	
F	0.45	0.65	.018	.026	
G	2.50	3.00	.098	.118	
H	0.23	0.35	.009	.014	
J	1.00 BSC		.039 BSC		RAD.
K	1.00 BSC		.039 BSC		CHAM.



NOTES:
1. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm (0.006 IN.) PER SIDE.

36-PIN QSOP ~ MWP PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.598	.614	15.20	15.60
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°

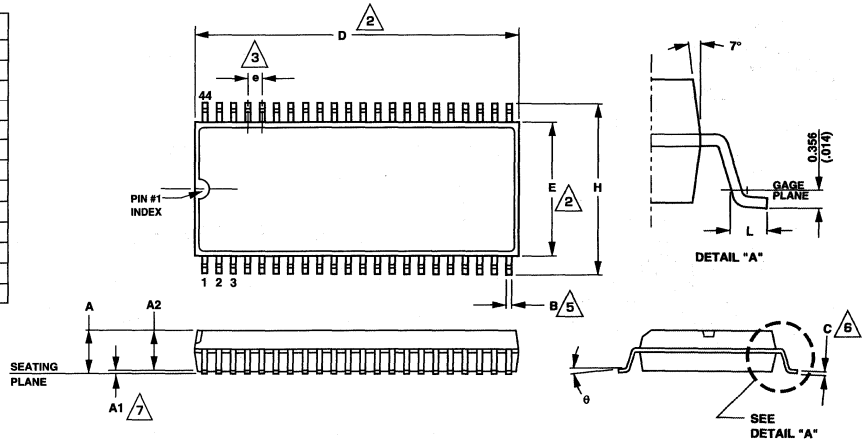


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

44-PIN QSOP ~ MWP PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.697	.712	17.70	18.10
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°

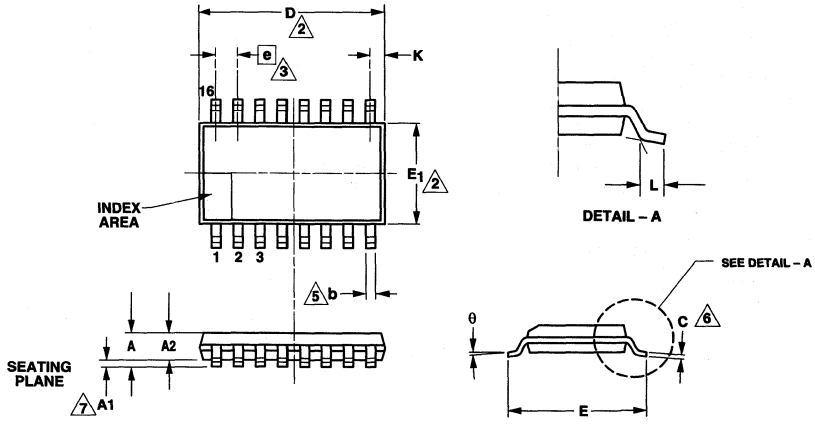


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN QSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.189	.197	4.80	5.00
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.009 REF		.23 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

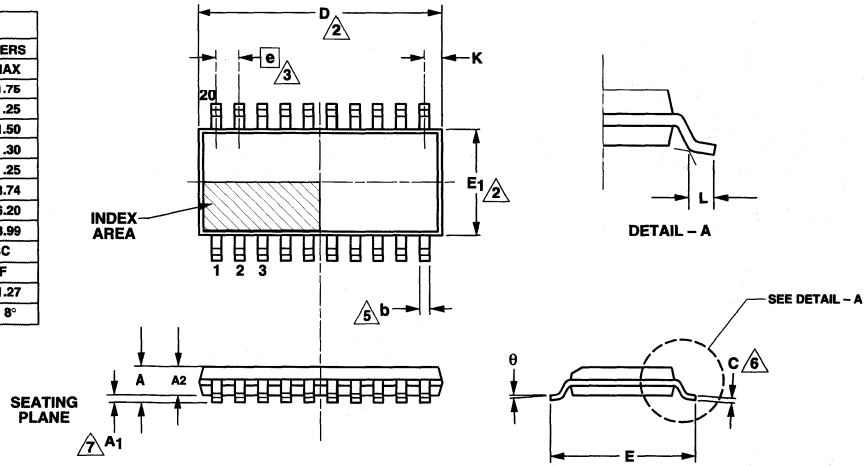


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN QSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A_1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.337	.344	8.56	8.74
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.058 REF		1.47 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

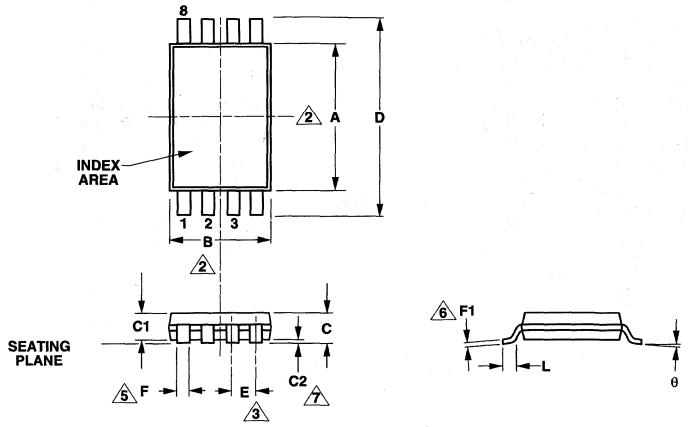


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED "b" MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

8-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	2.9	3.1	0.114	0.122
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

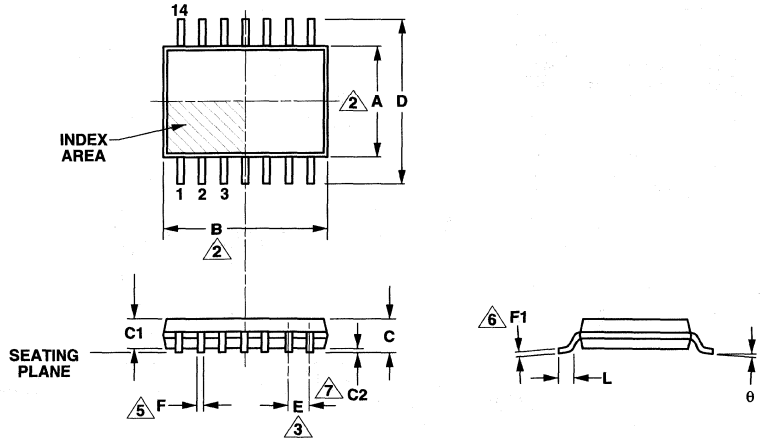


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

14-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

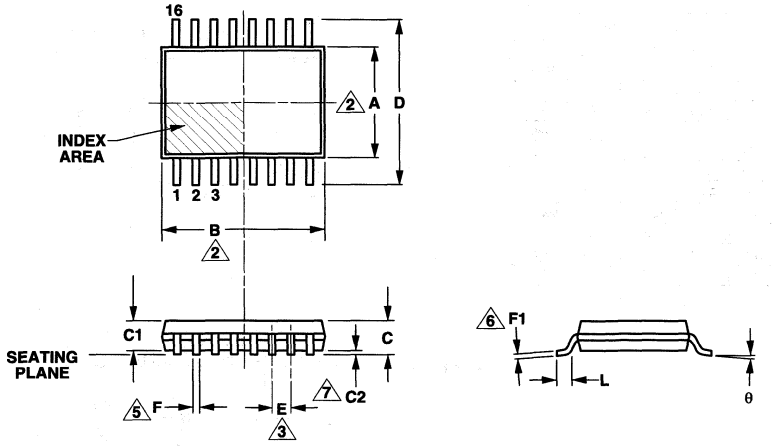


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

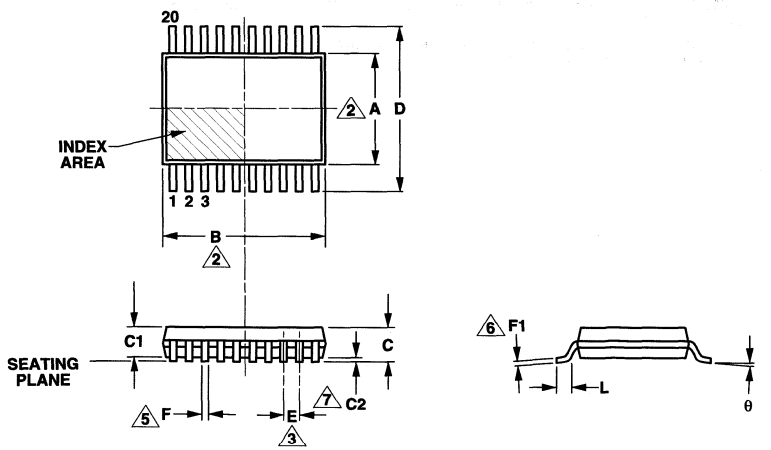


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	6.40	6.60	.252	.260
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

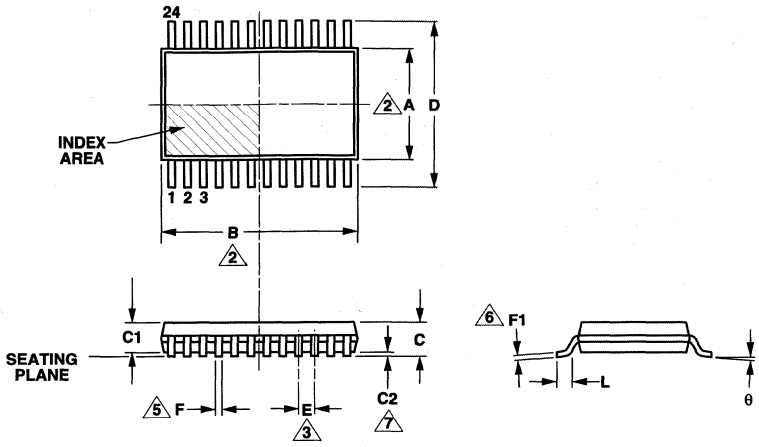


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

24-PIN TSSOP ~ PW, PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	7.70	7.90	.303	.311
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°



NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.

2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.

3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.

4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE

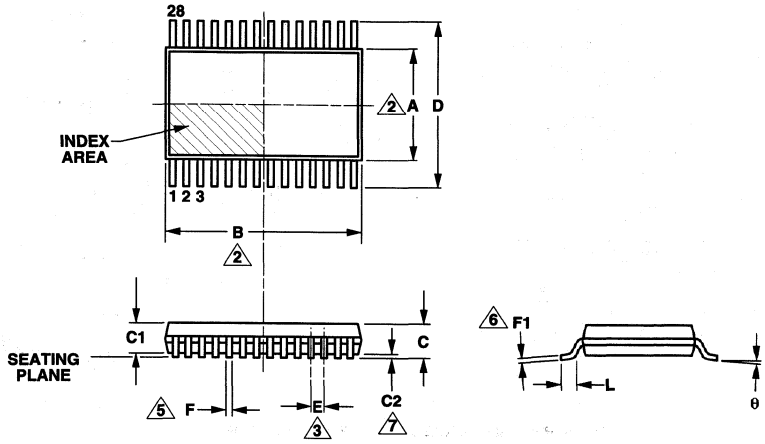
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

28-PIN TSSOP ~ PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	9.60	9.80	.378	.386
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

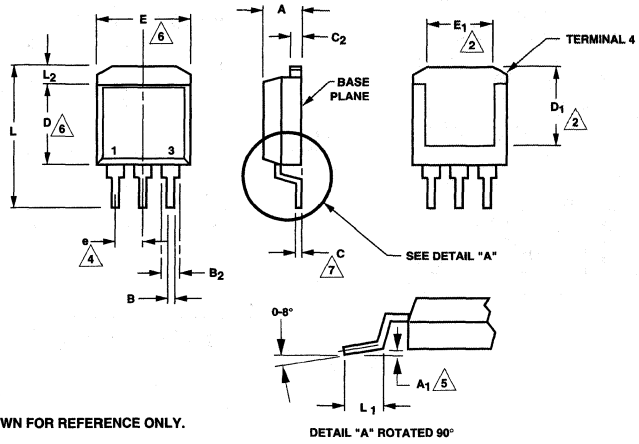


NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

3-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
B_2	.045	.050	.055	1.14	1.27	1.40
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.100 BSC			2.54 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68

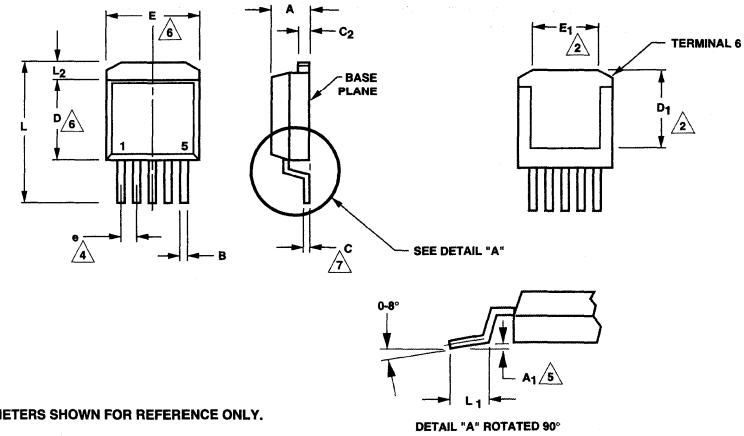


NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.100 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

5-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.067 BSC			1.70 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68

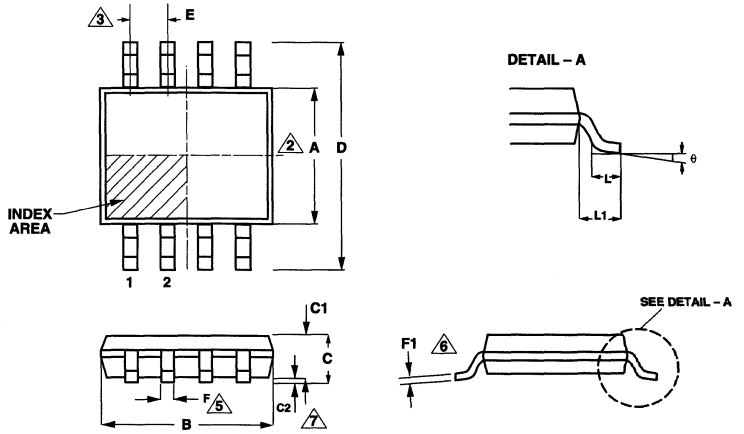


NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.067 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

8-PIN MINI SO ~ P PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.84	3.15	.112	.124
B	2.84	3.15	.112	.124
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	4.9 BSC		0.193 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.20	0.46	0.008	0.018
F1	0.08	0.28	0.003	0.011
L	0.41	0.71	0.016	0.028
L1	0.94 REF.		0.037 REF.	
θ	0°	6°	0°	6°

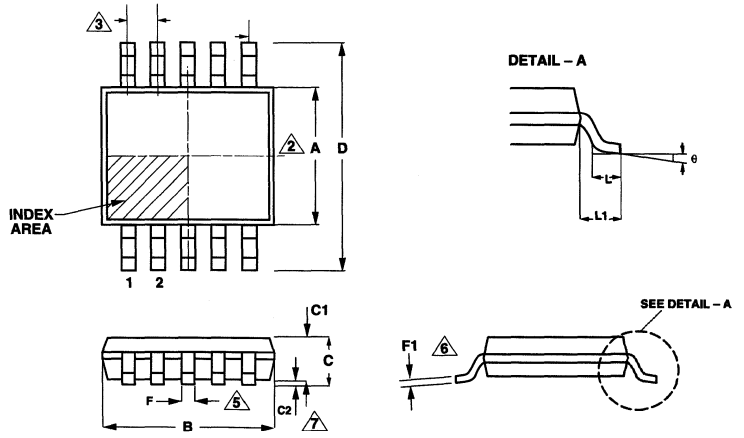


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

10-PIN MINI SO ~ P PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.84	3.15	.112	.124
B	2.84	3.15	.112	.124
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	4.9 BSC		0.193 BSC	
E	0.50 BSC		0.0197 BSC	
F	0.15	0.41	0.006	0.016
F1	0.08	0.28	0.003	0.011
L	0.41	0.71	0.016	0.028
L1	0.94 REF.		0.037 REF.	
θ	0°	6°	0°	6 °



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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